FEM Modeling of Temperature Distribution of a Flip-Chip No-Flow Underfill Package During Solder Reflow Process

Zhuqing Zhang, *Member, IEEE*, Suresh K. Sitaraman, and C. P. Wong, *Member, IEEE*

***Abstract*—Flip chip on organic substrate has relied on underfill to redistribute the thermomechanical stress and to enhance the solder joint reliability. However, the conventional flip-chip underfill process involves multiple process steps and has become the bottleneck of the flip-chip process. The no-flow underfill is invented to simplify the flip-chip underfill process and to reduce the packaging cost. The no-flow underfill process requires the underfill to possess high curing latency to avoid gelation before solder reflow so to ensure the solder interconnect. Therefore, the temperature distribution of a no-flow flip-chip package during the solder reflow process is important for high assembly yield. This paper uses the finite-element method (FEM) to model the temperature distribution of a flip-chip no-flow underfill package during the solder reflow process. The kinetics of underfill curing is established using an autocatalytic reaction model obtained by DSC studies. Two approaches are developed in order to incorporate the curing kinetics of the underfill into the FEM model using iteration and a loop program. The temperature distribution across the package and across the underfill layer is studied. The effect of the presence of the underfill fillet and the influence of the chip dimension on the temperature difference in the underfill layer is discussed. The influence of the underfill curing kinetics on the modeling results is also evaluated.**

***Index Terms*—Curing kinetics, finite-element modeling, flip-chip, no-flow underfill.**

I. Introduction

As a result of rapid advances in the integrated circuit (IC) fabrication and the growing market for faster, lighter, smaller, yet less-expensive electronic products, flip chip has drawn tremendous attention as a first-level interconnect technique. Flip chip on organic substrates has faced the challenge of the thermomechanical stress generated by the coefficient of thermal expansion (CTE) mismatch between the silicon chip and the organic substrate. The use of underfill is necessary to redistribute the thermomechanical stress and to enhance the solder joint reliability [1]. However, the conventional flip-chip underfill process involves multiple process steps including fluxing dispensing, chip placement, solder reflow, flux cleaning, underfill capillary flow, and underfill curing, which is time and cost consuming. With increasing input–output (I/O) count and decreasing gap distance, flux cleaning and underfill dispensing has become the bottleneck of the flip-chip process. As a solution to these problems, the no-flow underfill was invented and developed [2], [3]. The no-flow underfill process eliminates the need for flux, avoids capillary dispensing of underfill, and combines solder reflow and underfill curing into one step. It greatly improves the efficiency of flip-chip assembly and has been studied and evaluated in industry [4], [5].

The nature of the no-flow underfill process requires that the underfill have enough reaction latency to maintain its low viscosity until the solder joints are formed. Otherwise, gelled underfill would prevent the melting solders from collapsing onto the contact pads, resulting in low yield of the solder joint. The unique curing process of the no-flow underfill has provoked research in underfill curing during the reflow process. Curing kinetic modes as well as in situ viscosity measurements have been developed to predict the evolution of degree of cure (DOC) and the gelation behavior of a no-flow underfill during the solder reflow process [6]–[8]. In these kinetic modelings, the board temperature measured during the reflow process was used as the underfill temperature. However, in a practical situation, the underfill lies in the small gap between the chip and the substrate and is reflowed in a dynamic process in the reflow oven. The temperature of the underfill is affected by the conduction heating from the board and the chip, as well as the exothermic reaction of the underfill curing, and the phase transition of the solder melting and solidification. In the case of a large chip on board, there can be temperature distribution across the underfill layer, which leads to a difference in DOC of the underfill. The previous underfill curing models did not consider the temperature distribution, neither the exothermic effect of the curing reaction. Hence, there is a need to understand the temperature distribution of a flip-chip package with no-flow underfill during the solder reflow process.

Despite the wide application of flip-chip packages, there has been little research in the temperature distribution of a flip-chip package during the solder reflow process. In the case of flip-chip no-flow underfill, the material property of the underfill in the reflow process is also curing-dependent. The curing-dependent modeling of the polymeric material has aroused interest in recent years. Dunne *et al.* developed an integrated process modeling for sequential multilayer substrate fabrication using a coupled cure-thermal-stress analysis in ABAQUS [9]. In the area of curing-dependent underfill modeling, Yang *et al.* performed a stress analysis in a conventional flip-chip packaging

Manuscript received December 12, 2003; revised April 6, 2004.

Z. Zhang and C. P. Wong are with the School of Materials Science and Engineering and Packaging Research Center, Georgia Institute of Technology, Atlanta, GA 30332 USA (e-mail: cp.wong@mse.gatech.edu).

S. K. Sitaraman is with the The George W. Woodruff School of Mechanical Engineering, Georgia Institute of Technology, Atlanta, GA 30332 USA.

Digital Object Identifier 10.1109/TEPM.2004.830505

[10], [11]. However, the temperature profile a no-flow underfill experiences is drastically different from that for a conventional underfill. Hence, there is a need to understand the effect of underfill curing on a flip-chip no-flow underfill package.

In this paper, the temperature distribution of a flip-chip no-flow underfill package during the solder reflow process is modeled using the finite-element method (FEM) in ANSYS. The main objective of this paper is to understand the temperature profile the underfill experiences during the solder reflow process considering the geometry of the flip-chip package and the thermal events that happen during the process, including the phase transition of the solder material and the exothermic underfill curing reaction. The model will also evaluate the effect of the underfill fillet and the size of the chip on the temperature distribution of the underfill layer.

II. FEM Model

A. Governing Equation

The problem can be summarized as a three-dimensional (3-D) transient heat transfer analysis. The general equation for 3-D heat conduction can be expressed as [12]

$$\frac{\partial}{\partial x}k\left(\frac{\partial T}{\partial x}\right)+\frac{\partial}{\partial y}k\left(\frac{\partial T}{\partial y}\right)+\frac{\partial}{\partial z}k\left(\frac{\partial T}{\partial z}\right)+q_i=\rho c\frac{\partial T}{\partial t} \quad (1)$$

where k is the thermal conductivity of the material ($(W/m\cdot K)$, or $(mW/mm\cdot K)$); ρ is the density of the material (kg/m^3, or g/mm^3); c is the specific heat ($(J/kg\cdot K)$, or $(mJ/g\cdot K)$); and q_i is the volumetric rate of heat generation (W/m^3, or mW/mm^3). The convective heat transfer from the oven to the material is also considered

$$q_0=hA(T_0-T_f) \quad (2)$$

where q_0 is the heat transferred, T_f is the fluid temperature; T_0 is the surface temperature; A is the surface area; and h is the thin-film coefficient ($(W/m^2\cdot K)$, or $(mW/mm^2\cdot K)$).

B. Geometry

Two different geometric models are developed and compared in this study. A simplified flip-chip geometry (Model 1) is shown in Fig. 1, containing three layers, i.e., the chip, the underfill including the solder joints, and the FR-4 board. The chip size is 6.340×6.340 mm; the thickness of the chip, the underfill and the FR-4 board are 0.600, 0.075, and 0.850 mm, respectively. The 56 solder joints are distributed around the periphery of the die. For modeling purpose, the solder joints are assumed to be rectangular blocks; and the dimension of the solder block is $0.125\times 0.125\times 0.075$ mm. The distance between the center of the solder joint and the edge of the chip is 0.200 mm, whereas the distance between the centers of two solder joints is 0.400 mm. As is shown in Fig. 1, the chip lies in the x-y plane. Due to the symmetry of the chip-substrate assembly, only one fourth of the geometry is modeled. Heat flux on the symmetric planes is set to zero. Model 1 does not consider the underfill fillet to simplify the geometry. However, the fillet contains a large proportion of the underfill, especially in small dies. Hence, in Model 2, underfill fillet is considered. The height of the fillet is assumed to be 1/3 of the chip thickness and the angle of the fillet is 45°. Fig. 2 shows the 1/4; geometry of Model 2 with the underfill fillet. Model 2 is also used to study the effect of the chip dimension on the temperature distribution.

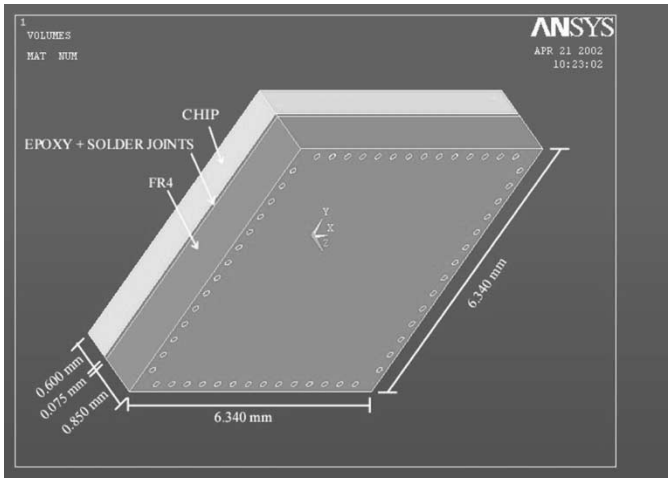

Fig. 1. Full geometry of Model 1 without the underfill fillet.

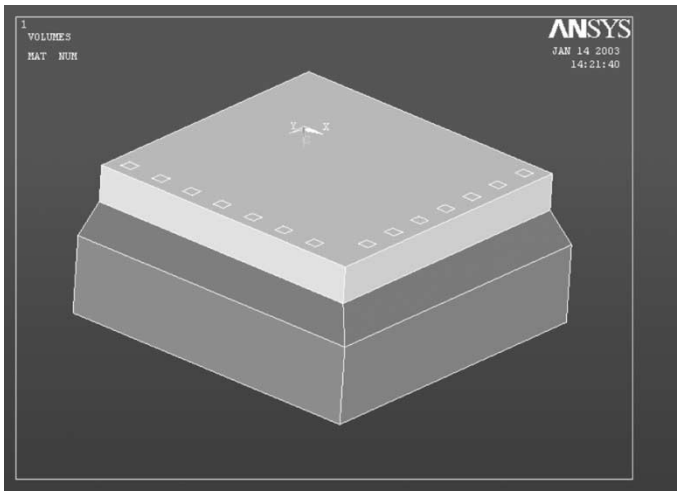

Fig. 2. The one-fourth geometry of Model 2 with the underfill fillet.

C. Material Property

There are four materials involved in this structure including silicon (the chip), eutectic SnPb (63/17) solder (solder joint), epoxy (underfill), and glass reinforced epoxy laminate (FR-4 board). Their material properties are listed in Table I. The thermophysical properties of silicon are presented as functions of temperature [13]–[16]. The specific heat of the SnPb solder is presented as a constant, independent of temperature. The solder melting point is 456 K; the latent heat of melting is 45.4 J/g and is presented as a step change in enthalpy as shown in Fig. 3. In order to study the effect of solder phase transition on the temperature distribution of the flip-chip package, a model without the solder phase transition was solved for comparison, in which the enthalpy of the SnPb solder changes linearly with temperature and the slope is the specific heat of the solder.

The thermophysical properties of epoxy present the most difficulty since they are not only functions of temperature but

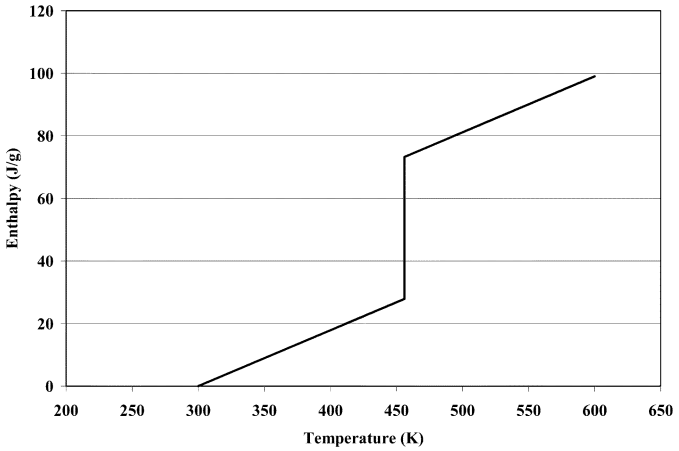

Fig. 3. Enthalpy of SnPb (63/37) solder as a function of temperature.

also functions of curing degree. The uniqueness of no-flow underfill lies in the simultaneous process of solder reflow and underfill cure. In the curing process, the small molecules of epoxy resin and hardener react with each other to form a 3-D network. The material undergoes the conversion from a viscous liquid to an elastic solid, and hence its physical properties change with increasing curing degree. In the reflow process, the material properties change with the DOC and with the temperature. Also, the DOC of epoxy is dependent on the temperature and the duration of exposure at a particular temperature. This dependency relates to the kinetics of curing reaction and is unique to a specific material system. It is very difficult to incorporate a temperature and curing dependent property in the ANSYS program. In this paper, the thermal conductivity of the epoxy resin is assumed to be constant and is equal to 0.30 $\mathrm{W/m{*}K}$. This simplification will nevertheless bring errors in the modeling result. The specific heat of the epoxy is 2400 $\mathrm{J/Kg*K}$ [17]. Constant thermophysical properties of FR-4 are assumed and are listed in Table I [18].

D. Loading Conditions

The board temperature and the air temperature are measured by thermocouples mounted on a PWB in the reflow process. These two temperatures can be used as the boundary condition of the model. Fig. 4 shows the air temperature in the reflow oven and the board temperature during the reflow process. In the current analysis, the time period that the package is in the reflow oven (240 seconds) is divided into 120 time intervals. Hence, including the initial condition, altogether 121 loading steps are applied in the transient analysis.

In order to apply air convection boundary condition, the thin film coefficient of the air on silicon surface is calculated as a forced convention of laminar flow on flat plates. All the properties (density, viscosity, specific heat, and thermal conductivity) of the air are functions of temperature. Table II contains the calculation results of the thin film coefficient of nitrogen in the reflow oven, assuming the flow rate is 1 m/s and the length is the chip dimension (6.34 mm) [19]. The calculated thin film coefficient as a function of temperature is shown in Table II.

TABLE I
THERMOPHYSICAL DATA OF THE MATERIALS IN THIS PAPER

Materials	Temperature (K)	Thermal Conductivity (W/m*K)	Specific Heat (J/Kg*K)	Density (g/mm^3)
Silicon	300	148	705	2.333e-3
	350	119	757.7	
	400	98.9	788.3	
	500	76.2	830.7	
	600	61.9	859.9	
SnPb (63/37) solder	312.2	49.3	178.74	8.34e-3
	375.2	47.1		
	412.2	46.7		
	509.2	23.1		
	583.2	25.5		
	693.2	29.7		
Epoxy	-	0.30	2400	1.2e-3
FR-4 board	-	0.30	1000	1.5e-3

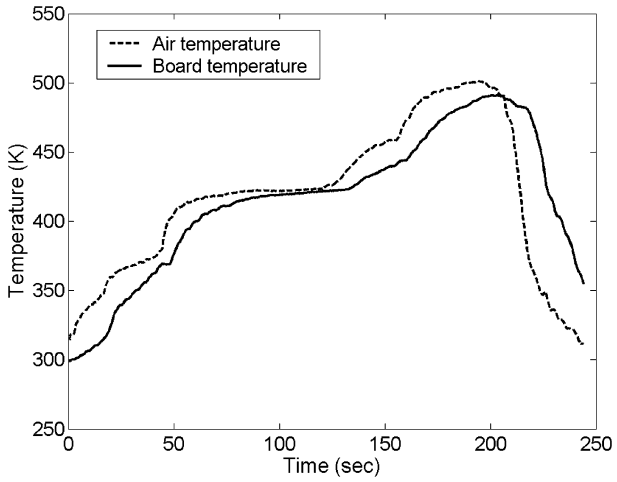

Fig. 4. Air and board temperatures in a reflow process.

III. INCORPORATION OF CURING KINETICS INTO THE FEM MODELING

The curing reaction of epoxy resin is time and temperature dependent. Usually it can be described by an autocatalytic model:

$$\frac{d\alpha}{dt} = K\alpha^m(\alpha_{\max} - \alpha)^n \tag{3}$$

where K is the rate constant; α is the DOC; $\alpha_{\max}$ is the maximum DOC; m and n are orders of the reaction. The parameter K, $\alpha_{\max}$, m, and n are all modeled as functions of the temperature. At low reaction temperatures, due to the vitrification effect, the curing reaction cannot be completed and the maximum DOC is limited to $\alpha_{\max}$, which is dependent on the reaction temperature. At high reaction temperature, the reaction can be completed and $\alpha_{\max}$ equals to 1. K is related to the temperature according to the Arrhenius equation:

$$K = A\exp\left(-\frac{E}{RT}\right) \tag{4}$$

where A is the frequency factor and E is the activation energy.

A typical no-flow underfill, Underfill A, was used in this study to demonstrate the incorporation of curing kinetics into the FEM modeling. In order to find the kinetic model parameters, Differential Scanning Calorimeter (DSC, by TA Instruments, Model 2920) was used to characterize the curing properties

TABLE II
CALCULATION RESULT OF THIN FILM COEFFICIENT

Temperature (K)	300	400	500	600
Density (Kg/m^3)	1.12	0.84	0.672	0.56
Specific heat (J/Kg*K)	1042	1042	1057	1075
Viscosity (Pa*s)	1.80e-5	2.22e-5	2.61e-5	2.95e-5
Thermal conductivity (W/m*K)	2.58e-2	3.23e-2	3.85e-2	4.45e-2
Reynolds number	394	240	163	120
Prandtl number	0.728	0.717	0.717	0.713
Nusselt number	11.9	9.20	7.59	6.51
Thin film coefficient (W/m^{2}K)	48.3	46.9	46.1	45.7

of the underfill. Both isothermal and constant heating rate experiments were conducted. The isothermal curing experiments were carried out at 110, 120, 130, 140, 150, 160, 170, and 180°C, respectively. For each isothermal temperature, the experimental data were fitted to (3) and the kinetic parameters K, $\alpha_{\max}$, m, and n were obtained. Then the parameters $\alpha_{\max}$, m, and n were fitted as polynomials of the temperature and the Arrhenius relation was established for the reaction rate K. The details of the curing kinetics modeling can be found elsewhere [20]. The results for the temperature-dependent kinetic parameters for the underfill curing are summarized below:

$$n = 2.258 \times 10^{-5} T^2 - 0.013\,70T + 2.716$$
$$m = 1.649 \times 10^{-4} T^2 - 0.1324T + 26.80$$
$$\alpha_{\max} = -4.893^{-5} T^2 + 0.042\,66T - 8.279$$
$$\text{when } T < 423.15 \text{ K}$$
$$\alpha_{\max} = 1 \text{ when } T \geq 423.15 \text{ K}$$
$$\ln K = \left(-\frac{1.079}{T} + 0.002\,005 \right) \times 10^4.$$

In order to compare the model with the experimental results, DSC constant heating rate experiments were conducted from room temperature to 300°C at 3, 5, 10, 15, and 20°C/min, respectively. The DOC of the underfill as a function of temperature was calculated from the DSC data and is presented as "experiment" curves in Fig. 5. From the developed model, the DOC of underfill at each heating rate can also be calculated and is presented as "model" curves in the same figure. The results displayed good agreement of the model with the experimental data.

In order to incorporate the curing kinetic model into the FEM model, the exothermic heat flow from the underfill curing reaction needs to be calculated by (5). If the temperature of the epoxy over time is known, the generated heat flow over time can be calculated. However, in order to obtain the temperature profile of the epoxy, the generated heat flow from the curing reaction needs to be known as the loading condition. Hence, the nodal solutions and the loading conditions are inter-dependent, which makes the incorporation of the curing kinetics difficult in the FEM model.

$$\frac{dH}{dt} = \Delta H_{\text{total}} \times \frac{d\alpha}{dt}. \tag{5}$$

Two approaches were developed in order to incorporate the curing kinetics into the FEM model. The first approach used iteration, where in the first iteration the board temperature was used as the temperature profile that the epoxy experienced in a reflow process. Using this temperature profile, the DOC and the exothermic heat of curing was calculated separately; and this heat was applied as the heat-generation loading condition. Using the exothermic heat on top of the board temperature profile, the temperature distribution in the underfill was computed in the second iteration. Using this revised underfill temperature distribution, the progression of DOC and the exothermic heat generation was determined. This heat load was re-applied on top of the board temperature profile in the 3rd iteration. This sequence of steps was repeated until the underfill temperature profile at specific points converged between two adjacent iterations. The results, in fact, converged after three iterations.

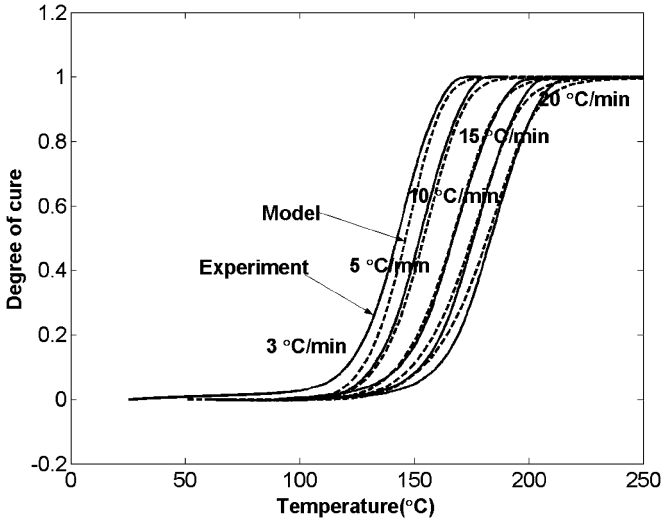

Fig. 5. Comparison of the model and experiment data in constant heating rate DSC.

The second approach used a computing loop in the ANSYS software. As was mentioned, the total time period in the transient analysis was divided into 121 steps. At the first load step when the board and the air temperatures are close to room temperature, it is assumed that there was no heat generated from the epoxy curing reaction. After the first loading step was applied, the solution was obtained. Using the underfill nodal solution, the DOC and heat flux can be calculated and was applied in the next loading step. Then the model was solved as a continuation of the previous solution. The result of the underfill temperature in the previous time step was used in the next time step. Same procedure was applied to the rest 120 time steps in the analysis.

The results of the modeling showed that the difference in the two solutions is indiscernible. Therefore, the loop approach is favored in terms of computational time since the model

only needs to be solved once whereas in the iteration approach, multiple computations are needed in order to obtain the convergence.

IV. Results and Discussion

A. Effect of Thermal Events

Solder Phase Transition: The effect of the solder phase transition on the temperature of the underfill was evaluated in Model 1 using different solder material properties. The step change in enthalpy of the solder as shown in Fig. 3 was used in the model to consider the phase transition and the solution was compared to the model that did not consider the solder phase transition. The temperature profile of one underfill node that is close to the solder joint was taken out for comparison to see the maximum effect from the solder phase transition. It turned out that the difference in the underfill temperature at the solder melting point and solidification point is less than 0.2°C. It can be concluded that the effect of the solder phase transition on the temperature distribution of the flip-chip package during the solder reflow process is negligible due to two facts. First, the latent heat of phase transition is relatively low (45 J/g). Second, the solder volume is very small compared to the whole structure.

Underfill Curing: Compared with the solder phase transition, the reaction heat of the underfill curing is much higher (320 J/g). The volume of the underfill is also much higher than the solder in the model. Hence the temperature of the underfill from the center node is plotted and compared in Model 1 with and without the underfill curing exotherm in Fig. 6. The results of the model suggested that with the exothermic effect from the underfill curing, the peak temperature of the underfill can be increased by 3°C.

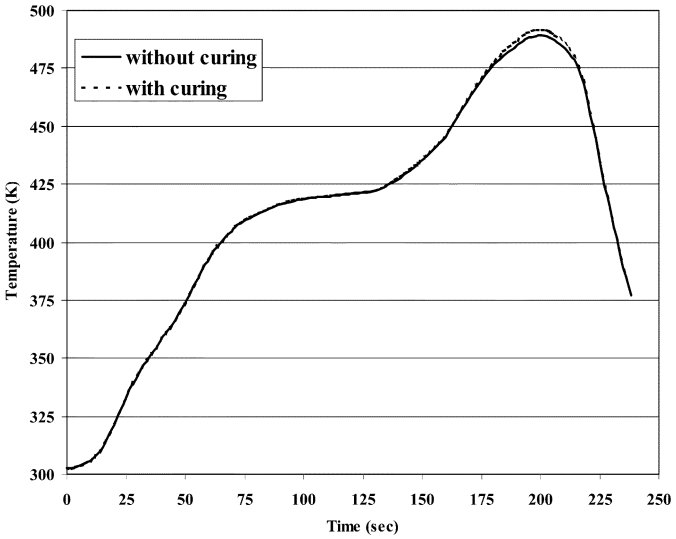

Fig. 6. Comparison of the underfill temperature with or without curing exotherm.

B. Temperature Distribution of the Flip-Chip Package During Solder Reflow Process

To observe the temperature difference between the chip, the underfill and the board during the reflow process, 10 nodes were selected, which lie in the center of the geometry with the same x and y coordinates but a different z coordinate. It was found that the vertical temperature gradient in the chip area was minimal since the thermal conductivity of silicon is high. In the epoxy layer, a vertical temperature gradient was also not very obvious because of the thin thickness. The biggest vertical temperature gradient existed in the board layer since the FR-4 board was thick and low in thermal conductivity. The nodal solutions in the epoxy layer were averaged and plotted together with the boundary conditions in Fig. 7. It can be observed from the figure that the board temperature was higher than other parts of the package in most instances during the reflow process since the conductive heating from the board was more efficient than the convective heating from the air. At the soaking zone, uniform temperature distribution was reached. At the reflow zone, the temperature of the underfill and the chip started to exceed that of the board due to the exothermic curing reaction of the epoxy. The temperature of the underfill remained higher than the board in the cooling zone as well. Throughout the reflow process, it can be concluded that the temperature of the underfill was much closer to the board boundary condition than to the air boundary condition. Therefore as a rough approximation, the board temperature can be taken as the underfill temperature.

The temperature distribution of the epoxy layer during the solder reflow process is of great interest, since the temperature which the underfill experiences directly relates to the DOC of the underfill, and hence, the material properties of the underfill, and therefore the reliability of the package. Fig. 8 illustrates the temperature distribution in the epoxy layer in a reflow process. It is noticed that in most instances, the temperature of the underfill at the edge was higher than that at the center, since the edge of the chip was exposed to more convective heat flux from the oven. With the increase in reaction rate, the temperature in the center started to exceed that at the corners. Overall, the temperature difference across the underfill layer was around 1°C, which did not make a significant difference in DOC of the underfill across the assembly area.

C. Effect of the Underfill Fillet and the Chip Size

Although the previous modeling results indicated that the temperature difference across the underfill layer was not significant, Model 1 did not include the underfill fillet, while in the actual flip-chip package the underfill fillet constitutes a large proportion of the underfill volume. Hence in Model 2, the fillet was included in the model. The air convection boundary condition was applied on the underfill fillet. Two nodes in the underfill layer were chosen for comparison; one at the center of the chip (symmetric point) and the other at the fillet corner. The difference between these two nodal solutions is plotted throughout the reflow process in Fig. 9. As can be seen in the plot, the temperature difference across the underfill layer in Model 2, where fillet was present, was almost three times the difference in Model 1 where fillet was absent. Due to the low thermal conductivity of the epoxy, the surface temperature of the underfill fillet was close to the air temperature and there was a larger temperature gradient in the underfill fillet part. Therefore, in a flip-chip model, the underfill fillet cannot be neglected.

In order to study the effect of chip dimension on the temperature distribution, the size of the chip in Model 2 was doubled

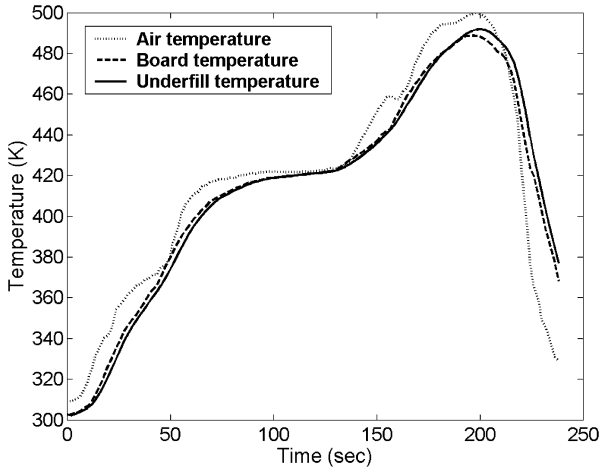

Fig. 7. Underfill temperature during reflow process.

with the presence of the underfill fillet. The nodal solutions at the same locations were again compared and the temperature difference between these two nodes is plotted in the Fig. 9. The increase in the die size did increase the temperature difference in the underfill. However, the effect was not as significant as that from the underfill fillet. The results were reasonable since the underfill layer was mainly heated by the substrate throughout the reflow process. Air convection only influenced the temperature gradient in the underfill fillet, but did not cause a significant temperature difference in the package. Therefore, the increase in die size will not influence the temperature distribution greatly.

D. Effect of Curing Kinetics

The previous study has shown that curing kinetics of Underfill A was successfully incorporated into the FEM modeling of the temperature distribution of a flip-chip no-flow underfill package in a reflow process. The results indicated that the underfill curing did not introduce significant temperature difference in the package. However, the solution from the FEM model might depend on the underfill curing kinetics. An underfill with a different curing kinetics, Underfill L, was investigated to study the effect of curing kinetics on the temperature distribution. Fig. 10 shows DSC heat flow diagrams of the two underfills, Underfill A and Underfill L, at a heating rate of $5^{\circ}\mathrm{C}/\min$. As can be seen from the figure, Underfill L has a very sharp curing peak and a higher latent heat of curing reaction compared to Underfill A. The isothermal curing behavior of Underfill L was evaluated at 140, 145, 150, and 155°C, and suitable kinetic model was developed with the following parameters:

$$\frac{d\alpha}{dt} = (k_1 + k_2\alpha^m)(1-\alpha)^n$$
$$m = -0.001\,28T + 1.197,$$
$$n = 0.008\,24T - 1.9404,$$
$$\ln k_1 = -\frac{9050.8}{T} + 13.701,$$
$$\ln k_2 = -\frac{9691.4}{T} + 17.021.$$

The curing kinetics was incorporated into the ANASYS model in the case of a small die with fillet. The board temperature, underfill temperature and the heat flow from underfill

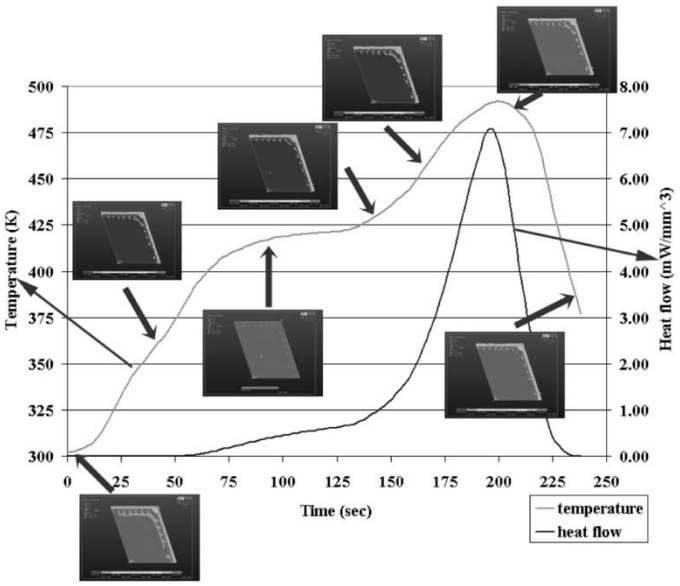

Fig. 8. Temperature distribution in the underfill layer during the reflow process.

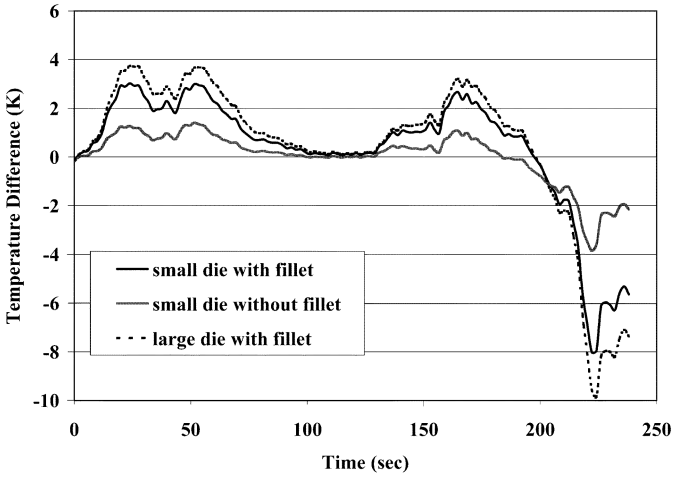

Fig. 9. Temperature difference in the underfill in different models.

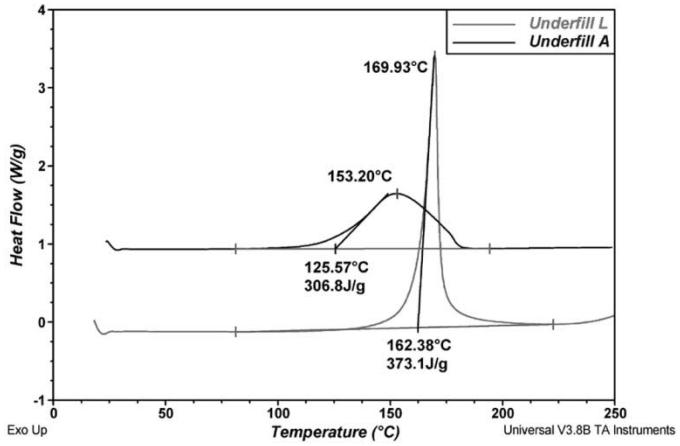

Fig. 10. DSC curing profile of the two underfills at a heating rate of $5^{\circ}\mathrm{C}/\min$.

curing during the reflow process are plotted in Fig. 11. Compared with the previous results from Underfill A, no significant difference was observed as to the temperature distribution.

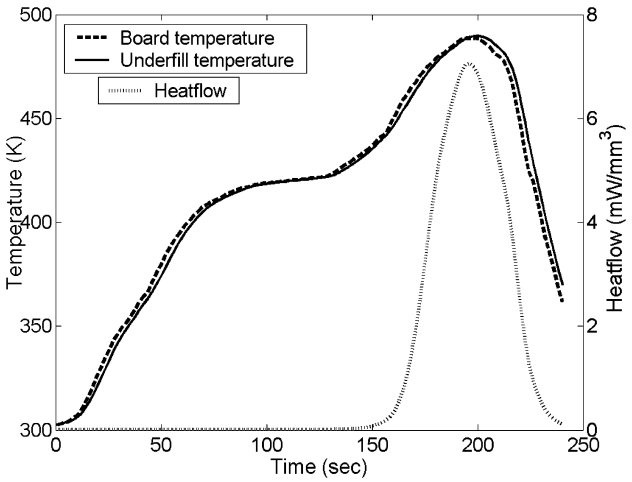

Fig. 11. Board temperature and underfill temperature during reflow with Underfill L.

Although the heat flow diagram of Underfill L at a heating rate of $5°\mathrm{C}/\mathrm{min}$ appeared to be very different from that of Underfill A, the heat flow diagram during the reflow process was similar to that of Underfill A as can be observed from a comparison between Figs. 8 and 11. The main reason for this similarity is that the curing behaviors of the no-flow underfills are designed to be compatible with the reflow condition, i.e., minimal DOC before the solder melting and maximum DOC after the reflow process. Therefore, the majority of the heat flow occurred around the peak temperature of the reflow profile. Although the curing kinetics of the two underfills were quite different from each other, the heat generation rates from underfill curing during the same reflow process were similar to each other due to the unique curing requirement of the no-flow underfill. As a result, the influences of the underfill curing on the temperature distribution of the flip-chip package were similar for these two underfills.

V. Conclusion

No-flow underfill significantly simplifies the flip-chip underfill process and reduces the packaging cost. To study the temperature distribution of the flip-chip no-flow underfill package during a solder reflow process, a 3-D transient thermal analysis model was developed using FEM in ANSYS. There were two major thermal events during the solder reflow process: the solder phase transition and the underfill curing. The effect of the solder phase transition was found to be negligible on the temperature of the package due to the small solder volume and the low latent heat. The curing kinetics of the no-flow underfill was developed based on the DSC isothermal curing data. The developed kinetic model of underfill curing was incorporated into the model using two methods: the iteration approach and the loop approach. These two approaches yielded very close solutions, which indicated that the exothermic epoxy curing reaction can raised the underfill temperature by $3\ °\mathrm{C}$ at the maximum curing rate. The solution from the FEM model suggested that the underfill temperature was close to that of the board during the solder reflow process. The temperature distribution across the underfill layer was not significant. However, the presence of underfill fillet increased the temperature difference in the underfill layer by three times. By doubling the dimension of the chip, the temperature difference in the underfill layer increased about 25%. The effect of different underfill curing kinetics on the modeling results was also evaluated. It was found that due to the unique curing process of no-flow underfill, the heat flow generated from the underfill during the solder reflow process was similar regardless of the difference in curing kinetics. Therefore, the temperature distribution of the flip-chip package was not significantly changed with a different no-flow underfill.

References

[1] Y. Tsukada, "Surface laminar circuit and flip-chip attach packaging," in *Proc. 42nd Electronic Components and Technology Conf.*, 1992, pp. 22–22.
[2] R. Pennisi and M. Papageorge, "Adhesive and encapsulant material with fluxing properties," U.S. Patent 5 128 746, 1992.
[3] C. P. Wong and S. H. Shi, "No-flow underfill of epoxy resin, anhydride, fluxing agent and surfactant," U.S. Patent 6 180 696, 2001.
[4] D. Gamota and C. M. Melton, "The development of reflowable materials systems to integrate the reflow and underfill dispensing processes for DCA/FCOB assembly," *IEEE Trans. Comp., Packag., Manufact. Technol. C*, vol. 20, pp. 183–183, 1997.
[5] C. P. Wong, S. H. Shi, and G. Jefferson, "High performance no-flow underfills for flip-chip applications: Material characterization," *IEEE Trans. Comp., Packag., Manufact. Technol. A*, vol. 21, pp. 450–450, 1998.
[6] Z. Zhang and C. P. Wong, "Study and modeling of the curing behavior of no-flow underfill," in *Conf. Proc. 8th Int. Symp. Exhibition on Advanced Packaging Materials Processes, Properties and Interfaces*, 2002, pp. 194–200.
[7] J. M. Hurley, T. Berfield, S. Ye, R. W. Johnson, R. Zhao, and G. Tian, "Kinetic modeling of no-flow underfill cure and its relationship to solder wetting and voiding," in *Proc. 52nd IEEE Electronic Components and Technology Conf. 2002*, 2002, pp. 828–833.
[8] P. Morganelli and B. Wheelock, "Viscosity of a no-flow underfill during reflow and its relationship to solder wetting," in *Proc. 51st Electronic Components and Technology Conf.*, 2001, pp. 163–166.
[9] R. C. Dunne and S. K. Sitaraman, "An integrated process modeling methodology and module for sequential multilayered substrate fabrication using a coupled cure-thermal-stress analysis approach," *IEEE Trans. Electron. Packag. Manufact.*, vol. 25, pp. 326–334, 2002.
[10] D. G. Yang, G. Q. Zhang, L. J. Ernst, J. F. J. Caers, H. J. L. Bressers, and J. Janssen, "Combined experimental and numerical investigation on flip chip solder fatigue with cure-dependent underfill properties," in *Proc. 51st Electronic Components and Technologies Conf.*, Orlando, FL, 2001, pp. 919–924.
[11] D. G. Yang, G. Q. Zhang, W. van driel, J. Hanssen, H. J. L. Bressers, and L. J. Ernst, "Parameter sensitive study of cure-dependent underfill properties on flip chip failures," in *Proc. 52nd Electronic Components and Technologies Conf.*, San Diego, CA, 2002, pp. 865–872.
[12] A. D. Kraus and A. Bar-Cohen, *Thermal Analysis and Control of Electronic Equipment*. Bristol, PA: Hemisphere, 1983.
[13] C. L. Yaws, *Handbook of Thermal Conductivity*. Houston, TX: Gulf, 1995, vol. 4.
[14] *CRC Handbook of Thermophysical and Thermochemical Data*, 80th ed., D. R. Lide, Ed., CRC, Boca Raton, FL, 1999.
[15] Y. S. Touloukian *et al.*, *Thermophysical Properties of Matter, Vol. 1, Thermal Conductivity: Metallic Elements and Alloy*. West Lafayette, IN: Purdue Univ., Thermophysical Properties Research Center, 1970.
[16] [Online]. Available: http://www.efunda.com
[17] G. Lubin, *Handbook of Composites*. New York: Van Nostrand Reinhold, 1982.
[18] R. R. Tummala, Ed., *Fundamentals of Microsystems Packaging: Ch6. Fundamentals of Thermal Management*. New York: McGraw-Hill, 2001.
[19] H. Wolf, *Heat Transfer*. New York: Harper Row, 1983.
[20] Z. Zhang and C. P. Wong, "Modeling of the curing kinetics of no-flow underfill in flip-chip applications," *IEEE Trans. Comp. Packag. Technol.*, vol. 27, pp. 383–390, June 2004.

Zhuqing Zhang (M'02) received the B.S. degree from Fudan University, Shanghai, China, in 1997, and the M.S. and Ph.D. degrees from the Georgia Institute of Technology (Georgia Tech), Atlanta, in 2001 and 2003, respectively.

She is currently a Postdoctoral Fellow with the School of Materials Science and Engineering, Georgia Tech.

Dr. Zhang was awarded the 10th Annual Motorola-IEEE/CPMT Society Graduate Student Fellowship for Research in Electronic Packaging for her paper "Double-Layer No-Flow Underfill Materials and Process" at the 52nd Electronic Components and Technology Conference held in San Diego, CA, in 2002. Her Ph.D. thesis was granted the Sigma Xi outstanding Ph.D. Thesis Award from Georgia Tech in 2004.

Suresh K. Sitaraman received the Ph.D. degree in mechanical engineering from the Ohio State University, Columbus, the M.A.Sc. in mechanical engineering from the University of Ottawa, ON, Canada, and the B.Eng. in mechanical engineering from the University of Madras, India.

He is currently with the George W. Woodruff School of Mechanical Engineering at Georgia Tech. Prior to joining Georgia Tech in 1995, he was with IBM Corp. His expertise is in the area of thermo-mechanical design, modeling, reliability, and new technologies for microelectronic systems. He guides a group of post-doctoral, doctoral, master's, and undergraduate students and has published extensively in journals and conferences. He leads the Reliability Thrust at the Packaging Research Center and directs the Computer-Aided Simulation of Packaging Reliability (CASPaR) Laboratory.

Dr. Sitaraman's co-authored papers have won the best paper award from the IEEE TRANSACTIONS ON COMPONENTS AND PACKAGING TECHNOLOGIES in 2000 and 2001. He received the Metro-Atlanta Engineer of the Year in Education Award in 1999, Outstanding Faculty Education Award from the Packaging Research Center in 1998, and the NSF-CAREER Award in 1997. He serves as an Associate Editor for the IEEE Transactions on Advanced Packaging. Dr. Sitaraman is an ASME Fellow.

C. P. Wong (SM'87–F'92) received the B.S. degree in chemistry from Purdue University, West Lafayette, IN, and the Ph.D. degree in organic/inorganic chemistry from Pennsylvania State University, University Park.

After his doctoral study, he was awarded two years as a Postdoctoral Scholar with Stanford University, Stanford, CA. He joined AT&T Bell Laboratories in 1977 as a Member of Technical Staff. He was elected an AT&T Bell Laboratories Fellow in 1992. He is a Regents Professor with the School of Materials Science and Engineering and a Research Director at the NSF-funded Packaging Research Center, Georgia Institute of Technology (Georgia Tech), Atlanta. He holds more than 40 U.S. patents, numerous international patents, and has published more than 400 technical papers and 400 keynotes and presentations in the related area. His research interests lie in the fields of polymeric materials, high Tc ceramics, materials reaction mechanism, IC encapsulation, in particular, hermetic equivalent plastic packaging, electronic manufacturing packaging processes, interfacial adhesions, PWB, SMT assembly, and components reliability.

Dr. Wong received the AT&T Bell Laboratories Distinguished Technical Staff Award in 1987, the AT&T Bell Fellow Award in 1992, the IEEE Components, Packaging and Manufacturing Technology (CPMT) Society Outstanding and Best Paper Awards in 1990, 1991, 1994, 1996, 1998, and 2002, the IEEE Technical Activities Board Distinguished Award in 1994, 1995 IEEE CPMT Society's Outstanding Sustained Technical Contribution Award, the 1999 Georgia Tech's Outstanding Faculty Research Program Development Award, the 1999 NSF-Packaging Research Center Faculty of the Year Award, the 1999 Georgia Tech Sigma Xi Faculty Best Research Paper Award, and the University Press (London, U.K.) Award of Excellence. He was elected a member of the National Academy of Engineering in 2000. He served as the Technical Vice President (1990 and 1991) and President (1992 and 1993) of the IEEE CPMT Society.