SOLUTION OF RELAY AND SWITCHING CIRCUITS BY SYMBOLIC ANALYSIS

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SOLUTION OF RELAY AND SWITCHING CIRCUITS BY SYMBOLIC ANALYSIS

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DEFINITION OF SYMBOLS USED

\(cX\) Complement or negative of the class \(X\).
\(f(Z)\) Function of an impedance.
\(X\) Group of contacts, or simply a class.
\(X_a\) Dependent or relay operated contact, or the relay coil itself.
\(X_a(T)\) Time delay relay coil.
\(X_a(t+p)\) Contact of a time delay relay with a delay of \(p\) seconds.
\(X_1\) Independent or manually operated contact, or a subclass of the class \(X\).
\(Z_{a}\) Impedance of the dependent contact \(X_a\).
\(Z_{ab}\) Impedance between the points \(a\) and \(b\).
\(Z_a(t+p)\) Impedance of a time delay relay contact.
\(Z_1\) Impedance of an \(X_1\) contact.
\(Z'_1\) Inverse of \(Z_1\), or the admittance of the \(X_1\) contact.
\(<\) Contained in.
\(>\) Contains.
\(\Lambda\) Null class.
\(O\) Impedance of a closed contact or circuit.
\(\infty\) Impedance of an open contact or circuit.
SOLUTION OF RELAY AND SWITCHING
CIRCUITS BY SYMBOLIC ANALYSIS

INTRODUCTION

Problems involving complicated systems of relays and switches are encountered frequently in all those phases of industry which employ electric control circuits and protective relay systems. Thus, the subject of relays and switches presents a field for much endeavor. In spite of this fact very little material has been written about relay and switching systems. There are several good references on protective relay networks with applications to power systems. Two of these are Relay Systems by Monseth and Robinson\(^1\) and Relays and Electromagnets by Jones\(^2\). Although these two references give an excellent treatment of protective relay systems, nothing is mentioned about control circuits which are becoming more important every day.

Claude E. Shannon\(^3\) has introduced a method of solving


\(^2\)B. W. Jones and I. C. S. Staff, Relays and Electromagnets (Scranton, Pa.: International Textbook Company, 1935).

relay and switching problems which uses the principles of symbolic logic. This study can be applied to both control and protective circuits. The present analysis is restricted to electrical systems.

The same method can also be applied to efficiency studies when there are systems of two alternatives to be chosen. Examples of this are railway dispatching, fuel piping, etc. It is well to know that these problems can be solved by the methods presented in the following analysis.

This analysis follows the lines of the paper written by Shannon, but a different approach will be used to arrive at similar conclusions. The method of attack employed by Shannon may be briefly described as follows: Any circuit may be represented by a set of equations, the terms of the equations corresponding to the various relays and switches in the circuit. A true circuit is a closed electrical path which usually includes a source of emf and a useful load device. In the present discussion the source and load will be tacitly assumed and the word circuit used to describe the remainder of the system. An algebra is developed for manipulating these equations by simple mathematical processes, most of which are similar to ordinary algebraic algorithms. This algebra is shown to be exactly analogous to the principles of the calculus of classes used in the study of symbolic logic.

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It should be noted that no resistors or other circuit elements other than relay coils and contacts are included in this study.

Symbolic logic is a subject that is unfamiliar to most persons in industry. Ordinary direct current circuit theory is, therefore, used as an approach to this analysis. Although a modified form of symbolic logic will be used in the later sections, no previous study of the subject is necessary in order to follow this analysis.

The first section will be devoted entirely to a study of the simplifications in the theory of simple electrical circuits which result from the assumption that a circuit impedance may have only two values, zero or infinity. A relationship between these simplified equations and symbolic logic will be introduced, and an algebra will be developed that will make the simplification of complicated circuits easier. Synthesis of networks will be discussed with particular attention devoted to the symmetric function circuit. As a final check, experiments were made in the laboratory to determine the precautions that should be observed in applying the theory to an actual problem.

In its present form, this analysis does not hold for many special relays such as polar relays, time delay relays, ratchet relays, and other specially constructed relays and switches. Likewise, this analysis does not hold for combinations of constant-current and constant-voltage relay oper-
ations in the same circuit. It is hoped in the future that this type of analysis can be extended to cover all these applications.
This study of relays and switches involves a closed or open contact treatment. We will consider that at any given time the contacts are either open or closed, and in view of this condition, the circuit between any two terminals must have either an infinite impedance or a zero impedance. In some cases a time delay may be involved, but in the ultimate analysis the previous statement is still valid.

The symbols and definitions will be explained as they are encountered. The first symbol to be used is $Z$. $Z$ will represent the impedance between two points. If the two points are lettered $a$ and $b$, then the expression for the impedance between the two points may be written as $Z_{ab}$. The representation of the contacts of a simple relay or switch is shown in Figure 1.

![Fig. 1. Representation of relay or switch contacts.](image)

$X_1$ and $X_2$ are notations for the contacts in the circuits.

It is known from direct current circuit analysis that the impedance of an open circuit is infinity, while the impedance of a closed circuit is zero. This statement is of course idealized, but it is adequately accurate for the pre-
sent purpose. Throughout this thesis the following definitions will be used:

1. An open circuit has an infinite impedance.
2. A closed circuit has a zero impedance.

It should be noted that zero and infinity as used here will not lead to indeterminate forms as they do in the calculus.

**Simple Series-Parallel Circuits**

If two impedances are connected in series, the total impedance is the sum of the two individual impedances. An open circuit in series with a closed circuit is known to be an open circuit since there is no closed path. This is represented in Figure 2 and shown by algebra in Equation 1.

![Simple series circuit](image)

\[ Z_{ab} = Z_1 + Z_2 = \infty + 0 = \infty \] (1)

The general equation for any number of contacts in series is given by Equation 2.

\[ Z_{ab} = Z_1 + Z_2 + Z_3 + Z_4 + Z_5 + \ldots + Z_n \] (2)

Equation 2 shows that for any number of contacts in series an
open circuit results if any one of the contacts is open.

It is also known from direct current circuit theory that if two or more parallel paths exist a solution can be obtained by using either admittances or impedances. The solution using admittances is analogous to the solution of the series circuit and will be given first.

An admittance, $Y$, will be defined as the reciprocal of an impedance, $Z$. A prime notation will be used to distinguish the impedance of a contact from its admittance. In other words, if $Z$ is the contact impedance, $Z'$ is the contact admittance. Figure 3 is a simple two element parallel circuit, and the solution in terms of the circuit admittance is given in Equation 3.

\[ Y_{ab} = Z'_1 + Z'_2 \]  \( (3) \)

Equation 3 states that the admittance between the points a and b is the sum of the admittance of the parallel contacts. Anytime that one of the contacts is closed the admittance of
the circuit will be infinite and the circuit will be closed as shown in Equation 4.

\[ Y_{ab} = 0 + \infty = \infty \]  
\[ Z_{ab} = \frac{1}{Y_{ab}} = \frac{1}{\infty} = 0 \]  

(4a)  
(4b)

The solution given in Equation 4 is for the simple circuit of Figure 3. The general equation for the impedance of any parallel circuit in terms of the admittance is given in Equation 5. This equation is derived from the fact that the impedance of the circuit is equal to the reciprocal of the admittance, while the admittance is the sum of all the individual parallel contact admittances.

\[ Z_{mn} = \frac{1}{Z_1 + Z_2 + Z_3 + \ldots + Z_n} \]  

(5)

Equation 5 shows for the general case that the impedance is zero if one of the contacts has an infinite admittance or in other words is closed.

The problem of parallel circuits shown in Figure 3 can be solved by the standard impedance method given in Equation 6.

\[ Z_{ab} = \frac{Z_1 Z_2}{Z_1 + Z_2} \]  

(6)

Since \( Z_1 \) in this figure is infinite, the solution appears to be indeterminate. Assume that \( Z_1 \) is finite, divide both numerator and denominator by this term, and then take the limit of this expression as \( Z_1 \) approaches infinity. These operations
lead to Equation 7.

$$Z_{ab} = \frac{Z_2}{Z_1 \rightarrow \infty} \frac{Z_2}{Z_1 + 1} = \frac{0}{0 + 1} = 0$$  \hspace{1cm} (7)

The general solution can also be treated by this same method. The general equation for the impedance of a parallel circuit with n elements is given in Equation 8.

$$Z_{mn} = \frac{Z_1 Z_2 Z_3 \ldots Z_n}{Z_2 Z_3 \ldots Z_n + Z_1 Z_3 \ldots Z_{n+1} + \ldots Z_1 Z_2 \ldots Z_{n-1}}$$  \hspace{1cm} (8)

In order to solve this equation it is necessary to divide both numerator and denominator by all the terms which are infinite. It will be noted from this equation that the circuit will be closed if any one of the contacts is closed.

This method is more cumbersome than the admittance method, but it is necessary to use this approach in order to arrive at the simplifications which relate these solutions to the analogous methods of symbolic logic.

**Fundamental Simplifications**

This section is a study of symbolic analysis and its purpose is to shorten the solutions of problems. It is, therefore, legitimate to state certain assumptions that at first do not appear true or useful. Thus far, this analysis is the same as that for any other simple circuit and has not been simplified by our first assumption that the circuit can have only two values of impedance. Really, we have mathematically
verified what is physically obvious. We have already solved the parallel circuit and determined the impedance equation as given in Equation 8. It has been proved by both the admittance and impedance methods that a closed circuit exists if any contact is closed.

We will now proceed with the problem and see what simplifications can be made. There are three possible conditions that can exist in the circuit. These are as follows:

1. All contacts are closed.
2. All contacts are open.
3. Some contacts are open; the rest are closed.

For the present we are interested in only the third condition when only one contact is closed. We will assume that all the other possible conditions under item 3 will have the same solution as this example. This is a plausible assumption since we have proved that a closed circuit exists if only one or any number of contacts are closed in a parallel circuit. Under the conditions chosen, the denominator of Equation 8 will be infinite for any contact that is selected to be closed, because the denominator is formed by sums of all possible products of the circuit elements with one element excluded in each product. We then have Equation 8 reduced to Equation 9.

\[
Z_{mn} = \frac{0}{\infty} = 0
\]

This identity is true since both infinite terms approach in-
finity at the same rate. The proof can be justified in several ways, all of which lead to the same conclusions. It appears that the denominator of Equation 9 has no effect on the solution of the identity and that the impedance of a parallel circuit can be found by forming a product of the elements involved. We will make the two following definitions:

1. The product of zero and infinity will be defined as zero.

2. The impedance of several contacts in parallel can be found by forming a product of all the contact impedances. It will also be noted that zero divided by zero and zero multiplied by zero will be defined as zero.

Inspection of the circuit when the first and second conditions are applied, show that these definitions are still valid. This can be proved by substituting the actual contact values in Equation 8 and simplifying by use of the definitions made.

From this previous circuit analysis it is obvious that the following postulates are true. It should be remembered that these postulates are mere statements of physical facts that are commonly known to exist.

1a. A closed contact in parallel with a closed contact is a closed circuit.

\[ Z = 0 \cdot 0 = 0 \]

1b. An open contact in series with an open contact
is an open circuit.

\[ Z = \infty + \infty = \infty \]

2a. An open contact in parallel with a closed contact is a closed circuit.

\[ Z = 0 \cdot \infty = 0 \]

2b. An open contact in series with a closed contact is an open circuit.

\[ Z = 0 + \infty = \infty \]

3a. A closed contact in series with a closed contact is a closed circuit.

\[ Z = 0 + 0 = 0 \]

3b. An open contact in parallel with an open contact is an open circuit.

\[ Z = \infty \cdot \infty = \infty \]

These postulates are arranged in pairs which are the inverse of each other. The inverse of zero is infinity, and the inverse of addition in this case is defined as multiplication. These postulates are called the inverse of each other, because they read alike if the word open is replaced with closed and if the word series is replaced with parallel.
Multi-Terminal and Non-Series-Parallel Circuits

Many relay and switching circuits are not of the simple series-parallel type. The analysis of a multi-terminal circuit can often be simplified by transforming the circuit into an equivalent series-parallel form. This transformation is accomplished by using the standard star-mesh conversions.

Whenever three paths form a three-cornered mesh, it is possible to convert this circuit into a three-cornered star\(^1\). This means that the two circuits will offer identical impedances between any pair of terminals. In this special case, the transformation will be referred to as the delta-wye conversion.

![Delta-wye conversion](image)

The equations given below show the transformations of Figure 4, with the usual restriction that all impedances are either zero or infinite.

---

These equations are similar to Equation 9 for the parallel circuit in which the denominator can be neglected; hence, by inspection it can be seen that the denominators of the above equations can be neglected, and the equations are simplified as shown. The final form can be justified by the fact that if \( Z_{ab} \) is zero; then \( Z_1 \) and \( Z_2 \) must be zero, etc. In the delta to wye transformation the equivalent leg of the wye is found by forming a product of the two delta branches adjacent to it when the figures are superimposed on one another.

The inverse transformation from wye to delta is given in the following equations.

\[
Z_{ab} = \frac{Z_1 Z_2 + Z_2 Z_3 + Z_3 Z_1}{Z_3} \quad (13)
\]

\[
Z_{bc} = \frac{Z_1 Z_2 + Z_2 Z_3 + Z_3 Z_1}{Z_1} \quad (14)
\]

\[
Z_{ac} = \frac{Z_1 Z_2 + Z_2 Z_3 + Z_3 Z_1}{Z_2} \quad (15)
\]

None of our previous work helps in simplifying these equa-
tions. Therefore, we must proceed directly. The first step in simplifying these equations is to divide the denominator into the numerator giving Equation 16.

\[ Z_{ab} = Z_1 + Z_2 + \frac{Z_1 Z_2}{Z_3} \]  

(16)

Examination of the last term leads to the conclusion that it adds nothing to the first two terms; therefore, the first two terms are complete in describing the impedance between a and b. This can be proved inductively by substituting any combination of zeros and infinities for the impedance terms in Equation 16. In the next section an equation will be developed which shows conclusively that this is true. Therefore, the expression for the impedance of an equivalent delta branch is equal to the sum of the impedances of the two adjacent legs of the wye. Using the same notation as given in Figure 4, we may write the following set of equations.

\[ Z_{ab} = Z_1 + Z_2 \]  

(17)

\[ Z_{bc} = Z_2 + Z_3 \]  

(18)

\[ Z_{ac} = Z_1 + Z_3 \]  

(19)

These transformations are valid for admittance terms as well as impedance terms. If this is done the admittance equations of the delta to wye conversion will be analogous to the impedance equations of the wye to delta transformation,
while the admittance equations of the wye to delta conversion will be analogous to the impedance equations of the delta to wye transformation.

The expressions just derived are special cases of the general star-mesh theorem. A great amount of work has been done by Rosen\(^2\) on this topic, and his theorem states: A star of \(n\) legs may always be replaced by a mesh of \(\frac{1}{2}n(n-1)\) branches joining every pair of points without affecting the rest of the network. In order to do this the mesh system must be symmetrical; that is, there must be a total of \(\frac{1}{2}n(n-1)\) branches if the original star contains \(n\) legs. Figure 5 is the diagram of a five point star converted to a five point mesh, and Equation 20 is the general equation as derived by Rosen.

\[
Z_{ab} = Z_1 Z_2 \left( \frac{1}{Z_1} + \frac{1}{Z_2} + \frac{1}{Z_3} + \frac{1}{Z_4} + \cdots + \frac{1}{Z_n} \right)
\]

Simplifying this equation we get Equation 21.

\[ Z_{ab} = Z_1 + Z_2 + \frac{Z_1 Z_2}{Z_3} + \frac{Z_1 Z_2}{Z_4} + \ldots + \frac{Z_1 Z_2}{Z_n} \]  (21)

This equation is similar to Equation 16 in which the term containing \( Z_1 \) and \( Z_2 \) divided by a \( Z_3 \) added nothing to the solution. This is also the case here, and it can be proved by substituting values in the equation as in Equation 16; therefore, the impedance is given in Equation 22.

\[ Z_{ab} = Z_1 + Z_2 \]  (22)

These solutions, like the previous one for the special three terminal circuit, can be made by using admittances instead of impedances.

It will be observed that since, in general, the number of mesh contacts is greater than the number of terminals, the theorem is not reciprocal; i.e., no mesh in which the members are arbitrarily chosen can be converted into a star. The delta to wye transformation is a special case of the general theorem. In the three cornered mesh there are the same number of contacts in both networks so this transformation holds for both.

Since the mesh to star transformation does not hold except in special cases and the star to mesh increases the number of switch contacts, these equations are not used to any great extent. The star to mesh transformation is useful when it is necessary to eliminate the center point.
To this point our approach has been from the ordinary circuit viewpoint. The next section will deal with the fundamental relations of symbolic logic and the correlation between these ideas and the expressions already formulated from the circuit theory.
BASIC CONCEPTS

**Fundamental Relations of Symbolic Logic**

The first serious student of logic was Leibnitz, though he recognized others as preceding him in this field. The signally important contribution in the 19th Century was that of the mathematician George Boole; but this was preceded by, and in part resulted from, a renewed interest in logic by Sir William Hamilton and Augustus De Morgan. A history of the development of this type of logic can be found in the literature\(^1\).

There are many relations which exist in the study of symbolic logic that are not useful in this analysis; consequently, these will not be discussed. The proofs for the expressions given here will not be reviewed, because these can be found in any book on symbolic logic\(^2\). The symbols and notations will be altered to conform with the work done in previous sections of this thesis. The following paragraphs present the ideas to be used.

Symbolic logic is a study of classes. We shall define \(X\) as a class and \(X_1, X_2, \ldots, X_n\) as subclasses of \(X\). This may


\(^2\)Lewis and Langford, op. cit.
be written symbolically as:

\[ X_1, X_2, \ldots, X_n \subset X \]  

(23)

or

\[ X \supset X_1, X_2, \ldots, X_n \]  

(24)

\( X_1 + X_2 \) shall be defined as the class which contains all the elements in either \( X_1 \) and/or \( X_2 \).

\( X_1 X_2 \) shall be defined as the class which contains all the elements which are common to \( X_1 \) and \( X_2 \). This is commonly called the intersection of \( X_1 \) and \( X_2 \).

\( \Lambda \) is the null class. This is the class that has no elements of \( X \).

The complement of the subclass \( X_1 \) shall be defined as all the elements in \( X \) which are not contained in \( X_1 \). This will be referred to as the negative of \( X_1 \) and will be written as \( cX_1 \). There are several other ways of representing this process, but they will not be needed for this analysis.\(^3\)

The negative of the null class is the class \( X \). In the follow-

analysis we shall use \( X_1 \) to denote any well defined subclass of \( cX_1 \).

The following propositions hold for all terms of the system:\(^4\)

\[ \text{Ibid.}, \ p. \ 28 \]

\[ \text{Cohen and Nagel, op. cit.}, \ pp. \ 123-126 \]
1. \( X_1 X_1 = X_1 \)

This means that the intersection of the class \( X_1 \) with itself is still the class \( X_1 \). Since this is true there are no exponents in this algebra.

2. \( X_1 X_2 = X_2 X_1 \)

The intersection of \( X_1 \) and \( X_2 \) is the same as the intersection of \( X_2 \) and \( X_1 \).

3. \( X_1 (X_2 X_3) = (X_1 X_2) X_3 \)

The intersection of \( X_1 \) and the intersection of \( X_2 \) and \( X_3 \) is the same as the intersection of \( X_3 \) and the intersection of \( X_1 \) and \( X_2 \). Since this law holds, the parenthesis can be omitted.

4. \( X \bot = \bot \)

The intersection of \( X \) and the null class is the null class.

5. \( X_1 \bot = X_1 \)

The intersection of the subclass \( X_1 \) and the whole class \( X \) is the subclass \( X_1 \).

6. \( X_1 + \bot = X_1 \)

\( X_1 \) is the class that contains all the elements of \( X_1 \) and the null class.
7. \[ X_1 + X = X \]

The class \( X \) contains itself and all its subclasses. There are several other principles used in symbolic logic that are useful in this analysis.\(^5\) These are:

1. The principle of contradiction: \( X \cap \overline{X} = \varnothing \)

   The intersection of a class and its negative is the null class. The intersection of a class and any subclass of its negative is also the null class, \( X \cap X' = \varnothing \).

2. The principle of the excluded middle: \( X + \overline{X} = X \)

   Every element in the class \( X \) is either a member of the subclass \( X \) or a member of the negative of the subclass \( X \).

3. The principle of absorption: \( X \cap X' = X \) or \( X(X + X') = X \)

   The class \( X \) contains all the elements common to the class \( X' \) and the intersection of that class with the class \( X \).

4. The principle of tautology: \( X + X = X \)

These definitions, propositions, and principles are not all that are included in the study of symbolic logic, but they will be sufficient for the present work.

The foregoing ideas are the basic principles of symbolic logic. It will be noted that the processes used in symbolic logic are similar to the impedance operations performed in the series and parallel circuit simplifications in

\(^5\)Ibid.
the first sections of this thesis. A proof that these operations are identical will be sufficient to permit the application of the principles of symbolic logic in the solution of circuit impedance equations.

First, the main distinction will be made between the algebra of classes and the method used in solving impedance equations. In the latter case numbers are used, while equations involving classes use only symbols.

We shall imagine a class $X$ as containing all the elements in any circuit to be simplified. Some of the elements will be related to other elements by an inverse nature. In other words, these inverse elements are a subdivision of the of the complementary class of the original element. The inverse element is related to the original element in that its impedance is always opposite in value. If $X_1$ is the original element and has an impedance of zero, $X^i_1$ is its inverse and has an impedance of infinity. All elements, other than inverse elements, may be assigned either a zero or an infinite impedance at random. Each of the elements in the whole class $X$ forms a basic class which can not be subdivided further.

We shall assume a general series-parallel circuit as shown in Figure 6. To prove that the impedances of these contacts behave like classes, we will divide them up into groups. Each contact or group of contacts that can be separated into a series component will be denoted as a subclass. Thus $X_1$, $X_m$, $X_n$, and the group of contacts on the
left are subclasses. If any of these series groups contain more than one contact, they can be further divided into groups of parallel paths. The path \( X_e, X_f, \) and \( X_g \) will be a subdivision of the left series subclass. This process is continued until the circuit is separated into many subclasses composed of basic classes.

\[ \text{Fig. 6. General series-parallel circuit.} \]

In order to find the impedance between \( a \) and \( b \) we will operate on the contacts as classes. It is observed that the operations involved in both cases are equivalent. The contact impedances that are in series will be treated as the sums of classes. The contact impedances that are in parallel will be treated as the intersection of classes. Writing the equation between \( a \) and \( b \) according to classes but in terms of impedances, we have a result similar to those found in the first section of this thesis. Since we have considered these impedances as classes they can be simplified according to the rules of symbolic logic. It should be remembered that certain basic classes have an inverse relationship with other basic
classes in the circuit. Since this is true a great many of the simplifications can be made by the use of the principles of the excluded middle, contradiction, and absorption.

Keeping the relationship between contact impedances and classes in mind, we see by the above explanation that the solution by the straight impedance method and the class method are identical. From this point on, we shall solve all impedance equations by the principles of symbolic logic.

Circuit Simplification Theorems

Many theorems and equations that are used in the study of symbolic logic will be useful to us in the procedure of simplifying certain networks. It should be remembered in simplifying the equations that will be handled here, the commutative, associative, and distributive laws of algebra still hold.

Four principles that were listed previously in the section on symbolic logic will now be written in the form of impedance equations.

1. The principle of contradiction: \( Z_1 Z_1' = 0 \)
   The impedance of two inverse contacts in parallel is zero.

2. The principle of the excluded middle: \( Z_1 + Z_1' = \infty \)
   The impedance of two inverse contacts in series is infinite.

3. The principle of absorption: \( Z_1 + Z_1 Z_2 = Z_1 \)
The impedance of an $X_1$ contact in series with a parallel system involving an $X_1$ contact is equivalent to the impedance of the $X_1$ contact.

4. The principle of tautology: $Z_1 + Z_1 = Z_1$

The impedance of several identical contacts in series is equivalent to the impedance of one of the contacts. These four principles will be useful not only in the simplification of equations, but also they are the basis of some of the theorems to follow. The third principle will be expanded into a more general case which will prove to be one of the handiest instruments in this analysis.

De Morgan's Theorem- This theorem makes it possible to perform the inverse of a sum or a product by transferring the inverse to the simple terms as follows: The inverse of a sum is the product of the inverse of its summands; the inverse of a product is the sum of the inverse of its factors. Stated in terms of equations:

\[
(Z_1 + Z_2)' = Z_1'Z_2' \tag{25}
\]

\[
(Z_1Z_2)' = Z_1' + Z_2' \tag{26}
\]

\[
(Z_1' + Z_2')' = Z_1Z_2 \tag{27}
\]

\[
(Z_1'Z_2')' = Z_1 + Z_2 \tag{28}
\]

In order to prove these equations we will first find the inverse of the expression $(Z_1 + Z_2)$. By virtue of the principle
of the excluded middle, \( Z_1 + Z_1' = \infty \) and \( Z_2 + Z_2' = \infty \), and the fact that \( \infty \infty = \infty \), we have:

\[
(Z_1 + Z_1')(Z_2 + Z_2') = \infty
\]  

(28)

Applying the distributive and associative laws, we may write:

\[
(Z_1Z_2 + Z_1Z_2' + Z_1'Z_2) + Z_1Z_2' = \infty
\]  

(29)

Consider now the two expressions \( (Z_1Z_2 + Z_1Z_2' + Z_1'Z_2) \) and \( Z_1'Z_2 \). Applying the principle of tautology, which in substance states that \( Z_1Z_2 + Z_1Z_2 = Z_1Z_2 \), we arrive at Equation 30.

\[
Z_1Z_2 + Z_1Z_2' + Z_1Z_2 = Z_1Z_2 + Z_1Z_2' + Z_1'Z_2 + Z_1Z_2
\]  

(30)

Examination of Equation 29 shows that \( Z_1'Z_2 \) is the inverse of \( (Z_1Z_2 + Z_1Z_2' + Z_1'Z_2) \). Substituting this fact in Equation 30 and factoring:

\[
\left[ Z_1(z_2 + z_2') + z_2'(z_1 + z_1') \right]' = z_1'z_2
\]  

(31)

By use of the fact that \( Z_1 + Z_1' = \infty \) and \( Z_2 + Z_2' = \infty \) and \( Z_1\infty = Z_1 \), we have proved Equation 25.

\[
(Z_1 + Z_2)' = Z_1'Z_2
\]  

(25)

By an identical argument Equation 26 can be proved. Equations 27 and 28 are merely the reciprocals of Equations 25 and 26. This same method used to prove Equation 25 can be used to prove that De Morgan's equation holds for any number of terms.
In the analysis of the parallel circuit we see from Equation 5 that the impedance is the reciprocal of the sum of the admittances of the parallel contacts. The discussion on page 9 leads to the conclusion that the impedance of a parallel circuit can be found by forming a product of all the parallel contact impedances. Writing the equation for the relationship between impedances and admittances in a parallel circuit, we have:

\[ Z_1Z_2Z_3Z_4...Z_n = (Z_1^* + Z_2^* + Z_3^* + Z_4^* + ...Z_n^*)' \quad (32) \]

This equation is recognized as the general form of Equation 27. If it were necessary, a proof could now be given, using De Morgan's theorem, to show that the impedance of a parallel circuit can be found by forming a product of the individual contact impedances. Since this step has already been justified once, another proof will not be given.

Development Theorems

It is often helpful in simplifying a problem to limit the number of times a contact appears in the circuit. This can be done if a function is developed with respect to the variable in question. A function of certain variables \( Z_1, Z_2, ..., Z_n \) is any expression formed by the operations of addition, multiplication, and inversion. Inversion is defined as an analogous operation to negation in symbolic logic, and when using impedances it is the same as taking the reciprocal.
We shall represent a function of these variables by the symbol $f(Z_1, Z_2, \ldots, Z_n)$.

This definition being established, we will proceed with the simple case, the development of $f(Z_1)$ with respect to $Z_1$. The development of this function is similar to the solution of a differential equation in that a solution must be assumed. There are two possible forms that this development might have. Since both will be useful they are listed as follows, where $u$ and $v$ are also functions of the variable:

\begin{align*}
  f(Z_1) & = uZ_1 + vZ_1' \\
  f(Z_1) & = (u + Z_1)(v + Z_1')
\end{align*}

Substituting $Z_1 = \infty$ and consequently $Z_1' = 0$ in Equation 33a, we have $f(\infty) = u$; then letting $Z_1 = 0$ and $Z_1' = \infty$, we have $f(0) = v$. With the coefficients $u$ and $v$ determined, we may write Equation 33a as follows:

\[ f(Z_1) = Z_1 f(\infty) + Z_1' f(0) \] (34a)

Making the same substitutions in Equation 33b for $Z_1$ and $Z_1'$, we find that $u = f(0)$ and $v = f(\infty)$. Substituting these values for $u$ and $v$ in Equation 33b we have Equation 34b.

---

Proceeding in a like manner, we will now develop a function of any number of variables with respect to $Z_1$. These general equations may be written:

\[ f(Z_1, Z_2, \ldots Z_n) = uZ_1 + vZ_1' \] (35a)

\[ f(Z_1, Z_2, \ldots Z_n) = (u + Z_1)(v + Z_1') \] (35b)

Again substituting values for $Z_1$ and $Z_1'$, we may write:

\[ f(Z_1, Z_2, \ldots Z_n) \]
\[ = Z_1 f(\infty, Z_2, \ldots Z_n) + Z_1' f(0, Z_2, \ldots Z_n) \] (36a)

\[ f(Z_1, Z_2, \ldots Z_n) \]
\[ = [Z_1 + f(0, Z_2, \ldots Z_n)] [ Z_1' + f(\infty, Z_2, \ldots Z_n) ] \] (36b)

Developing the function with respect to both $Z_1$ and $Z_2$ will lead, by a similar proof, to Equations 37a and 37b.

\[ f(Z_1, Z_2, \ldots Z_n) = Z_1 Z_2 f(\infty, \infty, Z_3, \ldots Z_n) \]
\[ + Z_1 Z_2' f(\infty, 0, Z_3, \ldots Z_n) \]
\[ + Z_1' Z_2 f(0, \infty, Z_3, \ldots Z_n) \]
\[ + Z_1' Z_2' f(0, 0, Z_3, \ldots Z_n) \] (37a)

and
\[
f(Z_1, Z_2, \ldots, Z_n) = [Z_1 + Z_2 + f(0, 0, Z_3, \ldots, Z_n)] \\
\cdot [Z_1 + Z_2 + f(0, \infty, Z_3, \ldots, Z_n)] \\
\cdot [Z_1' + Z_2' + f(\infty, 0, Z_3, \ldots, Z_n)] \\
\cdot [Z_1' + Z_2' + f(\infty, \infty, Z_3, \ldots, Z_n)] \\
(37b)
\]

Continuing this process for all the variables we will arrive at the complete development having the form:

\[
f(Z_1, Z_2, \ldots, Z_n) = Z_1 Z_2 \ldots Z_n f(\infty, \infty, \ldots, \infty) \\
+ Z_1' Z_2 \ldots Z_n f(0, \infty, \ldots, \infty) \\
+ \ldots + Z_1' Z_2' \ldots Z_n' f(0, 0, \ldots, 0) \tag{38a}
\]

and

\[
f(Z_1, Z_2, \ldots, Z_n) = [Z_1 + Z_2 + \ldots Z_n + f(0, 0, \ldots, 0)] \ldots \\
\cdot [Z_1' + Z_2' + \ldots Z_n' + f(\infty, \infty, \ldots, \infty)] \tag{38b}
\]

It was previously mentioned that these theorems can be used to limit the number of times that a contact appears in the circuit. If one contact is to be limited, it will be noted from Equation 36a and 36b that a development can be made with respect to the variable in question in such a way that the variable will appear at most twice, once as an open contact and once as a closed contact. If the function is developed
with respect to more than one of the contacts or variables, it will be noted that each variable will appear \(2^n\) times.\(^7\)

More equations that are useful can be obtained by merely multiplying Equations 36a and 36b by \(Z_1\) and \(Z_1'\). Performing these operations, the following four equations result:

\[
\begin{align*}
Z_1 f(Z_1, Z_2, \ldots, Z_n) &= Z_1 f(\infty, Z_2, \ldots, Z_n) \quad (39a) \\
Z_1' f(Z_1, Z_2, \ldots, Z_n) &= Z_1' f(0, Z_2, \ldots, Z_n) \quad (39b) \\
Z_1 + f(Z_1, Z_2, \ldots, Z_n) &= Z_1 + f(0, Z_2, \ldots, Z_n) \quad (39c) \\
Z_1' + f(Z_1, Z_2, \ldots, Z_n) &= Z_1' + f(\infty, Z_2, \ldots, Z_n) \quad (39d)
\end{align*}
\]

Equation 39c is the general statement of the principle of absorption. This equation also justifies the assumption that the last term of Equation 16 and all but the first two terms of Equation 21 can be neglected.

There are several other simplification equations that can be given.\(^8\) These involve the application of the theorems set forth in this section. The first of these is:

\[
(Z_1 + Z_2)(Z_1' + Z_3) = (Z_1 + Z_2)(Z_1' + Z_3)(Z_2 + Z_3) \quad (40)
\]

This identity can be verified by performing the indicated

\(^7\)Ibid., p. 28
\(^8\)Shannon, op. cit., p. 3
multiplications on each side and simplifying by using the principles of contradiction, absorption, and tautology. In carrying out this simplification the terms $Z_1Z_2Z_3$ and $Z_2Z_3$ will result. The term $Z_1Z_2Z_3$ can be disregarded by a form of the principle of absorption. This can be seen by considering the contacts $Z_2Z_3$ as one variable. Representing these two symbols by $Z$ and then applying the principle of absorption, we see that the term $Z_1Z_2Z_3$ can be left out. It would be well to note this situation since it will appear often in analyzing circuits.

The following identity is also very useful in this analysis:

$$Z_1Z_2 + Z_1'Z_3 = Z_1Z_2 + Z_1'Z_3 + Z_2Z_3 \quad (41)$$

If both sides of this identity are multiplied by $Z_1'$, the resulting equation will be: $Z_1'Z_3 = Z_1'Z_3 + Z_1'Z_2Z_3$. By the principle of absorption this reduces to $Z_1'Z_3 = Z_1'Z_3$.

These equations and theorems are not all the factors involved in simplifying circuits and circuit equations. Other methods will be encountered and will be discussed at a later time, but with these preliminary facts we can now proceed with the analysis with less difficulty.
SIMPLIFICATION OF COMPLEX NETWORKS

Non-Series-Parallel Forms

A representative circuit of this type is the simple bridge shown in Figure 7.

\[ X_1 \quad X_2 \quad X_3 \quad X_4 \quad X_5 \]

Fig. 7. Bridge circuit.

The conventional method of simplifying this circuit is to use a delta to wye transformation and reduce it to a simple series-parallel circuit. If this is done the circuit shown in Figure 8 results. By simplifying we do not necessarily mean a fewer number of contacts result. We mean a form in which the circuit can be studied to a better advantage. When a complex circuit is placed in a series-parallel form an equation can be written for the impedance between the two terminals.

\[ \frac{1}{X_1X_3} \]

Fig. 8. Series-parallel form of bridge.

Writing the equation for the impedance between a and b, we have the expression:
This equation is obtained by following the simple rules set down for writing impedance equations for simple series-parallel circuits. This resulting series-parallel circuit can be simplified by using the theorems and equations of the previous section. Performing the indicated operation of multiplication in Equation 42 we have:

\[ z_{ab} = z_1z_2 + (z_1z_3 + z_4)(z_2z_3 + z_5) \]  (42)

Using the principle of absorption and simplifying, we have:

\[ z_{ab} = z_1z_2 + z_1z_2z_3 + z_1z_3z_5 + z_2z_3z_4 + z_4z_5 \]  (43)

This final equation can be represented by Figure 9.

Shannon uses two other methods for simplifying this type of network. The first of these methods is to draw all possible paths between the points under consideration in the network. It is clear that the network impedance is zero if any one of these paths is closed. Hence, if the paths are

1Shannon, op. cit., p. 5
written as a product, each path will be a factor and the required result should be obtained. By all possible paths, we mean direct paths. Paths which double back and cross themselves need not be considered. Drawing all the possible paths in Figure 7, we have Figure 10.

![Figure 10. Bridge simplification.](image)

Writing the product of all the paths indicated in Figure 10, we have:

\[ Z_{ab} = (Z_1 + Z_4)(Z_2 + Z_3 + Z_4)(Z_2 + Z_5)(Z_1 + Z_3 + Z_5) \]  

(45)

Multiplying the first two terms together and the last two terms together:

\[ Z_{ab} = (Z_1Z_2 + Z_1Z_3 + Z_1Z_4 + Z_2Z_4 + Z_3Z_4 + Z_4) \]

(46)

\[ 
\times (Z_1Z_2 + Z_2Z_3 + Z_2Z_5 + Z_1Z_5 + Z_3Z_5 + Z_5) 
\]

Performing the multiplication and simplifying:

\[ Z_{ab} = Z_1Z_2 + Z_1Z_3Z_5 + Z_2Z_3Z_4 + Z_4Z_5 \]  

(47a)

\[ Z_{ab} = Z_1(Z_2 + Z_3Z_5) + Z_4(Z_5 + Z_2Z_3) \]  

(47b)

The results obtained by this method are identical to those
obtained by the standard transformation method.

The other method that Shannon used was to draw all possible lines which would break the circuit if the contacts along any one of the lines were open. The contacts along each line are then written as a product, with all these line products written as a sum. It is seen that the equation written in this form is a valid expression of the facts. If all the contacts are open along any one of the lines that are drawn, the impedance will be infinite as shown by Equation 48a and Figure 11. The equation and the figure also show that if at least one contact in each of the constructed lines is closed the circuit will be closed. Figure 11 is a modified form of Figure 7.

\[
Z_{ab} = Z_1Z_2 + Z_1Z_3Z_5 + Z_2Z_3Z_4 + Z_4Z_5 \quad (48a)
\]

\[
Z_{ab} = Z_1(Z_2 + Z_3Z_5) + Z_4(Z_5 + Z_2Z_3) \quad (48b)
\]

This method again leads to the same results that were obtained previously by the other two methods.

This third method is usually the most convenient and rapid, since it gives the result directly as a sum. However,
it is sometimes difficult to apply this method to a non-planar network, and one of the other two methods may be used with more ease.

**Complex Series-Parallel Networks**

The simplification of series-parallel networks has already been considered in the previous section, but in many applications the question arises as to whether the circuit given is in its simplest form: that is, are the fewest number of contacts and relays being used. The same methods that have been used can be applied here to determine if this condition exists. Frequently an equation representing a network or circuit may be written in several ways, each requiring the same minimum number of elements. In such a case, the form to be used may be chosen arbitrarily or from other factors involved.

As an example of a simplification we will consider the network shown in Figure 12 and expressed by Equation 49.

![Fig. 12. Series-parallel network.](image.png)
\[ Z_{ab} = Z_1 + Z_2^1(Z_1^1 + Z_2) + (Z_2 + Z_3)(Z_4)(Z_1^2 + Z_5) \]  

Performing all the operations indicated in Equation 49 and applying the principles of contradiction and absorption, this equation reduces to:

\[ Z_{ab} = Z_1 + Z_2^1Z_2 + Z_4Z_5(Z_2 + Z_3) \]  

Simplifying by using a modified form of Equation 39d we have:

\[ Z_{ab} = Z_1 + Z_2^1 + Z_4Z_5(Z_2 + Z_3) \]  

Applying Equation 39d again, the last term of Equation 51 becomes \( Z_4Z_5(\infty + Z_3) \), which is equal to \( Z_4Z_5 \). The final form is then:

\[ Z_{ab} = Z_1 + Z_2^1 + Z_4Z_5 \]  

This illustration is not a good engineering example, because \( X_3 \) was so interconnected to \( X_1 \) and \( X_2 \) that its presence made the system degenerate; i.e., the system is not as complicated as it appears. This example does show the typical procedure in minimizing the number of contacts in a series-parallel network. The final form of the network is shown in Figure 13.

Fig. 13. Simplification of Fig. 12.
Simplification of Network Equations

Up to this point the circuits and networks have involved contacts and switches that are operated by external relays, hand switches, and push buttons. The usual relay control circuit will involve not only these but also many internally operated contacts and switches. A circuit of this type will usually have the form of Figure 14.

\[ X_0 \quad X_1 \quad X_N \]

Fig. 14. Constant-voltage relay circuit.

N is a network of relay contacts and manually operated switches. The relay contacts can be ones that are either internally or externally operated. The following distinction will be made between internal or dependent contacts and external or independent contacts. An internal contact will depend upon other circuit conditions for its operation and will be noted by \( X_a, X_b, \ldots X_n \). The coils of these relays will also be lettered \( X_a, X_b, \ldots X_n \). The operation of independent contacts will depend only on external conditions and will carry the same notation as given previously; \( X_1, X_2, X_3 \).

The relay coil \( X_a \) in Figure 14 will be energized only if the impedance between 0 and \( X_a \) is zero: \( Z_{oa} = 0 \). Since
this relation is true, an equation can be written using the expression \( Z_{oa} \) to represent the impedance in series with the relay coil equated to the various contact impedances which control the operation of the relay.

![Fig. 15. Typical constant-voltage relay circuit.](image)

The equation for Figure 15 would be:

\[
Z_{oa} = Z_1 + Z_2 Z_a
\]  

(53)

The right hand members of equations of this type will be known functions involving the various dependent and independent element impedances; and given the starting or initial conditions and the values of the independent contact impedances, the dependent variables may be computed.

Suppose that a relay network is made up of several equations of a type similar to Equation 53. For example consider the set of equation as follows:

\[
\begin{align*}
Z_{oa} &= Z_1 + Z_2 + Z_3 Z_a \\
Z_{ob} &= Z_1 + Z_2 \\
Z_{oc} &= Z_1 + Z_2 + Z_3 Z_c \\
Z_{od} &= Z_1 + Z_2 + Z_4 Z_d
\end{align*}
\]  

(54a)
It will be noted that several of the elements appear in more than one equation, and therefore, there is reason to believe that a simplification can be made. The number of elements can be minimized quickly if the equations are arranged in the following order.

\[ Z_{oa} = Z_1 + Z_2 + Z_3Z_a \]

\[ Z_{oc} = Z_1 + Z_2 + Z_3Z_c \]

\[ Z_{ob} = Z_1 + Z_2 \]

\[ Z_{od} = Z_1 + Z_2 + Z_4Z_d \]

Representing these equations symbolically, we can use only one $Z_1$, one $Z_2$, and one $Z_3$ and draw a line after these terms to show that they are common to more than one equation. This sort of determinant form is illustrated for the above equations as follows:

\[
\begin{align*}
Z_{oa} &= Z_1 + Z_2 + Z_3Z_a \\
Z_{oc} &= Z_1 + Z_2 + Z_3Z_c \\
Z_{ob} &= Z_1 + Z_2 \\
Z_{od} &= Z_1 + Z_2 + Z_4Z_d
\end{align*}
\]

This symbolic representation shows the contact impedances in a position similar to the actual placement of the contacts in the circuit. When equations are given for a relay
control circuit it is very helpful to simplify them by this simultaneous equation method. The circuit for the equations given above is diagramed in Figure 16.

Sequential Relay Systems

In a circuit of this type the relays can operate only in a certain order or sequence. The operation of one relay prepares the circuit for the next to operate. If \( X_a \) precedes \( X_b \) in the sequence and both are constrained to remain operated until the sequence is finished, then we will have the basis for further simplifying equations. A circuit of this type is illustrated in Figure 17.

In this circuit the switch \( X_1 \) is normally open while the switch \( X_2 \) is normally closed. If push button \( X_1 \) is oper-
ated, \( X_a \) will operate thus operating \( X_b \). To make the relays inoperative the switch \( X_2 \) is opened. Since the relays are restricted to a certain mode of operation, we can state that \( Z_a Z'_b = 0 \), or \( Z_a Z'_b = 0 \). The following equations are also true:

\[
Z'_a Z'_b = Z'_a = Z'_b \quad (55)
\]
\[
Z_a Z'_b = Z_a = Z_b \quad (56)
\]
\[
Z'_a + Z'_b = \infty = Z_a + Z'_b \quad (57)
\]
\[
Z'_a + Z'_b = Z'_a = Z'_b \quad (58)
\]
\[
Z_a + Z'_b = Z_a = Z_b \quad (59)
\]

These equations can be proved in several ways. The easiest is to consider that in the ultimate analysis that \( Z_a = Z_b \) which is the case.

These equations will be helpful in analyzing sequential systems, but it must be remembered that these relations hold only if both relays remain operated until the circuit is de-energized. In many cases the operation of one relay may operate another relay, the first being de-energized after the second relay has been energized. The above equations might hold for brief intervals during the sequence but they could not be considered to hold rigorously. A circuit illustrating this type of relay control network is shown in Figure 18. In this circuit it is considered that the contacts are so constructed that the \( X_b \) contact closes before...
the \( X_0 \) contact opens. This can be reliably arranged by use of the so called make-break contactor.

Before the sequence is set into operation \( Z_a = Z_b \). After the relays have operated, \( Z_a = Z_b' \) before the push button \( X_2 \) is operated. No equations can be written that will hold throughout the entire time, but equations with time limits could be written to show the relations that exist during the different intervals of the operation.

Equations could also be developed similar to Equations 55 through 59 for the case in which \( X_b \) would be de-energized when \( X_a \) was energized; that is, \( Z_a = Z_b' \).

There are other circuits that have special uses that can be developed in a manner similar to the circuits given in this section. Circuits of this type will be helpful in solving problems which contain special difficulties.
Inverse Networks

The inverse of any network can be found by applying De Morgan's theorem, but the network must be transformed into an equivalent series-parallel circuit if it is not already in that form. Shannon has developed a method by which the inverse of any planar two-terminal network can be found directly.\(^1\) As an example of this method consider the network in Figure 19.

![Fig. 19. Planar two-terminal network.](image)

In order to find the inverse of this network the following procedure is used. For each path of Figure 19 assign a node or junction point. For each element separating the two nodes, say \(X_n\), there corresponds an element \(X'_n\) connecting the two nodes in the inverse circuit.\(^2\) With this general statement in mind the inverse of Figure 19 can be recognized in Figure 20.

\(^1\)Shannon, op. cit., p. 6
\(^2\)Ibid.
In the network of Figure 19 the paths c and d correspond to the nodes c and d in Figure 20.

If these two figures are the inverse of each other; then \( Z_{ab} = Z_{cd} \). In order to prove this let the network of Figure 20 be superimposed upon that of Figure 19, the nodes of one within the corresponding paths of the other and the corresponding elements crossing as shown in Figure 21.

Incidentally, this is the easiest method of finding the inverse of a simple network. Now if \( Z_{ab} = 0 \), then there must be a path from a to b in Figure 19 such that every contact along this path is closed. Any closed path that is chosen in Figure 19 from a to b will make it impossible to draw a closed path from c to d in Figure 20. Therefore, \( Z_{cd} = \infty \).
It also follows that if $Z_{cd} = 0$, then $Z_{ab} = \infty$. By analyzing these two circuits we have seen that they do meet the necessary conditions: $Z_{ab} = Z_{cd}'$.

In view of this transformation developed by Shannon, we can realize the inverse of any planar network with the same number of elements as the given network. This is true since the inverse of the original element appears only once in the inverse network.

The foregoing principle is analogous to the principle of potentially inverse networks given by Shea. In a network of this latter type all the series element are changed to parallel elements and vice versa. The elements in one network are the reciprocals of the elements in the inverse network. Sometimes it is easier to use Shea's method to find the inverse than it is to apply Shannon's procedure. In many complex networks neither of these two methods are applicable. Therefore, a few rules will be given in order that they may be followed in case the conversion can not be made by one of the before mentioned methods. Actually these are based on the previous methods but use a little different approach.

1. Select the two paths to be converted to nodes.
2. All the elements that are passed through when going through each path will have one connection to each node.

---

3. Elements that meet at a common junction in one network will form a closed series path in the inverse network.

4. Elements that form a closed series path in the original network will meet at a common point in the inverse network.

5. The elements that appear in the inverse network will be the inverse of the corresponding element in the original network.

As stated, these rules are obtained by study of the methods previously presented and are found to hold simply through experience in their use. These rules hold if they are applied to the simple transformation given in this section, but they will be applied to a more complicated system to show that they will hold again. Shannon states that the two following networks are the inverse of each other.

![Fig. 22. Inverse planar networks.](image)

We will demonstrate that we arrive at the same conclusions by
using the five rules set forth. In the first network of the
above figure we will use the two paths as shown. It is seen
that in passing through the d path \(X_1, X_2, X_3\), and \(X_c\) are en-
countered. According to Rule 2, the inverse of these elements
will be connected to the d node in diagram B. Traversing the
other path in diagram A, \(X_1, X_8\), and \(X_a\) are encountered. The
three inverse contacts corresponding to these elements will
be connected to the node c in diagram B. It will be noted
in the inverse network B that these two conditions exist.
In the first network the elements \(X_4, X_5, X_6, X_7\), and \(X_b\) form a
common junction point. In the inverse network these five ele-
ments form a closed series path. Upon checking all the ele-
ments of both the A and B circuits, we find that the inverse
transformation meets the requirements of the five rules.

**Constant-Voltage and Constant-Current Circuits**

The general constant-voltage system was shown in Figure
14. In this circuit all the relays are in parallel across
the line, and it is necessary to open the circuit in series
with the relay coil in order to open the relay. In the figure
below both the constant-voltage and the constant-current cir-
cuits are shown.

![Fig. 23. Constant-voltage and constant-current systems.](image-url)
In the constant-current system the relays are all in series. To de-energize a relay it is necessary to short circuit the relay coil. If the relay $X_a'$ in the constant-current circuit is to be operated when $X_a$ is operated, it is evident that the admittance in parallel with $X_a'$ must be the inverse of the impedance in series with $X_a$. Since the constant-voltage system and the constant-current are the inverse of each other, the above methods may be used to convert from one to the other. The two circuits of Figure 23 are typical of the constant-voltage and constant-current transformations. The relay coils of these circuits have a prime notation in the inverse circuit. Actually, these relays are the same as before, and the primes are used to show that they are in different circuits. They are the same since the same operation is obtained from the circuits in both cases; that is, in the first circuit the relay is not energized because it is in series with an open circuit. In the second circuit or the inverse circuit the relay is again inoperative, but it is because the relay is short circuited in this case. If the circuit had any dependent contacts, contacts that are dependent on the relay for their operation, they would have to appear as an inverse contact in the inverse circuit.

It should be pointed out that either the constant-voltage or the constant-current system can be used to solve a control problem by the methods presented in this analysis. Although many problems may have a solution
employing a combination of constant-voltage and constant-current relays, this analysis does not make any provisions for a solution of this kind.

Synthesis of the General Symmetric Function

In the section on circuit simplification it was seen that the number of elements required was increased when the simple bridge of Figure 7 was converted to a series-parallel circuit. This fact leads us to believe that a series-parallel circuit, even though it contains the fewest number of series-parallel elements, is not the simplest circuit possible. The transformation of the series-parallel circuit to a bridge or similar form is not nearly as easy as the reverse process. Probably the simplest method of securing this type of conversion would be to use a reverse type of the last method given in changing from a bridge circuit to a series-parallel circuit. This method was to draw lines breaking the circuit and then writing all of the terms as a sum. A reverse of this process would be difficult to apply; and since only special cases of series-parallel circuits can be simplified by use of non-series-parallel circuits, the symmetric function circuit which appears in many relay systems will be introduced.

A function of \( n \) variables \( Z_1, Z_2, \ldots, Z_n \) is defined to be symmetric with respect to these variables if any interchange of these variables leaves the function identically
the same. The function $Z_1Z_2 + Z_1Z_3 + Z_2Z_3$ is symmetric in the variables $Z_1, Z_2, Z_3$. This is true since any permutation of any two variables, at every place they appear, leaves the function unaltered.

In some cases it may be possible to write an apparently unsymmetric function as a symmetric function multiplied by or added to a simple term. Such would be the case with the function given above if the three terms had a common factor $Z_4Z_5$. The function could then have been written as $Z_4Z_5$ multiplied by the symmetric function. In situations of this type, the symmetric portion of the expression can be represented by a network to be described, and the extra terms can be drawn as series or parallel elements as the expression calls for.

**Additional Theorems**

Shannon has developed the following five theorems which describe the properties and the symbolic representation of the symmetric function.⁴

**Theorem**—The necessary and sufficient condition that a function be symmetric is that it may be specified by stating a set of numbers $a_1, a_2, \ldots, a_n$ such that if exactly $a_j$ of the variables are zero, where $a_j = 1, 2, \ldots, n$, then the function is zero and not otherwise. The set of numbers $a_1, a_2, \ldots, a_n$

---

⁴Shannon, op. cit., p. 8
may have any value from zero to \( n \), where \( n \) is the number of variables, and for convenience they will be called a-numbers. In the example given as a symmetric function the a-numbers are 2 and 3 since \( Z_1Z_2 + Z_1Z_3 + Z_2Z_3 \) is zero if either two or three of the variables are zero, but it is not zero if just one or none of the variables is zero. To find the a-numbers of a given symmetric function it is necessary to evaluate the function with 0, 1, ..., \( n \) of the variables equal to zero. The numbers for which the function is zero are the a-numbers of the function.

Theorem- The symmetric function of \( n \) variables \( Z_1, Z_2, ..., Z_n \) with the a-numbers \( a_1, a_2, ..., a_n \) will be written \( S_{a_1a_2...a_n}(Z_1, Z_2, ..., Z_n) \). The symbolic representation of the function discussed at several points in this section would be: \( S_{2,3}(Z_1, Z_2, Z_3) \). In the following theorems we will assume that the function and the a-numbers are known.

Theorem- The sum of two given symmetric functions containing the same variables is a symmetric function of those variables, having for a-numbers those numbers common to both given functions. This can be realized if the two networks are placed in series, both networks containing the same variables. The first network is closed only if 1, 2, or 3 of the variables are closed. The second is closed only if 3 or 4 of the variables are closed. It can be seen that the whole circuit will be closed only if 3 of the variables are closed. This circuit could then be replaced by one contain-
ing the same variables but which is closed only when three
of the variables are closed. This is the statement of the
theorem given above. Writing this theorem symbolically we
have: \( S_{1,2,3}(Z_1,Z_2,...Z_6) + S_{3,4}(Z_1,Z_2,...Z_6) = S_{3}(Z_1,Z_2,...Z_6) \)

Theorem- The product of two given symmetric functions
containing the same variables is a symmetric function of these
variables with all the a-numbers appearing in either or both
of the given functions as a-numbers of the final function.
This can be shown in a similar manner to the theorem above
by considering the two networks in parallel. The symbolic
equation for this product is: \( S_{1,2,3}(Z_1,Z_2,...Z_6) \)
\* \( S_{3,4}(Z_1,Z_2,...Z_6) = S_{1,2,3,4}(Z_1,Z_2,...Z_6) \).

Theorem- The inverse of a symmetric function is a sym­
metric function of the same variables having for a-numbers
all the numbers from zero to n that are not contained in the
original function. This is logical, because the inverse circuit
would require the inverse impedance of the original circuit.
If the original circuit operated when 1, 2, or 3 of the vari­
ables are closed, the inverse circuit would be inoperative
when 1, 2, or 3 of the variables are closed but would be oper­
ative if 0, 4, 5, or 6 of the variables are closed. This may
be written as follows: \( S_{1,2,3}(Z_1,Z_2,...Z_6) = S_{0,4,5,6}(Z_1,Z_2,...Z_6) \).

So far we have said nothing about designing a circuit
that will perform the operations of a symmetric function.
Before the general circuit is given for a function with any
number of variables, we will consider a simple case. Take for instance the function: \( S_2(Z_1, Z_2, Z_3) \). In other words, we will design a circuit that will operate a relay when any two of three push buttons are pressed simultaneously but will fail to operate the relay if none, one, or three of the push buttons are pressed. The circuit of Figure 24 is found to meet the conditions set forth.

![Symmetric function with a-number = 2.](image)

This circuit may be divided into three bays, one for each variable, and four tiers marked 1, 2, 3, and 0. The terminal p is connected to the tier corresponding to the a-number. We will examine the circuit to see if it has the properties desired. In passing through the circuit from left to right the first set of contacts encountered are the ones belonging to the first push button. If the button is not pressed the circuit is closed through \( X_1 \), and we can move one bay to the right. If the first contact was closed we would have moved up one level. In either case the next two contacts to be
confronted are the ones belonging to the second push button. Here again we have the alternative of moving to the right one bay or up one level depending on whether the push button is pressed. The same situation is encountered at the next junction. It will be noted that the only possible way to complete the circuit is to push two of the buttons. Using any other combination leads to an open circuit. Five of the elements in Figure 24 are superfluous and can be omitted resulting in Figure 25. This circuit contains seven contacts. If a system had been set up using series-parallel contacts, a minimum of nine contacts would have been necessary. The series-parallel circuit is shown in Figure 26.

![Series-parallel circuit](image)

**Fig. 25.** Simplification of Fig. 24.

**Fig. 26.** Series-parallel representation of the circuit in Fig. 25.

If an attempt to simplify Figure 26 is made, a different arrangement of contacts results, but the minimum of nine ele-
ments remains.

The general procedure for drawing the circuit for the general symmetric function is exactly the same as that followed in the example. Representing the contacts or elements by straight lines, the general circuit is shown in Figure 27.

![Fig. 27. General symmetric function circuit.](image)

After the terminal \( p \) is connected to the levels corresponding to the \( a \)-numbers of the desired function, all the superfluous elements may be disregarded.

**Shifting Down**—In certain cases it is possible to simplify the circuit by shifting down levels. If the function \( S_{0,3,6}(Z_1,\ldots,Z_6) \) is desired, instead of continuing the circuit up to the sixth level we can connect the third and sixth levels to the zero level as shown in Figure 28. Terminal \( p \) is then connected to the zero level, and we have produced a great saving of contacts.
Figure 29 shows that additional contacts may be eliminated.

The shifting down process results in a saving of contacts by utilizing some of the contacts more than once. Inspection of the circuit will reveal sufficient facts to determine whether it can be shifted down. The shifting down process can always be performed when the a-numbers form an arithmetic progression.

In the one example it was evident that an economy of elements could be obtained by using a symmetric function instead of a series-parallel representation. Shannon gives a proof that this economy of elements holds in the general case.\(^5\) In these proofs he shows that a function of the sym-

\(^5\)Ibid., pp. 7-9
metric type represented by a series-parallel circuit requires \(3 \cdot 2^{n-1} - 2\) elements, while the same function can be realized by a symmetric function circuit with only \(4(n-1)\) elements, where \(n\) is the number of variables involved. When \(n=2\) in these equations both circuits require the same number of elements. This is a special case, because the symmetric function circuit and the series-parallel circuit are identical when only two variables are involved.

The general network of Figure 27 contains \(n(n+1)\) elements. We will show that for any given selection of \(a\)-numbers, at least \(n\) of the elements are unnecessary. Each number from 1 to \(n-1\), inclusive, which is not in the set of \(a\)-numbers produces two unnecessary elements; 0 or \(n\) missing will produce one unnecessary element. However, if two of the \(a\)-numbers differ by only one, then two elements will be superfluous. If more than two of the \(a\)-numbers are adjacent, or if two or more adjacent numbers are missing, then more than one element for each \(a\)-number will be superfluous. It is evident, then, that the worst case will be that in which the \(a\)-numbers are all odd or all even numbers from 0 to \(n\). In each of these cases it is easily seen that \(n\) of the elements will be superfluous.
To this point we have developed several useful operational tools that can be applied in theory to solve various problems in relay and switching systems. In practice we find that there are other factors which affect the solution of these problems. It is the purpose of this section to point out some of the limitations of the theory set forth and also other factors involved.

In some of the previous examples many contacts were operated by the same switch or push button. In setting up these circuits in the laboratory we may find that a switch having the exact number of contacts is not available. It is certainly feasible that switches and relays can be made to have almost any desired characteristic. In many cases, however, unless special apparatus is made, it is necessary to have a switch operate a relay which has the desired contacts. If too many contacts are desired for one switch, it may be necessary to have the master switch operate two or more relays which may be either in series or parallel depending on the relay ratings and other circuit conditions. In selecting a switch to fit a desired application, one may find more contacts on the switch than the minimum number of contacts required by the problem. It is still advisable to use the least possible number of contacts for two reasons: the wiring of the circuit is greatly simplified in most cases, and in
trouble-shooting the circuit there are fewer points to check for failure. If great reliability is required, sometimes it might be more desirable to use two contacts in parallel.

These few points are very helpful in setting up a solution to a problem. Three problems and their solution will now be discussed. It is believed that these examples will clarify many of the difficulties encountered in applying this analysis to relay and switching problems.

**Symmetric Function Circuit**

The problem is to construct a circuit consisting of six push buttons that will turn on a lamp when none, any three, or all six of the buttons are depressed. If any one, two, four, or five of the buttons are depressed the light will go out. This circuit can be realized by a series-parallel representation, but the number of contacts required would be prohibitive. The symmetric function approach gives a circuit that performs the desired operation. The circuit for this operation was given in Figures 28 and 29. The circuit was first set up in the laboratory according to the general symmetric function before the shifting down process was applied. The contacts that were required by this set-up were numerous and the actual wiring was fairly complicated. When the circuit was connected as shown in Figure 29 many of the contacts were eliminated and the wiring was greatly simplified. Photographs of these circuits are shown on the
following page. In both of these circuits five of the push buttons did not have the desired number of contacts so these push buttons were used to operate corresponding relays. In the first case the push buttons X₄ and X₅ required two relays in parallel in order to obtain the desired number of contacts. When the shifting down process was applied the two extra relays were eliminated.

The detailed diagram of the circuit used in the experiment is shown in Figure 30. It will be noted that relay Xₐ which controls the operation of the lamp is connected in series with the symmetric function circuit. This relay has both make and break contacts and the operation of the lamp can be reversed by throwing switch X₇. In other words the lamp can be lighted by depressing any one, two, four, or five of the push buttons, but the light will be off if none, any three, or all six of the push buttons are depressed. This point should be noted carefully, for it is a help in solving many problems of the symmetric function type. If the problem above had been to design a circuit that would operate a lamp if any one, two, four, or five of the six push buttons were pressed, this could have been done by the circuit given in Figure 30 with X₇ in the proper position. If this second circuit had been set up by the general symmetric function method there would have been many contacts that were necessary. It should be remembered that a general symmetric function is a planar network and its inverse can be found by
Set up of circuit in Fig. 28

Set up of circuit in Fig. 29

Fig. 30. Circuit diagram of the symmetric function problem.
the method outlined on page 48. In this case the inverse will have the same number of elements as the original circuit. The inverse of a symmetric function can also be found by the theorem set forth on page 55. If the inverse is found in this last manner, it will often contain fewer elements than the original network. The previous example was a case of this kind. The inverse of $S_{1,2,4,5}(Z_1,...Z_6)$ is $S_{0,3,6}(Z_1,...Z_6)$ which is a shift down function. In this case the inverse could not be obtained by the method of page 48, because a shift down function is a non-planar network. Even if the inverse is not a shift down function many times it too will contain less elements than the original network. The network can then be transformed into an inverse network that will perform the same operation as the original network. A general rule to follow to determine whether a symmetric function can be simplified by using its inverse is: If the inverse is a shift down function or if the inverse contains less a-numbers than the original function the circuit can be simplified. If the circuit is of the first type of transformation, a correcting relay must be used in series with the circuit. If the circuit is of the second type the inverse can be found directly by transformation.

Design of a Variable Combination Lock and Door Bell

The next problem is to design a lock which will open only if three push buttons are depressed in the correct se-
sequence. If the buttons are pushed in the wrong sequence the door bell will ring and wipe out any holding relays that were correctly operated previously. After the lock has been operated another push button will return the circuit to the starting conditions. It is also desirable to provide means for using all the possible combinations of the sequence of operation. Before we are able to write any equations we must designate all the circuit components. The push buttons will be \( X_1, X_2, \) and \( X_3 \). The lock release button will be \( X_4 \); the holding relays for the respective push buttons will be \( X_a, X_b, \) and \( X_c \); and \( X_d \) will be the bell relay. A contact of \( X_c \) will control the operation of the lock. In order to solve the problem we will assume that the correct sequence for operating the lock is \( X_1, X_2, \) and \( X_3 \). After the circuit has been solved using these conditions, additional connections can be made to the selector switch in order to give the other possible combinations.

Since \( X_1 \) is to be operated first, we may write:

\[
Z_{oa} = Z_4 + Z_1Z_a + Z_d
\]

(60)

This equation states that \( X_a \) is operated and holds itself closed until either \( X_4 \) or \( X_d \) is operated. Since \( X_a \) has prepared the circuit for the next push button, we may write:

\[
Z_{ob} = Z_4 + Z_a + Z_bZ_2
\]

(61)
These equations are progressive and we may write:

\[ Z_{oc} = Z_4 + Z_c Z_3 + Z_b \]  \hspace{1cm} (62)

These three equations take care of all the stated conditions except the ringing of the door bell. The door bell is to ring whenever \( X_2 \) or \( X_3 \) are depressed incorrectly. If the buttons are pushed in the proper sequence, nothing will happen. In other words, \( X_a \) must be operated before \( X_2 \) or \( X_3 \), and \( X_b \) must be operated before \( X_3 \). If these conditions are not met the door bell will ring. Thus we may write:

\[ Z_{od} = (Z_2 + Z_a')(Z_3 + Z_b') \]  \hspace{1cm} (63)

These four equations meet the requirements stated in the problem. By grouping in determinant form it is seen that \( X_4 \) contact is needed only once.

\[
\begin{align*}
Z_{oa} &= Z_1 Z_a + Z_d \\
Z_{ob} &= Z_4' Z_a + Z_b Z_2 \\
Z_{oc} &= Z_b + Z_c Z_3 \\
Z_{od} &= (Z_2 + Z_a')(Z_3 + Z_b')
\end{align*}
\]  \hspace{1cm} (64)

These equations have now been simplified as far as they can be. It will be noted that in the second equation if \( Z_1 Z_a \) had been written in place of \( Z_a \), the operation of the circuit would not have been changed but further simplification could
have been made. The same is true for the third equation. As far as the operation is concerned nothing is changed if we write \( Z_b \) as \( Z_2Z_b \) and also add another \( Z_1Z_a \). If the first equations had been written in this manner it would have appeared that superfluous elements were being introduced. It is found that the circuit is actually simplified when the revised equations are placed in determinant form.

\[
\begin{align*}
Z_{oa} &= + Z_d' \\
Z_{ob} &= Z_4 + Z_1Z_a + Z_2Z_b \\
Z_{oc} &= + Z_3Z_c \\
Z_{od} &= (Z_2 + Z_4')(Z_3 + Z_b')
\end{align*}
\]

(65)

The circuit for this last set of equations is given in Figure 31. These sets of equations are not identical even though they represent circuits which have the same operations. This is a good point to remember when setting up equations for a group of given conditions. The first equations written at random may not lead to a direct simplification. The first equations should be thoroughly investigated for possible elimination of contacts. Anytime that a contact appears in more than one place in the set of equations, there is always a possibility that the set may be simplified.

Experience and previous knowledge of the type of problem involved aids greatly in the final solution. A mere
study of the theory set forth will not always give the simplest solution.

This circuit takes care of the first combination. Since the push buttons are operated in sequence one at a time and no buttons are operated more than once, there are six possible combinations. A selector switch made up of five, two terminal, six position wafers will give the desired connections for the six combinations. The problem of connecting the selector switch is beyond the purpose of this thesis so further explanation will be omitted. Pictures of the actual laboratory experiment along with the circuit diagram are shown on the next page.

**Time Delay Relays**

So far in this thesis we have not mentioned time delay relays. One of the purposes of the laboratory work was to find the part which relays of this type play in the theory that has been presented.

Experience with problems involving time delay relays is the only certain way to know if a time delay relay will be required. If a problem is encountered which requires a time delay relay in order to complete the solution, it will become obvious by following a logical procedure in writing the equations.

It is often helpful to have a definite notation for time delay relay and its contacts. Hence, if $X_a$ is a time delay relay the coil can be represented by $X_a(T)$ and the
Two views of the combination lock and door bell

The light is used to simulate the action of the lock. When the light is on the lock would be open.

Fig. 31. Circuit diagram of the combination lock and door bell.
contacts by $X_a(t + p)$, where $p$ is the delay in seconds and $t$ is the time when the circuit conditions are such that the factors controlling the delay are set into operation.

To illustrate the above points we will design a circuit that will light a lamp when push button $X_1$ is depressed the first time; the second time that $X_1$ is operated the lamp will be turned off. This problem is to be solved without the use of any stepping switches or ratchet switches.

The first equation is obvious and is:

$$z_{oa} = z_1z_a + z'_b$$

(66)

The given conditions state that when $X_1$ operated the first time, the lamp would light. Under these conditions $X_b$ could not operate the first time the push button $X_1$ is depressed. In writing this first equation it was assumed that $X_a$ controls the operation of the lamp, and when $X_a$ is closed the lamp is on. It now becomes obvious that a time delay is necessary. An alternative solution would result if $X_1$ was a momentary make-contact, but this type of circuit is unstable and likely to cause the contacts to chatter if the exact period of the make-contact is not maintained. This alternative is in itself a sort of time delay situation in that the contacts must close in a certain order which requires specially designed "make before break" and "break before make" contacts. This circuit can also be realized by use of a combination of constant-voltage and constant-current re-
lays. Since this type of solution is not possible with our analysis, the circuit using a time delay will be used. If $X_b$ is a break contact on a time delay relay which operates $p$ seconds after $X_1$ is depressed we have the simplest solution to the problem. The complete equations for this solution can be written:

$$Z_{oa} = Z_a Z_1 + Z_b'(t + p)$$

$$Z_{ob}(T) = Z_a Z_1$$

This solution has certain limitations in that the first time $X_1$ is operated it must be released before $p$ seconds has passed, but the second time $X_1$ is operated it must be closed for a period exceeding $p$ seconds.

In some cases this might have been the desired circuit, but the more general interpretation would be to have the light come on at the first push of the button and to likewise have it go off at the second push. The solution under these conditions will now be carried out. It will be necessary to use three relays instead of two. The first relay will set the time delay relay into operation. The time delay relay will set up circuit conditions that will make it possible to turn off the light when $X_1$ is operated the second time. The following equations are sufficient to satisfy the given conditions.
\[ Z_{oa} = Z_1 Z_a + Z'_c \]

\[ Z_{ob}(T) = Z_1 Z_a \]  \hspace{1cm} (70)

\[ Z_{oc} = Z_1 + Z_b (t + p) (Z_c) \]

In this case the same contact used for the first \( X_1 \) can not be used in the third equation. If this was done \( X_c \) would operate as soon as the time delay was over.

The time delay relay used in the laboratory experiments was a tube-operated relay employing a thyratron with A.C. plate voltage and a R.C. time circuit in the grid. The complete circuit diagram and photographs are given on the following page.

It can be seen from the previous example that time delay relays can be useful in simplifying certain problems, but no definite rules can be laid down as to when they are necessary. By exercising previous knowledge, a compilation of representative types of circuits can be made which require the use of time delay relays. Two general types of circuits that require time delay relays are as follows: A circuit which requires the control of two different elements by a third element at different times and the inverse of this, a circuit in which two elements control a third element when it is physically impossible to operate the two elements at the same instant.

The laboratory experiments varify and clarify many
Equipment set up for the time delay circuit

Two views of the tube operated time delay relay

Fig. 32. Time delay relay circuit.
points that arise in solutions of problem. A summary of these facts will be given in the conclusions.
CONCLUSIONS

It is concluded that the solution of any relay or switching problem that can be approached from the open or closed circuit viewpoint is aided by the proper application of the theory presented in this thesis. There are practical limitations and extensions to the application of the theory. These are points which are not readily recognized from theoretical solution but which require laboratory experiments to verify them.

The following summary should aid in the practical application of the theory of this thesis:

1. Selection of necessary switches and relays, utilizing combinations in order to obtain desired elements.

2. Simplification of all wiring even though there is an excess of contacts, except when parallel contacts are used to obtain reliable operation.

3. Careful investigation of circuits before applying simplification theorems especially if the circuit contains "make before break" or "break before make" contacts.

4. Use of inverse circuits in simplifying problems that involve symmetric function circuits.

5. Investigation of original equations, in circuits similar to the lock problem, to see that they are in a form that may be simplified to the greatest degree.

6. Investigation of use of time delay relays and
combinations of constant-voltage and constant-current systems if the problem cannot be solved with ordinary switches and relays. It should be remembered that this analysis makes no provision for the use of time delay relays and combinations of constant-voltage and constant-current applications other than the condition given above.
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