COMPUTER-AIDED-DESIGN OF METAL-OXIDE SEMICONDUCTOR CIRCUITRY USING A PROCESS-SENSITIVE DEVICE MODEL

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# TABLE OF CONTENTS

<table>
<thead>
<tr>
<th>Section</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>ACKNOWLEDGEMENTS</td>
<td>ii</td>
</tr>
<tr>
<td>LIST OF TABLES</td>
<td>v</td>
</tr>
<tr>
<td>LIST OF ILLUSTRATIONS</td>
<td>vi</td>
</tr>
<tr>
<td>SUMMARY</td>
<td>vii</td>
</tr>
<tr>
<td>Chapter</td>
<td></td>
</tr>
<tr>
<td>I. INTRODUCTION</td>
<td>1</td>
</tr>
<tr>
<td>The Problem</td>
<td>1</td>
</tr>
<tr>
<td>Semiconductor Device Modeling</td>
<td>1</td>
</tr>
<tr>
<td>Impact of the MOS Device</td>
<td>2</td>
</tr>
<tr>
<td>Literature Review and Background</td>
<td>2</td>
</tr>
<tr>
<td>Purpose</td>
<td>4</td>
</tr>
<tr>
<td>II. COMPUTER-AIDED-DESIGN OF LSI ARRAYS</td>
<td>7</td>
</tr>
<tr>
<td>Array Topological Design Using Computer-Aided-Design</td>
<td>7</td>
</tr>
<tr>
<td>The Layout Problem</td>
<td>7</td>
</tr>
<tr>
<td>The Element Design</td>
<td>9</td>
</tr>
<tr>
<td>III. MOS DEVICE MODELING</td>
<td>13</td>
</tr>
<tr>
<td>Structure of the MOS Device</td>
<td>13</td>
</tr>
<tr>
<td>Qualitative Description of Operation</td>
<td>13</td>
</tr>
<tr>
<td>Development of the Model</td>
<td>19</td>
</tr>
<tr>
<td>List of Approximations</td>
<td>19</td>
</tr>
<tr>
<td>Operation in the Linear Region</td>
<td>20</td>
</tr>
<tr>
<td>Operation in the Saturation Region</td>
<td>27</td>
</tr>
<tr>
<td>Conductance in the Saturation Region</td>
<td>29</td>
</tr>
<tr>
<td>Operation in the Low Level Region</td>
<td>32</td>
</tr>
<tr>
<td>Operation in the Breakdown Region</td>
<td>33</td>
</tr>
<tr>
<td>Temperature Effects</td>
<td>34</td>
</tr>
<tr>
<td>Parasitic Resistances</td>
<td>35</td>
</tr>
<tr>
<td>Parasitic Capacitances</td>
<td>35</td>
</tr>
<tr>
<td>The Four Terminal Model</td>
<td>38</td>
</tr>
<tr>
<td>Final Device Equations</td>
<td>40</td>
</tr>
</tbody>
</table>
**LIST OF TABLES**

<table>
<thead>
<tr>
<th>Table</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Parasitic Resistances for Three Popular MOS Processes</td>
<td>36</td>
</tr>
<tr>
<td>2. Device Parameter Polarities</td>
<td>45</td>
</tr>
<tr>
<td>3. Experimental Parameters for Reference Device</td>
<td>64</td>
</tr>
<tr>
<td>4. List of Experimental Test Equipment</td>
<td>65</td>
</tr>
<tr>
<td>5. Reference Device Experiment/Calculation Comparison for Ratio Solution</td>
<td>68</td>
</tr>
</tbody>
</table>
## LIST OF ILLUSTRATIONS

<table>
<thead>
<tr>
<th>Figure</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>Comparison of Earlier Theoretical Device Model with Present-Day Theory</td>
<td>5</td>
</tr>
<tr>
<td>2.</td>
<td>&quot;Standard Cell&quot; MOS Inverter Topological Design</td>
<td>8</td>
</tr>
<tr>
<td>3.</td>
<td>Metal Mask of a Computer-Designed MOS Array</td>
<td>10</td>
</tr>
<tr>
<td>4.</td>
<td>Automated MOS/LSI Design Process</td>
<td>12</td>
</tr>
<tr>
<td>5.</td>
<td>Structural Characteristics of the MOS Device</td>
<td>14</td>
</tr>
<tr>
<td>6.</td>
<td>Modes of MOS Electrical Operation</td>
<td>16</td>
</tr>
<tr>
<td>7.</td>
<td>MOS Device Coordinates</td>
<td>21</td>
</tr>
<tr>
<td>8.</td>
<td>Electric Field Distribution for the MOS in the Saturation Region</td>
<td>31</td>
</tr>
<tr>
<td>9.</td>
<td>Schematic of MOS Parasitic Resistances</td>
<td>37</td>
</tr>
<tr>
<td>10.</td>
<td>Schematic of MOS Parasitic Capacitances</td>
<td>39</td>
</tr>
<tr>
<td>11.</td>
<td>Four-Terminal MOS Model (P-Channel)</td>
<td>41</td>
</tr>
<tr>
<td>12.</td>
<td>Four-Terminal Model of MOS Inverter</td>
<td>42</td>
</tr>
<tr>
<td>13.</td>
<td>Computational Technique Used to Evaluate MOS Drain Current as a Sensitive Function of Parasitic Resistances and Effective Majority-Carrier Mobility.</td>
<td>48</td>
</tr>
<tr>
<td>14.</td>
<td>MOS Characteristics at 225 °K</td>
<td>49</td>
</tr>
<tr>
<td>15.</td>
<td>MOS Characteristics at 300 °K</td>
<td>50</td>
</tr>
<tr>
<td>16.</td>
<td>MOS Characteristics at 375 °K</td>
<td>51</td>
</tr>
<tr>
<td>17.</td>
<td>MOS Terminal Resistance Variation at $V_T = 1.5$</td>
<td>54</td>
</tr>
<tr>
<td>18.</td>
<td>MOS Terminal Resistance Variation at $V_T = 4.28$</td>
<td>55</td>
</tr>
<tr>
<td>19.</td>
<td>MOS Sensitivity to Oxide Thickness at $L_T = 0.35$ mils</td>
<td>56</td>
</tr>
</tbody>
</table>
20. MOS Sensitivity of Oxide Thickness at $L_1 = .25$ mils  . . . 57
21. Current Relationships in the MOS Inverter  . . . . . . . . . . . . 58
22. MOS Capacitive Charge and Discharge  . . . . . . . . . . . . . . 61
23. Equipment Set-Up for Experimental Verification  . . . . . . . 66
24. Comparison of Theory and Measurement - Inverter Device  . . 69
25. Comparison of Theory and Measurement - Load Device  . . . . 70
26. Comparison of Theory and Measurement - Transient Calculation .71
27. MCS Inverter Design Algorithm  . . . . . . . . . . . . . . . . . . 75
28. MOS Inverter "Optimum Design" Algorithm  . . . . . . . . . . . . 76
SUMMARY

Metal-Oxide-Semiconductor (MOS) technology began to have an impact on the electronics industry in 1965, and by 1980 is expected to dominate the semiconductor computer memory market. Although research in the field of semiconductor surface-state physics has been highly active since 1960, accurate theoretical models for the MOS device have only been available since 1969.

At the present time, the MOS design engineer uses as design tools circuit models developed early in the development of the MOS technology—models which have since become inaccurate due to smaller device dimensions made possible by present-day photographic techniques.

In this investigation, the MOS device model is systematically developed and implemented on a set of computer programs which are then used to generate several sensitivity studies. The validity of the MOS model is demonstrated by comparison of electrical and physical measurements with the results of program calculations. Good agreement between measurement and theory is obtained over a wide range of parameters. Particular attention is given to the "linear-saturation" boundary region, which has not been given sufficient treatment previously.

The application of the proposed model to a generalized Computer-Aided-Design Program is discussed, with recommendations for future research into MOS device modeling.
CHAPTER I

INTRODUCTION

The Problem

Semiconductor Device Modeling

Metal-Oxide-Semiconductor (MOS) technology is beginning to have a substantial impact on the electronics industry. At this time, there is a significant gap in the latest theoretical device models and the usage of these models by the circuit engineer. Most of the MOS circuitry being designed makes use of an earlier device model, established in 1961 through 1963 (1,2). Although the model was useful at that time, the advance in semiconductor processing and photographic technology has rendered certain assumptions of the MOS operation invalid. For example, MOS transistor geometries could be reduced three-fold in the period from 1961 to 1967, primarily due to finer line width and definition of the MOS photomask plates. Certain assumptions regarding inter-electrode effects became invalid with the advent of these smaller geometries. A high degree of activity in the study of semiconductor surface-state physics has since resulted in many device models for the circuit engineer's use. The circuit engineer must now be aware of these device models, and be able to select which features of the MOS operation are to be incorporated into the design of large-scale arrays.
Impact of the MOS Device

As Large-Scale-Integration (LSI) arrays are being introduced into electronic equipment, dramatic changes in system and circuit design conventions become apparent. The use of MOS/LSI in a digital system can result in a 100-to-1 reduction in part interconnections, a 10-to-1 reduction in power consumption, and a 5-to-1 reduction in envelope size. Faced with these promising characteristics, many electrical engineers are anticipating and preparing for this technology. Unfortunately, the semiconductor industry is at a point where MOS design techniques are being guarded jealously in order to obtain a competitive edge. MOS/LSI technology is just now being discussed in technical institutions, and will continue to grow in importance in the engineering curriculum, as engineering students become familiar with actual LSI array design.

Literature Review and Background

The first description of a Metal-Oxide-Semiconductor device appeared in a patent by J. E. Lelienfeld, "Device for Controlling Electric Current," U. S. Pat. 1,900,018, March 7, 1933. Although the initial concept of the device appeared very early, practical fabrication of MOS circuits were not possible until 1964-1966. In 1961, H. K. J. Ihantola of Stanford Electronics Laboratories proposed a systematic design theory for the MOS device (1), and C. T. Sah fully characterized the MOS device in a paper presented in 1964 (2). Although much of the studies for semiconductor conduction mechanisms were performed several decades earlier by Ryder (3) and Shockley (4), studies of critical areas such as hole surface mobility characteristics
and effects of surface-states did not begin in earnest until 1964 with efforts by Hofstein and Warfield (5), Deal, Snow and Grove (6), and many others (7-18).

It is significant to note that early attempts to utilize the MOS technology failed primarily because of a lack of understanding of MOS physics. In 1963 a small company, General Microelectronics, entered into a contract with Victor Comptometer to produce the first Large-Scale-Integration (LSI) calculator. Although highly sophisticated circuit techniques were worked out for the calculator, each semiconductor wafer yielded only .01% to .1% good die which eventually caused the firms' collapse in 1966. However, once researchers directed their attention from injection minority-carrier devices (bipolar transistors) to field-controlled majority-carrier devices (field-effect transistors), process yields began to steadily increase until 40% yields of very large arrays (140-mil on a side) are being reported in 1971 in popular trade magazines such as "Electronic News," a weekly newspaper published by Fairchild Publications, New York, New York.

In the latter part of the 1960 decade attention was on two problem areas of the MOS device: the oxide-silicon interface and the effect of accumulated charge in the bulk of the device. Initial studies of radiation effects disclosed that MOS devices are sensitive to radiation damage in the insulating oxide film (19,20). A significant observation of MOS behavior became apparent when the device dimensions were reduced by a factor of 5, compared to Sah's and Thantola's experimental units. When the MOS majority-carrier induced channel
becomes "pinched off" for certain values of gate-to-drain voltage, it is said to be operating in the "saturation region." The device conductance in the saturation region, previously assumed to be zero, was discovered to be a strong function of oxide thickness, terminal (source-drain) dimensions, and electric field at the gate electrode. These effects, reported by D. Frohman-Bentchkowsky (21), Grove (22), Vadasz (23), and Cobbold (24) have caused a re-assessment of the device design methods in several cases (Figure 1). Earlier array designs not incorporating these effects almost always resulted in a design error on the "safe" side, that is, array operation would be slower, but the function was guaranteed. New designs, however, should make use of the latest device models, as the result will often be equivalent performance with a higher density of circuitry. Two books have recently been published which describe the status of MOS development up to 1970 (25, 26).

Purpose

The purpose of this research is to investigate several MOS models proposed in the literature, select a model from the standpoint of circuit application, use the newly-developed equations in the device model, perform experiments on the latest devices and validate the model with comparisons of computer program calculations. The conclusion will recommend the use of a particular model, and outline the construction of a general-purpose sensitivity-design program.

Computer-Aided-Design of MOS/LSI circuits generally resolves into two major areas: the topological layout problem and the element design problem (design of NAND gates, flip-flops, etc.). This research will demonstrate that the topological layout problem has been essentially
Figure 1. Comparison of Earlier Theoretical Device Model with Present-Day Theory
solved on several fronts, but that element design remains to be thoroughly explored. Topological design of MOS/LSI arrays generally proceeds in a well-defined heuristic algorithm, using computerized techniques which operate on a pre-defined "library" of circuit elements, arranging these elements according to the circuit configuration.
CHAPTER II

COMPUTER-AIDED DESIGN OF LSI ARRAYS

Array Photomask Design Using Computer-Aided-Design

The Layout Problem

Large-Scale-Integration circuitry can generally be divided into two major areas:

Well-ordered arrays (Memories, including serial, random-access and read-only memories)
Disordered arrays (general logic, sequential or combinational which in general cannot be performed efficiently by use of memories)

Memory circuits readily lend themselves to two-dimensional repetitive layouts, hence they will not be considered further. Disordered arrays are generally a complex grouping of gates and storage elements whose interconnections are not predictable from one circuit to another. The most successful computerized technique for handling this type of circuitry has been called the "Standard Cell" technique. This method recognizes that the layout problem must cope with the elements (cells) and the interconnect. The use of standard logic elements suggests that "cells" may be partitioned into a "library," and the interconnect customized to define the circuit pattern.

An example of a "standard cell" is shown in Figure 2, where the topology for the cell is carefully designed so that interfacing to adjacent cells and the cell interconnect can be completely described
Figure 2. "Standard Cell" Topological Design
by a serial algorithm, and committed to a computer program. The completed layout of an LSI chip is shown in Figure 3, where the placement of the cells is shown as a linear and folded plot, and the interconnect routed between and around the cells to completely define the chip. This method of array design has been highly successful, enabling an engineer to complete a chip design within two weeks, as compared to six months by manual methods. It will be noted that the "standard cell," once designed, is not altered but used as an element repeatedly.

There is one deficiency in this type of design: the "cells" are almost always over-designed since the layout can always be improved by a designer altering the chip design by hand. Most of the time, however, this consideration is unimportant when the press of schedule and initial-design confidence are important factors.

The Element Design

If the computer is to modify the "standard cells," there are several options:

(1) Maintain several "families" of cells, each capable of supplying a signal to a certain number of other cells.

(2) Modify the design of the cell itself, so that one dimension of the cell changes with a given modification.

Of the two possibilities, the option of maintaining several "families" has been preferred to date. There is one notable exception, however. A certain class of MOS circuitry, which requires a four-phase clock, is readily capable of "cell modification" within the
Figure 3. Metal Mask Design of an MOS/LSI Chip
(approximately 50X)
chip (27). This type of circuitry is recognized as an exceptionally complex logic mechanism, however, and requires extensive calculations at every logic node and clock-driven node. A combination of highly developed computer aids and long experience in array layout is required to implement this logic form.

A design process flow of an automated layout system is shown in Figure 4. This type of computerized system can produce a finished MOS/LSI chip design within two weeks after definition of the logic diagram. This same design effort would take as much as six months if done manually. Since computer aids have almost solved the chip topological design problem, the "cell," or element design problem merits further consideration. In order to consider the automated design of an MOS "cell," a highly-accurate device model would be required and then implemented in a heuristic algorithm which would seek an optimum topological solution for an MOS cell from constraints of power, output drive, input capacitance, and speed.
Figure 4. Automated MOS/LSI Design Process
CHAPTER III

MOS DEVICE MODELING

Structure of the MOS Device

The MOS may be described as an insulated-gate induced majority-carrier device, capable of enhancement or depletion mode operation, depending on substrate doping level and polarity. An MOS is said to be enhancement-mode if a forward-bias on the gate electrode (with respect to the source) causes an increase in source-drain current, and is depletion-mode if a reverse-bias on the gate electrode causes a decrease in source-drain current (see Figure 5a).

An exaggerated isometric view of the MOS is shown in Figure 5b, along with typical dimensions. Although the term MOS implies an oxide insulator, many forms of insulated-gate field-effect transistors use nitride, aluminum oxide, or other materials as the gate insulator. A popular form of MOS does not use a metal electrode but instead uses a layer of highly doped polycrystalline silicon. A more general term for these devices may be IGFET, for insulated-gate field-effect transistor, but since MOS has been used for so long, it is doubtful that the term will be dropped.

Qualitative Description of Operation

The MOS operation can be described from the observation at its terminals or from the condition of the induced channel. These modes of operation are summarized as follows:
I-V Characteristics of the MOS

Figure 5 Structural Characteristics of the MOS Device
MOS OPERATION (P-CHANNEL)

<table>
<thead>
<tr>
<th>Observation of Channel</th>
<th>Figure</th>
<th>Observation of Source-Drain Terminals</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electron Accumulation</td>
<td>6a</td>
<td>Cut-Off</td>
</tr>
<tr>
<td>Flat-Band</td>
<td>6b</td>
<td>Cut-Off</td>
</tr>
<tr>
<td>Inversion</td>
<td>6c</td>
<td>Linear Conduction</td>
</tr>
<tr>
<td>Pinch-Off</td>
<td>6d</td>
<td>Saturated Conduction</td>
</tr>
<tr>
<td>Punch-Through</td>
<td>6e</td>
<td>&quot;Evident&quot; Breakdown</td>
</tr>
</tbody>
</table>

Consider Figure 6a. Initially, a net positive charge at the silicon-silicon dioxide interface due to broken bonds and interface charge causes an electron accumulation below the ground gate. No current flow is possible since all junctions are reversed-biased.

Figure 6b indicates that the gate has been brought to a potential sufficiently negative as to cause the electron accumulation at the surface to approach the substrate concentration. Since this neutralization of surface effects maintains the substrate concentration, the Fermi Level is given as

\[ E_F = \frac{1}{2}(E_C + E_V) + \frac{1}{2}kT \ln \frac{N_V}{N_C} \]  

(1)

where \( E_C, E_V, N_C, N_V \) are the energy levels and densities of states in the conduction and valence bands, respectively. A "flat-band" condition at the semiconductor surface is caused when the electron and hole concentrations, well known as

\[ n = N_C e^{-\frac{(E_C - E_F)}{kT}} \quad \rho = N_V e^{-\frac{(E_V - E_F)}{kT}} \]
6a. Electron Accumulation

6b. Flat-Band

6c. Inversion

Figure 6. Modes of MOS Electrical Operation
6d. Inversion Layer Pinch-Off

6e. Source-Drain Punch-Through

Figure 6. (continued) Modes of MOS Electrical Operation
are the same as in the substrate bulk. Since the source and drain terminals are still reversed-biased relative to the substrate, there is no source-drain conduction.

Figure 6c illustrates that a further increase of the gate voltage will drive more electrons into the substrate bulk, causing a population of holes to accumulate at the channel surface. When the hole accumulation is high enough to cause appreciable current flow (10µA), the channel is said to be inverted, or changed from N-type to P-type. For low values of the drain voltage, the source-drain current is proportional to the gate voltage, hence the device is said to be in the region of linear conduction.

An increase in drain voltage will cause an increase in drain current until the potential difference from drain to gate approaches the flat-band voltage. At this point, the hole concentration near the drain electrode goes to zero, and a high-resistivity depletion region is left. A further increase in drain voltage will cause little increase in drain current, as a high-resistivity "pinched-off" channel region will take up most of the potential drop. The term "saturation", for the MOS device is applied to this region of operation (Figure 6d).

As the drain voltage is further increased, the drain depletion region spreads toward the source terminal. At some point, the drain P-N junction will either go into avalanche breakdown or will experience a "punch-through" from drain to source, as the drain depletion region approaches the source depletion region, (Figure 6e).
Development of the Model

List of Approximations

The mathematical development given here represents an adaptation of the theoretical work of Sah (2) with refinements by Cobbold (26), Grove and Frohman-Bentchkowsky (22), L. Vadasz (27), and Frohman-Bentchkowsky (28). The author's primary contribution is one of bringing together the development and clarifying certain aspects of saturation region operation.

Initially, the "gradual-channel-approximation," first proposed by Shockley (1,4) will be made. This approximation allows an easy derivation of the MOS equations from Gauss' law, since it proposes a linear conductive channel along the MOS surface. After the simple theory is developed, the approximations given below will be lifted to develop the final equation:

1. Total extrinsic conditions which affect channel conduction such as oxide traps and surface states are considered as a single term defined as Q_{SS} (Surface-state charge) lumped together and located at the silicon-oxide interface.

2. Leakage currents from source to drain due to thermally-generated minority carriers are neglected.

3. The gate oxide dielectric is a perfect insulator.

4. Substrate doping is uniform.

5. Parasitic resistances are neglected.
(6) The thickness of the dielectric is assumed to be much greater than the channel thickness.

(7) Carrier mobility in the channel is constant.

(8) There is no drain-to-channel negative feedback.

(9) Channel Thickness variation is small.

**Operation In the Linear Region**

From Figure 7,

\[ W = \text{Channel width} \]
\[ L = \text{Channel length} \]
\[ x_{c} = \text{Channel depth} \]

The orthogonal coordinate system \( x, y, z \) is taken along the directions of channel depth, length and width, respectively. By integrating along the channel depth, the total current in the channel is given by:

\[
I_{DS} = \int_{0}^{x_{c}} J W dx = \int_{0}^{x_{c}} \sigma E_{y} W dx = \int_{0}^{x_{c}} q \bar{\mu}_{p} \left( -\frac{dV}{dy} \right) W dx. \tag{2}
\]

If the material is homogeneous (ie, \( E_{y} \neq f(x) \)), and if we define

\[
\bar{\mu}_{p} = \frac{\int_{0}^{x_{c}} \rho(x) \mu_{p} dx}{\int_{0}^{x_{c}} \rho(x) dx} \quad \text{(average hole mobility)}
\]

then

\[
I_{DS} = -qW \frac{dV}{dy} \int_{0}^{x_{c}} \rho(x) dx
\]

The final problem will be to evaluate the total charge within the channel.
Figure 7. MOS Device Coordinates
Applying Gauss' theorem:
\[ \int_{\text{closed surface}} D \cdot ds = \text{charge enclosed by the surface} \]

or,
\[ \int_{\text{top}} D \cdot ds + \int_{\text{bottom}} D \cdot ds + \int_{\text{ends}} D \cdot ds + \int_{\text{sides}} D \cdot ds = \text{charge enclosed by the surface} \]

It can be seen that the regions external to the device such as above the gate, below the substrate and regions on the ends and sides will have zero charge since the electric field is perpendicular to the channel and uniform in the x, z direction. Therefore,
\[ \int_{\text{surface}} D \cdot ds = 0, \quad \text{and } Q_{\text{enclosed}} = 0. \]

The enclosed charges are:
- Surface charge: \( Q_{SS} \) (coulombs/meter\(^2\))
- Gate Charge: \( Q_G \) (coulombs/meter\(^2\))
- Acceptor impurity ions: \( N_A \) (number/meter\(^3\))
- Donor impurity ions: \( N_D \) (number/meter\(^3\))
- Free electrons: \( n \) (number/meter\(^3\))
- Free holes: \( p \) (number/meter\(^3\))
- Un-ionized holes: \( p_A \) (number/meter\(^3\))
- Un-ionized electrons: \( n_D \) (number/meter\(^3\))

Thus
\[ Q_{\text{enclosed}} = Q_{SS} + Q_G + q \int_{A}^{D} (p + p - n - n - N + N) dx = 0 \]
Define

\[ Q_{\text{silicon}} = q \int_{0}^{\infty} \left( p + p_A - n - n_D - N_A + N_D \right) dx. \]

Then

\[ Q_{\text{enclosed}} = Q_{\text{SS}} + Q_G = Q_{\text{silicon}} = 0. \]

The gate charge, \( Q_G = C_o \, V_{\text{ox}} (y) \) where \( V_{\text{ox}} \) is the total voltage across the oxide layer. As will be shown later, \( V_{\text{ox}} \) is not uniformly distributed in the oxide layer, but is given by

\[ V_{\text{ox}} (y) = V_{G_S} - V(y) \]

where \( V_{G_S} \) is the equipotential on the metal gate electrode and \( V(y) \) is the voltage distributed over the semiconductor surface and is a variable due to the assumed uniform channel gradient and increasing potential from source to drain along the channel. The total free hole charge per unit area in the channel is then

\[ q \int_{0}^{\chi_c} \rho(x) dx = Q_{\text{SS}} + C_o (V_{G_S} - V(y)) + Q_{\Phi} \]

\( Q_{\Phi} \) is defined as the total charge in the silicon less the free hole charge in the channel

\[ Q_{\Phi} = q \int_{0}^{\infty} (p + p_A - n - n_D - N_A + N_D) dx - q \int_{0}^{\chi_c} \rho dx \]

To simplify the final expression, several assumptions and approximations will be made:
(1) All impurities are ionized, thus

\[ p_A << p \quad \text{and} \quad n_D << n \]

(2) Since the substrate is N-type silicon,

\[ N_D >> N_A \]

From these approximations,

\[ Q_B = q \int_0^\infty (N_D - n) dx + q \int_{x_c}^\infty p dx, \]

but \[ q \int_{x_c}^\infty p dx = 0, \]

so \[ Q_{\text{silicon}} = Q_B + q \int_0^{x_c} p dx \]

The total charge equation becomes

\[ Q_{ss} + Q_G + Q_B + q \int_0^{x_c} p dx = 0 \quad (3) \]

The gate charge, \( Q_G \), is due to the applied gate voltage, the metal-semiconductor work function difference, and the surface potential of the silicon.

\[ Q_G = C_o \left[ V_G - V(y) \right] = C_o \left[ V_G - \phi_{so} - \phi_{MS} \right] \]

\( (C_o = \varepsilon_{so}/t_{ox}, \ \text{expressed as \text{pf/cm}^2}) \)

Substituting,

\[ q \int_0^{x_c} p dx = -C_o \left[ V_{GS} + (Q_{ss} + Q_B)/C_o + \phi_{so} + \phi_{MS} \right]. \]
Then:

\[ I_{DS} = \mu_p C_0 W \left( \frac{dV}{dy} \right) \left[ V_{GS} + (Q_{SS} + Q_B)/C_0 + \phi_{SO} + \phi_{MS} \right]. \quad (4) \]

Assuming that the total charge is neutralized within the depletion region, the charge in the bulk region is given by:

\[ Q_B = -q N_D x_{d(max)} \quad (5) \]

where the depth of the depletion region is given by

\[ x_{d(max)} = \sqrt{\frac{2 k_S \varepsilon_0 (V(y) + \phi_{SO})}{q N_D}} \quad (6) \]

Then

\[ Q_B(y) = -q N_D x_{d(max)}(y) = -\sqrt{2 k_S \varepsilon_0 q N_D (V(y) + \phi_{SO})} \]

Assuming that the surface silicon charge is not a function of \( V_{GS} \), the energy band bending at the silicon surface must be enough to support significant majority carrier conduction. It has been shown that "strong inversion" will be reached if it is assumed (11) \( \phi_{SO} = 2 \phi_F \).

The entire charge in the silicon inversion layer is given by:

\[ Q_n(y) = C_0 \left\{ \sqrt{\frac{2 N_D q \varepsilon_0 k_S (V(y) - V_{BS} + 2 \phi_F)}{C_0}} - V_{BS} + V_{g(y)} + 2 \phi_F + \phi_{MS} - \frac{Q_{SS}}{C_0} \right\} \]

The \( V_{BS} \) is a reversed-bias junction voltage, referred to as the substrate bias. The "flat-band" voltage is defined as that potential required to bring the minority carrier concentration at
the channel to the point existing in the bulk region. The resulting decreasing density of states in the channel causes the valence and conduction energy bands to "flatten out" to the same point existing in the neutral bulk. The equation describing this "flat-band" condition is given by:

\[ V_{FB} = \phi_M - Q_{SS} / C_0 \]

and the final current equation is given by:

\[
\int_0^L I_d \, dy = \bar{\mu}_F \int_0^{V_{GS}} \left\{ C_0 \left[ V_{GS} - V_{FB} + 2 \phi_F - V(y) \right] - \sqrt{2N_0 q \varepsilon_s \left[ V(y) - V_{BS} + 2 \phi_F \right]} \right\} dV(y)
\]

Integrating,

\[
I_D = C_0 \bar{\mu}_F \left( \frac{W}{L} \right) \left\{ V_{OS} \left( V_{OS} - V_{FB} + 2 \phi_F \right) - \frac{V_{OS}^2}{2} \right\} - \frac{2}{3} \sqrt{\frac{2N_0 q \varepsilon_s}{C_0^2}} \cdot \left[ \left( V_{OS} - V_{BS} - 2 \phi_F \right)^{3/2} - \left( 2 \phi_F - V_{BS} \right)^{3/2} \right]
\]

An approximation of this equation can be made by taking the series expansion of the third term:

\[
I_D = C_0 \bar{\mu}_F \left( \frac{W}{L} \right) \left\{ V_{OS} \left[ V_{GS} - V_{FB} + 2 \phi_F - \sqrt{\frac{2N_0 q \varepsilon_s (2 \phi_F - V_{OS})}{C_0}} \right] \right\}.
\]
The final term can be expressed as:

$$A \sqrt{2 \phi_F - V_{DS}}, \quad A = \frac{\sqrt{2 N_d q \varepsilon_s}}{C_0}$$

thus,

$$I_D = C_0 \mu_p \left( \frac{W}{L} \right) \left\{ \left( V_{G} - V_{FB} + 2 \phi_F - A \sqrt{2 \phi_F - V_{DS}} \right) V_{DS} \right\} \tag{8}$$

for small $V_{DS}$. This approximation is commonly used for design purpose and is a good approximation to the theoretical equation for low $V_{DS}$ and low substrate doping levels.

The final equation for the drain current in the linear region can now be obtained, with all voltages referred to ground, instead of the source terminals:

$$I_{DS} = \left( \frac{W}{L} \right) \mu_p C_0 \left\{ \left[ \left( V_{G} - V_{FB} + 2 \phi_F - V_b/2 \right) V_D - \left( V_D - V_{FB} - 2 \phi_F - V_b/2 \right) V_b \right] - \frac{2}{3} \frac{1}{C_0} \sqrt{2 K_s \varepsilon_0 q N_d} \left[ \left( V_D + 2 \phi_F \right)^{3/2} - \left( V_b + 2 \phi_F \right)^{3/2} \right] \right\} \tag{9}$$

**Operation in the Saturation Region**

When this equation is evaluated, it is found that a maxima exists, beyond which $I_D \rightarrow 0$ for increasing $V_D$. This maxima will occur at
\[ \frac{\partial I_D}{\partial V_D} = 0. \]

At this point the "gradual channel approximation" (approximation number 9) becomes invalid. The reason for this becomes evident when it is seen that

\[ Q_G = C_0 \left[ V_D - V_\gamma \right] \]

decreases for increasing \( V_D \). There will be a point where the electric field terminating on the channel near the drain electrode becomes insufficient to cause inversion, or

\[ V_D < \left( V_{FB} + 2 \phi_F \right) \]

The lack of the inversion layer near the drain electrode creates a depletion region of high resistivity. This depletion region will then account for most of the voltage drop across the channel as \( V_D \) is increased. The value of \( V_D \) where the inversion layer concentration is reduced to the intrinsic level is called the "saturation voltage" and can be found by the following:

\[ K = \frac{\sqrt{2 N_D q \xi_s}}{C_0} \]

\[ V_T = V_{FB} + 2 \phi_F \quad V_D = 0. \]
Then,
\[
\frac{\partial I_D}{\partial V_D} = 0 = \mu_p C_0 \frac{\partial}{\partial V_D} \left[ (V'_6 - V_T - V'_6/2) V_D' \right] - \frac{2}{3 C_0} \frac{\partial}{\partial V_D} K (2\phi_F)^{3/2}
\]
and
\[
V_D + \frac{2\phi_F}{3} K (2\phi_F)^{3/2} = V_6 - V_T
\]

\(V_D(SAT)\) will typically be an order of magnitude greater than \(2\phi_F\), hence the simplification
\[
V_D + \frac{2\phi_F}{3} K \sqrt{V_D} - (V_6 - V_T) = 0.
\]

This equation can be solved using \(t^2 = V_D\) as a change of variable, yielding the only valid root,
\[
V_D(SAT) = \left[ \frac{1}{8} \sqrt{\frac{16}{81} K^2 + (V_6 - V_T) - \frac{2}{3} K} \right]^2
\]

This final expression, which has not been developed as such in the literature to date, indicates a point where assumptions 7, 8 and 9 become invalid.

**Conductance in the Saturation Region**

Earlier researchers (1, 2) assumed a zero conductance in the saturation region (for \(V_D > V_D(SAT)\)). Actual devices presently exhibit a finite conductance (Figure 1). Assuming the increase of drain current in the saturation region is due entirely to the shortening of the channel length when the "pinch-off" region appears, the following relationship can be obtained:
\[ I_D^{(\text{SAT})} = \frac{I_D^{(\text{SAT})}}{1 - \frac{L}{L_{\text{dep}}}} \]  

(11)

Where \( I_D^{(\text{SAT})} \) is the value of the drain current at \( V_D = V_D^{(\text{SAT})} \), \( L \) = the unmodulated channel length, and \( L_{\text{dep}} \) denotes the reduction in channel length.

The \( L_{\text{dep}} \) can be expressed as a function of the device and applied voltage as:

\[ L_{\text{dep}} = \frac{V_D - V_D^{(\text{SAT})}}{E_T} \]

(12)

Where \( V_D = V_D^{(\text{SAT})} \) is the voltage across the "pinched-off" region, and \( E_T \) is the transverse electric field component near the silicon surface. Bentchkowsky and Grove (22) proposed that the transverse electric field be approximated by the following (Figure 8):

\[ E_T = E_1 + E_2 + E_3 \]

(13)

\( E_1 \) = channel surface field

\( E_2 \) = drain field termination

\( E_3 \) = channel end termination

\( K_0 \) = relative silicon dioxide dielectric constant

\( K_s \) = relative silicon dielectric constant

\[ E_1 = \frac{1}{K(V_D - V_D^{\text{sat}})^{\frac{1}{2}}} \]

\[ E_2 = \alpha \frac{K_0}{K_s} \left( \frac{V_D - V'_G}{t_{\text{ox}}} \right), \quad E_3 = \beta \frac{K_0}{K_s} \left( \frac{V'_G - V_D^{(\text{sat})}}{t_{\text{ox}}} \right), \]

\[ K = \sqrt{\frac{2K_s E_0}{qN_0}}, \quad V'_G = V_G + Q_{ss}/C_0, \quad \alpha = 0.2, \quad \beta = 0.6 \]
Figure 3. Electric Field Distribution for MOS in the Saturation Region (22)
The constants $\alpha, \beta$ are "field fringing" factors, and allow the assumption that the transverse fields are proportional to the normal fields across the oxide, instead of using a rigorous solution of Poisson's equation.

An approximation is now made which is valid for low substrate concentration or thin oxide (most MOS designs),

$$t_{ox} \ll \kappa \left( V_D - V_{D(sat)} \right)^2$$

The expression for $I_{dep}$ is now given from equations 12 and 13,

$$I_{dep} = \frac{K_{st} t_{ox}}{K_0} \cdot \frac{V_D - V_{D(sat)}}{\alpha (V_D - V_G') + \beta (V_G' - V_{D(sat)})}$$

Operation in the Low Level Region

In deriving the expression for drain current in the linear region, the assumption was made that MOS conduction cannot begin until the onset of "strong inversion", or at the point where the surface potential is twice the Fermi potential, or

$$\phi_s \approx 2 \phi_F.$$
It has been shown that current in the channel exhibits an exponential behavior from approximately

\[ V_g = \left( \frac{1}{V_{FB}} + \frac{2\phi_F}{V} \right)^{-1.3} \]

with channel currents ranging from 1pA to 1μA (29).

For design purposes, it is sufficient to neglect these low-level currents, but to realize that transistors must be biased close to the flat-band voltage to insure complete cut-off.

**Operation in the Breakdown Region**

An MOS device can exhibit three modes of breakdown:

- **Drain-source "punch through"** drain avalanche breakdown and gate oxide breakdown. Drain-source "punch-through" occurs in a non-conducting MOS device when the reverse-bias depletion region normally surrounding the drain P-region spreads into the substrate for increasing drain potentials until the depletion region for the drain and source terminals touch. Holes will then be accelerated at high velocity from source to drain. Drain avalanche breakdown occurs at the drain-substrate diode for a given voltage depending on substrate doping and junction curvature. Gate oxide breakdown occurs when field strengths of 10^7 V/cm. in the oxide are exceeded, or approximately 100 volts across 100 Å of oxide. Gate oxide breakdown is a destructive breakdown, whereas punch-through and avalanche breakdown become important only when localized substrate heating causes silicon crystal damage.

Operation in these breakdown regions is generally unpredictable and has not proven useful enough to justify analytical study. It will be sufficient for design purposes to "forbid" this type of
operation by appropriate design rules:

Punch-through: drain-source spacings will be such that punch-through will not occur for operating voltages.

Avalanche: operating voltages will be less than the avalanche voltage.

Oxide breakdown: gate field strengths will be less than $10^7$ V/cm, under operating conditions.

Temperature Effects

It has been shown that the majority carrier mobility in the channel is a function of temperature (12,13) and gate voltage (23). The combined effect of these conditions can be expressed by the following equations:

$$\mu_{\text{eff}} = \mu_{\text{eff}(0)} \left( \frac{T}{300^\circ A} \right)^{-3/2} \left( \frac{E_{S0}}{E_S} \right)^{C_i}$$

where $\mu_{\text{eff}(0)} = \text{low gate voltage mobility at } 25^\circ C$

$E_{S0} = 6 \times 10^4$ V/cm

$E_S = -(V_G - V_{PB} - 2\phi - 0.5V_D - 0.5V_s) \cdot (C_0/K_s \epsilon_o)$

$C_i = 0.22$ for p-channel devices

$C_i = 0.36$ for n-channel devices

Temperature also affects the flat-band voltage as the Fermi level increases for increasing temperature, hence the threshold voltage is decreased, on the order of $-4\text{mV/}^\circ C$ for most practical MOS devices (26).

Graff and Neilen determined that $Q_{ss}$ is constant over a
wide temperature range (12). The expression for the temperature
coefficient of the threshold voltage is given by (26),

$$\frac{dV_T}{dT} = \frac{3}{T} \left( V_{GS} - V_T \right) - \left( \frac{0.605 - \frac{9}{T}}{T} \right) \left[ \frac{2 (V_G - V_T)}{V_D (S_{AT})} - 1 \right]. \quad (16)$$

The fact that the threshold voltage decreases with increasing
temperature on the order of 3 to 5 mV/°C, causes some concern
in the design of practical arrays. Reduced threshold voltage will
seriously affect the noise margin of MOS digital circuits unless
suitable allowance is made for this effect.

Parasitic Resistances

Approximation (5) will now be eliminated by examining
the parasitic resistances associated with MOS devices. Examination
of Figure 9 will indicate that certain parasitic resistances such as the
device terminal drain and source resistance $R_D$ and $R_S$ are important
while the diode "spreading" resistance $R_{SD}$ and $R_{SS}$ can be neglected as
small, the gate oxide resistance $R_{ox}$ can be neglected as large.
The resistances $R_D$ and $R_S$ are especially important when using diffused
regions as signal and power conductors. Every attempt in MOS array
layout is made to use gate metal as interconnection material, as
the resistivity is several orders of magnitude lower than P-region.

Representative parasitic resistances for several processes
are presented in Table 1.

Parasitic Capacitances

MOS parasitic capacitances are caused by intrinsic capacitances
Table 1. Parastic Resistances for Three Popular MOS Processes

<table>
<thead>
<tr>
<th>Parastic Resistor</th>
<th>Process</th>
<th>&lt;111&gt; P-MOS Silicon Gate</th>
<th>&lt;100&gt; N-MOS Metal Gate</th>
<th>&lt;111&gt;, &lt;100&gt; P-MOS Metal Gate</th>
</tr>
</thead>
<tbody>
<tr>
<td>Diffused Region</td>
<td>30 Ω/□</td>
<td>20 Ω/□</td>
<td>100 Ω/□</td>
<td></td>
</tr>
<tr>
<td>Gate Conductor</td>
<td>40 Ω/□</td>
<td>.05 Ω/□</td>
<td>.05 Ω/□</td>
<td></td>
</tr>
<tr>
<td>Second-Level</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Conductor (Metal)</td>
<td>.05 Ω/□</td>
<td>...</td>
<td>...</td>
<td></td>
</tr>
<tr>
<td>Diffused-Region ohmic contact to metal</td>
<td>10 Ω/mil²</td>
<td>10 Ω/mil²</td>
<td>10 Ω/mil²</td>
<td></td>
</tr>
</tbody>
</table>
Typical Values:

$R_G = 2$ ohms

$R_{ox} = 10^{16}$ ohms

$R_{SD}, R_{SS} = 5$ ohms

$R_D, R_S = 50$ ohms to 500 ohms
(resistance of diffused region)

Figure 9. Schematic of MOS Parasitic Resistances
associated with the device construction, and extrinsic capacitance associated with the device layout or external connection (Figure 10).

The intrinsic capacitances are (referred to the gate):

- $C_{gs}$ (gate-source intrinsic capacitance, etc.)
- $C_{gb}$ (gate-body intrinsic capacitance)
- $C_{gd}$ (gate-drain intrinsic capacitance)

The extrinsic capacitances are:

- $C_{gde}$ (gate-drain)
- $C_{gse}$ (gate-source)
- $C_{de}$ (drain)
- $C_{se} = 0$ if assumed to the source is grounded

These extrinsic capacitances are caused by the "overlap" of the metal-over-diffused region and distributed source and drain interconnect.

The leading capacitance presented to an MOS circuit consists of two terms (26),

$$C_L = C_1 + C_2 (\phi) \left( \frac{\phi}{\phi + V} \right)^n$$

(17)

where $C_1$ is the capacitance due to the metal-to-substrate proximity over thick oxide (15,000Å), and $C_2(0)$ is the distributed P-N junction capacitance measured at zero bias, $\phi = 0.6V$, $n = 2$ for doping levels and junction profiles normally used in MOS circuits ($N_D \approx 10^{15}$).

**The Four Terminal Model**

The final circuit model for the MOS device will include
Figure 10. Schematic of MOS Parastic Capacitances
lumped capacitance terms,

\[ C_{gd} = C_{gdi} + C_{gde} + \frac{1}{2} (C_{gdi}) \]
\[ C_{gs} = C_{gsi} + C_{gse} + \frac{1}{2} (C_{gbi}) \]
\[ C_s = 0 \]
\[ C_d = C_{de} = C_{di} \]

The source capacitance will be zero for a grounded device, and will be assigned to the drain capacitance of the lower device in a logic inverter circuit.

The final four-terminal model is shown in Figure 11. The current generator, \( I_D \), is a function of the voltages appearing at \( V_D \) and \( V_S \), referred to as the device "internal voltages" and will be different from the drain and source terminal voltages by the amount equal to the IR drop across \( R_D \) and \( R_S \).

The drain and source diodes are assumed to be reverse-biased at all times (a valid assumption and a design goal - the "charge-control" diode model can be used if the diodes are to become forward biased at any time). The spreading resistances, \( R_{SD} \) and \( R_{SS} \), are very small and will be neglected in the device analysis.

Since all digital functions can be realized with NAND-gates, and the simplest NAND-gate is the inverter, the analysis work will utilize the inverter model. A schematic of an MOS inverter is shown in Figure 12 in terms of the four-terminal model. It will be noted that the diodes do not appear in the circuit model if they are reverse-biased at all times.

**Final Device Equations**

The equations for the final device will be given for the
Figure 11. Four-Terminal MOS Model (P-channel)
Figure 12. Four-Terminal Model of MOS Inverter
"strong inversion" case (i.e., $V_C > V_{FB} + 2 \phi_F$ for conduction), as a design goal of avoiding the low-level region of operation. In addition, the temperature dependence of the threshold voltage will be handled by evaluating $V_{FB}$ at $25^\circ$C, and assigning a $4\text{mV}/^\circ\text{C}$ decrease, linearly, over the $-55^\circ\text{C}$ to $+125^\circ\text{C}$ temperature range.

**Linear Region:**

$$I_D = \mu_{\text{eff}}(0) \frac{W}{L} \left( \frac{T}{300^\circ\text{C}} \right)^{-3/2} \left( \frac{E_S}{E_S} \right) c_i c_0 \cdot$$

$$\left\{ \left[ (V_G - V_{FB} - 2\phi_F - \frac{V_D}{2}) V_D - (V_G - V_{FB} - 2\phi_F - \frac{V_S}{2}) V_S \right] \right.$$

$$- \frac{2}{3} c_0 \sqrt{2k_S c_0 qN_D} \left[ (V_D + 2\phi_F)^{3/2} - (V_S + 2\phi_F)^{3/2} \right] \left\} \right.$$

**Saturation Region**

$$I_D = \frac{I_D'}{(1 - \frac{\rho_{dep}}{L})}$$

where $I_D$ is given at

$$V_D = V_D^{(SAT)} = \left[ \frac{1}{8} \sqrt{\frac{l_0}{g_i}} K^2 + (V_G - V_T) - \frac{4}{3} K \right]^2$$

$$K = \frac{\sqrt{2N_D qE_S}}{C_0}, \quad V_T = V_{FB} + 2\phi_F$$
and $I_{dep}$ is given by:

$$I_{dep} = \frac{K_S \xi_{ox}}{K_0} \cdot \frac{V_D - V_D^{(SAT)}}{\alpha(V_D - V_G') + \beta(V_G' - V_D^{(SAT)})}$$

$$V_G' = V_G + Q_{ss}/C_0$$

The polarities of various currents and potentials for MOS devices are shown for reference in Table 2.

Currents are defined positive flowing into the terminals, and polarities for $V_{GS}$, $V_{SB}$, and $I_B$ assume reverse bias operation.
Table 2. Device Parameter Polarities

<table>
<thead>
<tr>
<th>Quantity</th>
<th>Enhancement Mode</th>
<th>Depletion Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>N-Channel</td>
<td>P-Channel</td>
</tr>
<tr>
<td>$V_{DS}$</td>
<td>$&gt; 0$</td>
<td>$&lt; 0$</td>
</tr>
<tr>
<td>$V_{GS}$</td>
<td>$\geq 0$</td>
<td>$\leq 0$</td>
</tr>
<tr>
<td>$V_{DS}$</td>
<td>$\leq 0$</td>
<td>$\geq 0$</td>
</tr>
<tr>
<td>$V_{T}$</td>
<td>$&gt; 0$</td>
<td>$&lt; 0$</td>
</tr>
<tr>
<td>$I_{D}$</td>
<td>$&gt; 0$</td>
<td>$&lt; 0$</td>
</tr>
<tr>
<td>$I_{S}$</td>
<td>$&lt; 0$</td>
<td>$&gt; 0$</td>
</tr>
<tr>
<td>$I_{B}$</td>
<td>$&lt; 0$</td>
<td>$&gt; 0$</td>
</tr>
<tr>
<td>$\phi_{F}$</td>
<td>$&gt; 0$</td>
<td>$&lt; 0$</td>
</tr>
<tr>
<td>$Q_{B}$</td>
<td>$&lt; 0$</td>
<td>$&gt; 0$</td>
</tr>
<tr>
<td>$Q_{SS}$</td>
<td>$&gt; 0$</td>
<td>$&gt; 0$</td>
</tr>
<tr>
<td>$\delta \phi_{F}/\delta T$</td>
<td>$&lt; 0$</td>
<td>$&lt; 0$</td>
</tr>
<tr>
<td>$\delta V_{T}/\delta T$</td>
<td>$&lt; 0$</td>
<td>$&lt; 0$</td>
</tr>
</tbody>
</table>
CHAPTER IV

COMPUTER IMPLEMENTATION

Computer Simulation of the MOS Device

As previously discussed, earlier MOS theory involved the use of much simpler relationships. For example, the equations previously used for the MOS in the linear and saturation region are given as:

\[ I_D^* = \frac{\mu_p \epsilon_{ox}}{2 t_{ox}} \left[ 2(V_{GS} - V_T) V_{DS} - V_{DS}^2 \right] \]

\[ I_D = \frac{\mu_p \epsilon_{ox}}{2 t_{ox}} \left( \frac{W}{L} \right) (V_{GS} - V_T)^2 \]

These equations are easily solved directly. The more recent MOS theory, however, involves relationships too difficult to perform by hand.

Practical use of the proposed four-terminal model requires the use of a digital computer to perform the many calculations. The computer programs discussed herein are in a form to be easily implemented in a generalized Computer-Aided-Design program, and represent the solutions to four basic problems encountered in the MOS device design: transistor I/V relationships, inverter "ratio" design, capacitive charge through an active MOS and capacitive discharge through an active MOS. The use of these programs is demonstrated.
by several examples of the MOS sensitivity to variation of parameters and a comparison of experimental measurements on a commercial device to computer solutions of the device behavior. All programs were written in the FORTRAN V language and run on a UNIVAC 1106. Computer plots were provided on a CALCOMP 765 (California Computer Products Company) pen plotter. Each plotted line is established by 100 calculated points to provide very fine resolution.

MOS Static Simulation

The calculation of the MOS drain current characteristics (source-drain current verses gate voltages for a constant drain voltage) cannot be easily obtained by a direct solution of the device equations, since the dependent variable appears many times in the form

\[(I_D + \varphi)^n\]

where \(n = 2.0, 1.5, .5\) and .22, and \(\varphi\) is a constant term.

The approach taken in this study is to use an iterative procedure. The solution is predicted using a simple relationship, and then corrected by compensating for the effects of terminal resistance and surface mobility variation. A brief flowchart of the computational technique described is shown in Figure 13.

Since the four-terminal model exhibits sensitivity to temperature, oxide thickness and terminal resistances, it is possible to study the effects of variation of parameters. Figures 14, 15, and 16 illustrate the effect of temperature changes on a MOS device with the following device parameters:
Figure 13. Computational Technique Used to Evaluate MOS Drain Current as a Sensitive Function of Parasitic Resistances and Effective Majority-Carrier Mobility.
Figure 14. MOS Characteristics at 225° K
Figure 15. MOS Characteristics at 300° K
Figure 16. MOS Characteristics at 375° K
\[ N_D = 2 \times 10^{15} \text{ cm}^{-3} \] (substrate impurity level)

\[ \mu_p = 190 \text{ cm}^2/\text{V} \cdot \text{sec} \] (surface mobility at 300 °K)

\[ V_{FB} = -3.68 \text{ volts at 300 °K} \]

\[ \phi_T = -0.3 \text{ volts} \] (Metal-Silicon Work Function Difference)

\[ K_o = 4.5 \] (relative oxide dielectric constant)

\[ K_S = 12 \] (relative silicon dielectric constant)

\[ \epsilon_{ox} = 3.98 \text{ pf/cm} \] (permittivity of silicon dioxide)

\[ Q_{ss} = 5 \times 10^{-11} \text{ coulombs/cm}^2 \] (surface-state charge)

\[ R_D, R_S = 100 \text{ ohms} \]

\[ W = 3.68 \mu\text{m} \] (channel width)

\[ L = 0.88 \mu\text{m} \] (channel length)

\[ t_{ox} = 1,000 \text{ Å} \] (oxide thickness)

It can be noted that the slope of the \( I_D/V_D \) curve becomes greater with increasing gate voltage in accordance with the device theory, and that the combined effect of temperature on hole mobility and threshold voltage exhibits a substantial shift in operating characteristics. The transition from the linear region to the saturation region is accomplished by a change to the saturation region equation. The slight discontinuity at the point of transition can probably be traced to assumption number 8, that "there is no drain-to-channel negative feedback." Future work in accounting for this effect will probably remove the discontinuity.

Programs DRPLOT, TOXDRPLOT, RSVTIPLOT and DRPLOTSUB prepare drain current plots for sensitivity studies of an MOS device fabricated by any process, including N-channel, by substitution
of the appropriate parameter values.

**Effect of Variation of Parameters**

The LSI designer must contend with an MOS process which is subject to extreme variation. Effects of process variation must be taken into account in the design. Fortunately, it is possible to handle the design in such a manner that some parameter variations cancel out, since they appear as ratios in the design equations.

Figures 17 and 18 illustrate the effects of variation of the device source resistance from 100 Ω to 1000 Ω, and variation in the threshold voltage from 1.50 volts to 4.28 volts. It can be seen that drain current is a strong function of source resistance and threshold voltage. Since source resistance is a function of the array topological layout, a design goal is usually set to meet some specified maximum source resistance.

Oxide thickness variation causes two effects on MOS operation: a linear increase with drain current with decreasing oxide thickness and an increase in drain conductance in the saturation region. These combined effects can be seen in Figures 19 and 20, where the variation in oxide thickness is shown for two values of channel length. A comparison of these two plots will illustrate the increased conductance in the saturation region as a direct result of smaller channel length.

**MOS Inverter Design**

The basic MOS static inverter is designed by using one transistor biased "on" as a load element for another transistor, which is called the inverter, as shown in Figure 21. Input-output relationships are determined by the voltage-divider effect of the
Figure 17. MOS Terminal Resistance Variation at $V_T = 1.5$
Curves Indicated (1) are $R_S = 100 \Omega$ (2) are $R_S = 1000 \Omega$
Figure 18. MOS Terminal Resistance Variation at $V_T = 4.28$

Curves Indicated (1) are $R_S = 100 \, \Omega$  (2) are $R_S = 1000 \, \Omega$
Figure 19. MOS Sensitivity to Oxide Thickness at $L = .35$ mils

Curves Indicated (1) are $T_{ox} = .13\mu$ (2) are $T_{ox} = .09\mu$
Figure 20. MOS Sensitivity to Oxide Thickness at $L_T = .25$ mils

Curves Indicated (1) are $T_{ox} = .13\mu$ (2) are $T_{ox} = .09\mu$
$V_o$ is obtained when $I_{load} = I_{inverter}$

Figure 21. MOS Static Inverter Indicating Operating Output Voltages as a Function of Device Geometry and Applied Voltages
two transistors. Since the current equation for the MOS transistor can be expressed as:

\[ I_D = \frac{\mu_p \varepsilon_{ox}}{2 t_{ox}} \left( \frac{W}{L} \right) f(V_D, V_G, V_S, V_T, N_D, C_0, \Phi_f) \]

it can be seen that an adjustment of the device geometry (W/L) will affect the current independently of the applied voltages.

Selection of the load (W/L) is normally determined to be one-tenth the inverter (W/L). The output voltage is then found when

\[ I_{load} = I_{inverter} \text{, or} \]

\[ V_{out} = V_{DD} \left\{ \frac{R_{inverter}}{R_{load} + R_{inverter}} \right\}. \]

The ratio of inverter to load is dictated by logic level constraints.

Since the resistance of the MOS inverter and load is determined by the device geometry for the same operating voltages, inverter design is primarily one of mask topology.

The programs RATIO and RATIOSUB accept as input parameters the MOS inverter process and circuit specifications, and provides the ratio of inverter (W/L) to load (W/L) as the ratio-type inverter solution. Program computations utilize a predict-correct algorithm, similar to that described in Figure 13. Extensive program coding was required to handle the multiple parameter dependencies. The output voltage is found from the intersection of the inverter I/V
curve with the load I/V curve, as shown in Figure 21.

**MOS Transient Simulation**

An MOS/LSI array consists largely of distributed capacitors and MOS devices biased as resistors. Transient simulation, therefore, involves a nonlinear capacitive charge and discharge. Dimensions in an LSI array are so small (typical conductors run less than 50 mils) that lead inductance can be ignored; hence all charge and discharge equations are first-order. Numerical integration is required to handle the transient calculations, due to the complexity of the MOS current equation.

An examination of Figure 22 will indicate that the charge-time equation can be developed as follows:

\[
\frac{dV_o}{d\tau} = \frac{I_{DL}}{C_L} ,
\]

\[
\int_{v(0)}^{v(t)} dV_o = \frac{I_{DL}}{C_L} \int_0^{\tau_c} dt ,
\]

hence

\[
\tau_c = \int_{v(0)}^{v(t)} \frac{C_L}{I_{DL}(V)} dV_o
\]

The discharge-time solution can be found similarly,
22a. Current Flow for Charge Time Solution

22b. Current Flow for Discharge Time Solution

Figure 22. MOS Capacitive Charge and Discharge
\[
\frac{dV_o}{dt} = -\frac{1}{C_L} \left[ I_{DL} - I_{DI} \right],
\]

\[
\tau_{dch} = \int_{V(i)}^{V(e)} \frac{1}{C_L(V_o)} \frac{1}{I_{DL}(V_o) - I_{DI}(V_o)} \, dV_o
\]

In both cases, the load and inverter current is obtained as a function of internal device voltages, as represented in the four-terminal model. The Runge-Kutta numerical integration scheme is used in both calculations, and multiple predict-correct calculations are made in the programs CHARGE and DISCHARGE before each exit to the Runge-Kutta subroutine.
CHAPTER V

EXPERIMENTAL VERIFICATION

Reference Device Measurements

The device chosen for electrical measurements is the UL03C MOS Gate Array, manufactured by American Micro-Systems, Inc., Santa Clara, California.

AC and DC device measurements were made with the equipment and electrical connections shown in Figure 23. Physical measurements were made by de-capping the device and taking gate width measurements at 50X with a Unitron Series N Metallograph. Channel length measurements were made by observing the source-drain separation at 800X, after all oxides had been removed by an HF solution, the diffused region stained with a 10:1 HF/HNO₃ solution to clearly define the P-region. Making measurements of diffused-region separations is a critical science in itself, hence a proper estimate of the minimum and maximum, as visually observed, is given in Table 3. Oxide thickness measurements were made by comparing oxide coloration against an oxide thickness/color chart, after all metal had been removed by a weak NaOH solution. The parameter values used in the MOS device equations were taken directly from Table 3. The list of referenced test equipment used in making electrical measurements is given in Table 4.
Table 3. Experimental Parameters for Reference Devices

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Dimension Variation</th>
<th>Value used in Computation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channel Width (load)</td>
<td>1.40 to 1.44 mils</td>
<td>1.4 mils</td>
</tr>
<tr>
<td>Channel Length (load)</td>
<td>.31 to .35 mils</td>
<td>.32 mils</td>
</tr>
<tr>
<td>Channel Width (inverter)</td>
<td>26.3 to 26.5 mils</td>
<td>26.4 mils</td>
</tr>
<tr>
<td>Channel Length (inverter)</td>
<td>.19 to .22 mils</td>
<td>.2 mils</td>
</tr>
<tr>
<td>Channel Oxide Thickness</td>
<td>1000 to 1200 Å</td>
<td>1000 Å</td>
</tr>
<tr>
<td>Flat-Band Voltage</td>
<td></td>
<td>-3.68 volts</td>
</tr>
<tr>
<td>Load Source and Drain Resistance</td>
<td></td>
<td>400,100 ohms</td>
</tr>
<tr>
<td>Inverter Source and Drain Resistance</td>
<td></td>
<td>4 ohms</td>
</tr>
<tr>
<td></td>
<td>(Including metal-silicon contact and diffused-region)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>The following parameters were obtained as representative of the Thick Oxide MOS Process from the manufacturer</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$K_0$ (Relative oxide dielectric constant)</td>
<td></td>
<td>4.5</td>
</tr>
<tr>
<td>$K_S$ (Relative silicon dielectric constant)</td>
<td></td>
<td>12.</td>
</tr>
<tr>
<td>$\varepsilon_{ox}$ (permittivity of Silicon Dioxide)</td>
<td></td>
<td>0.398pf/cm</td>
</tr>
<tr>
<td>$Q_{SS}$ (Surface-State-Charge, calculated from the flat-band voltage)</td>
<td></td>
<td>$5 \times 10^{11}$ coulombs/cm$^2$</td>
</tr>
<tr>
<td>$\mu_p$ (Surface hole mobility)</td>
<td></td>
<td>190 cm$^2$/v-sec</td>
</tr>
</tbody>
</table>
### Table 4. List of Test Equipment

<table>
<thead>
<tr>
<th>Equipment Reference</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>DVM #1</td>
<td>Hewlett-Packard 3440A with 3445A plug-in</td>
</tr>
<tr>
<td>DVM #2</td>
<td>Hewlett-Packard 3440A with 3444A plug-in</td>
</tr>
<tr>
<td>E1, E2, E3</td>
<td>Hewlett-Packard 6200D</td>
</tr>
<tr>
<td>Oscilloscope</td>
<td>Tektronix Model 585A</td>
</tr>
<tr>
<td>Signal Generator</td>
<td>Rutherford Model 814</td>
</tr>
</tbody>
</table>
Drain Current Measurements

Device Ratio (Vin/Vout) Measurements

Charge/Discharge Time Measurements

Figure 23. Equipment Set-Up for Experimental Verification. Pin numbers are noted within circles.
Drain Current Measurements

Figure 24 and 25 illustrate the calculated drain current characteristic for the inverter and load device of the UL03C, using DRPLOT with parametric information obtained from the manufacturer and by direct measurement. The plotted points represent electrical measurements obtained from the test set-up illustrated in Figure 23. As can be seen from the device curves, agreement between measurement and theory is good, within 10% over a wide range of values. Measurements could not be taken for large values of $V_G$, since the increasing power dissipation of the device induce self-heating and resulting shift of characteristics.

Device Ratio Measurements

From direct measurements of the inverter, the ratio of inverter geometry to load geometry was found to be 30.2. Solutions for an inverter ratio using the program RATIO are given on Table 5. The input/output voltages used for the program input were taken from electrical measurements of the UL03C. Agreement between theory and experiment is within 8% over a wide range of values.

MOS Transient Calculations

In order to obtain the comparison of theory and experiment for the transient case, the set-up shown in Figure 23 was made for $V_{GG} = 27.0$ volts, $V_{DD} = 15.0$ volts, $C_L = .009$ microfarads, and input pulse level of -10.0 volts, rise and fall times of 50 nanoseconds. After the output waveform was recorded photographically, the response was plotted on Figure 26 against the solution obtained by using CHARGE and DISCHARGE. Comparison between experiment and theory in close for the transient case, this case being the most difficult to analyze.
Table 5. Comparison of Theory and Experiment for RATIO Program

<table>
<thead>
<tr>
<th>Input Voltage (volts)</th>
<th>Output Voltage (volts)</th>
<th>Computed Ratio</th>
<th>Measured Ratio</th>
<th>Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>7.500</td>
<td>2.320</td>
<td>27.3</td>
<td>30.2</td>
<td>9.5%</td>
</tr>
<tr>
<td>8.000</td>
<td>1.700</td>
<td>27.0</td>
<td>30.2</td>
<td>10.5%</td>
</tr>
<tr>
<td>8.500</td>
<td>1.408</td>
<td>27.3</td>
<td>30.2</td>
<td>9.5%</td>
</tr>
<tr>
<td>9.000</td>
<td>1.226</td>
<td>27.6</td>
<td>30.2</td>
<td>8.5%</td>
</tr>
<tr>
<td>9.500</td>
<td>1.096</td>
<td>27.8</td>
<td>30.2</td>
<td>8%</td>
</tr>
<tr>
<td>10.000</td>
<td>0.984</td>
<td>28.4</td>
<td>30.2</td>
<td>6%</td>
</tr>
<tr>
<td>10.500</td>
<td>0.910</td>
<td>28.4</td>
<td>30.2</td>
<td>6%</td>
</tr>
<tr>
<td>11.000</td>
<td>0.848</td>
<td>28.4</td>
<td>30.2</td>
<td>6%</td>
</tr>
<tr>
<td>11.500</td>
<td>0.795</td>
<td>28.5</td>
<td>30.2</td>
<td>5.6%</td>
</tr>
<tr>
<td>12.000</td>
<td>0.750</td>
<td>28.5</td>
<td>30.2</td>
<td>5.6%</td>
</tr>
<tr>
<td>12.500</td>
<td>0.711</td>
<td>28.5</td>
<td>30.2</td>
<td>5.6%</td>
</tr>
<tr>
<td>13.000</td>
<td>0.679</td>
<td>28.4</td>
<td>30.2</td>
<td>6%</td>
</tr>
</tbody>
</table>
Figure 24. Comparison of Theory and Experiment - Inverter Device
Figure 25. Comparison of Theory and Experiment - Load Device
Figure 26. Comparison of Theory and Experiment—Transient Case
CHAPTER VI

CONCLUSIONS

It has been shown that the MOS device can be successfully modeled on the basis of current theory. This model can now be used for circuit analysis or design work.

In pursuing the choice of the MOS mode, many inconsistencies in previously published material were encountered. For example, the equation normally used for defining the "saturation voltage" is given as

\[ V_{D(SAT)} = V_G - V_{FB} - 2\phi_F + \frac{K_S \varepsilon_0 q N_D}{C_0^2} \left[ 1 - \sqrt{1 + \frac{2C_0^2 (V_G - V_{FB})}{K_S \varepsilon_0 q N_D}} \right]. \]

This relationship, however, does not work in practice, and it is necessary to use the method previously defined in Chapter III.

Other disagreements concerning the behavior of MOS surface-states with temperature variation exist, and the effects of the gate electric field on majority-carrier mobility is an empirically-derived relationship which can greatly affect device operation. Throughout the programming for the MOS model, it was found that the majority-carrier voltage sensitivity was the dominant problem, causing more concern than parasitic resistances.
The application of the MOS model to digital circuit design requires the use of the programs RATIO, CHARGE and DISCHARGE. For DC-type MOS circuits, the load geometry is calculated from speed and power dissipation constraints. The inverter geometry is then determined from the load design, and logic level (input/output) requirements. An example of this design algorithm is given in Figure 27.

For DC-type MOS logic, there is an optimum ratio design to be determined from circuit and process requirements. This optimum design point has been studied extensively with the previous (1965) MOS model, but has not been examined with the new equations. An outline of the "optimum design algorithm" is given in Figure 28 for future research. Users of these programs for the purpose of studying the algorithms are cautioned that they are not optimized for run-time, and some optimization should be performed, especially if the algorithm on Figure 28 is to be considered.

In applying the current MOS model to the practical design of logic networks, it was found that the earlier theory produced errors approximately three times that of the proposed model. In almost every case, however, the error produced by the earlier model resulted in circuits which were over-designed. It can be said therefore, that the new model provides insights into MOS operation not previously realized, and gives the practicing engineer a grasp of the accuracy of his design equations. For example, previously designed ratio-type circuits can be examined using the new model to determine if smaller
inverter-to-load ratios can be used. New circuit designs can use the new model to predict circuit response more accurately. Finally, since the effects of mobility variation, terminal resistance and bulk-effect charge all serve to reduce MOS conductance, earlier designs will generally have larger ratios and lower predicted charge-discharge times. These two characteristics result in circuits that are "over-designed," hence use of the new MOS model will bring the circuit solution closer to the optimum point.
Increment

Input Design
Specifications

Input Circuit
Specifications

Input Process
Specifications

Assume

\[(\frac{W}{L})_L = 1\]

Calculate Charge Time

Is charge time ok?

High

Calculate Ratio from
Design Specifications

Calculate \( (\frac{W}{L})_I \) from Ratio

Is Prop. delay ok?

Yes

No

FINISH

Specification Incompatibility

Figure 27. MOS Inverter Design Algorithm
Process Specification

\[ V_T = V_T \text{ (min)} \]
\[ \text{Ratio} = \text{Ratio} \text{ (min)} \]

Calc. \((W/L)\) from \(\text{RATIO}\)

Calc. Pair Delay, \(K_L\) & \(K_T\)

\[ R \leftarrow R + 1 \quad \text{No} \]
\[ \text{is} \quad \text{Ratio} > R \text{ (Max)} \quad \text{?} \]
\[ \text{Yes} \]
\[ \text{is} \quad \text{No} \]
\[ V_T > V_T \text{ (Max)} \quad \text{Yes} \]

\[ K_L + K_L + \Delta \quad \text{is} \quad \text{No} \]
\[ K_L > K_L \text{ (Max)} \quad \text{Yes} \]

\[ V_T \leftarrow V_T + \Delta \]

\[ R = R \text{ (min)} \]

Stop

Figure 28. MOS Inverter "Optimum Design" Algorithm
APPENDIX I

COMPUTER PROGRAM LISTINGS
DKPLOT - MAIN PROGRAM

C—THIS PROGRAM COMPUTES A FAMILY OF DRAIN CURVES FOR A SPECIFIED
C—MOS DEVICE, IN PREPARATION FOR A CALCOMP 765 PLOT
C—OR A LINE PRINTER PLOT. ++VERSION+4/19/71++
C—THIS IS THE MAIN EXECUTIVE PROGRAM

DIMENSION A1(1000), A2(1000), A3(101), Z(10),
2X1(10, 100), Y1(10, 100)
REAL W1, W2, L1, L2, MP, CO, CB, VG, VFB, PHF, VD, KO, KS, VS,
1GSAT, VGMX, K1, K2, K3, K4, Q, EPOX, TOX, IDLIN, IO, VDS, VT, VTO,
2GMLIN, VSAT, VSAT, QSS, X1, VDMXC, VSDATP, IMDR, R, VDI, VS1,
3VO, VOJT, VINP, RP, K1, K2, LMIN, VGP, INCR, KPRIME, MPO, MPEFF
4, EPSO, VGP, GMSAT, VDI, VSL
4, TEMP, C1
INTEGER I, J, K
COMMON QSS, MP, CO, CB, VFB, PHF, KO, KS, EPSO, Q, EPOX, TOX, RD1,
1RSI, RDL, RSL, VDD, VG, K1, K2, K3, K4, W1, L1, L2, DEBUG, VT0,
2LMIN, KPRIME, INCR, TMAX, ESO, VIN, TEMP, C1

C—STATEMENT DEFINITIONS

IDLIN(WL, VG, VS, MP, CO, VT, KS, EPSO, Q, CB, PHF)
2=(W/L)*(MP*CO*(VG-VT-VD/2.)*VD-(VG-VT-VS/2.)*VS)
3=(2.E6/(CO*K3.))*SORT(2.*KS*EPSO*Q*CB)*
4=((SORT(VD+2.*PHF)*(V0+2.*PHF))-(SORT(VS+2.*PHF)*
5(VS+2.*PHF)))*

VSAT(VG, VT, VFB, KS, EPSO, Q, CB, CO)
2=VG-VT-(KS*EPSO*Q*CB/CO)**2*(1.-SORT(1.+2.E-12*CO*12**2))
3=(VG-VFB)/(KS*EPSO*Q*CB/CO)**2

GMSAT(ID, KS, TOX, CO, CB, VOSAT, VT1, L)
2=(ID/KS*K0*L*TOX**4*(VGP-VD)/
3(K0*KL*+(2*(VD-VGP)+4*(VD-VD/VDSAT))-KS*TOX*(VD-VD/SAT))**2

VGF(ID, W1, L1, L2, MP, CO, VD, VS, VT, PHF, K1)
2=(ID/(W/L))*(MP*CO*(VD-VS))-(VT*(VS-VD)+VS**2/2.-VD**2/2.
3-K1*(VD+2.*PHF)*SORT(VD+2.*PHF)-(VS+2.*PHF)*SORT(VS+2.*
4PHF))/(VD-VS)

C—INITIALIZE RUN
C—PROCESS CONSTANTS

TEMP=378.
CB=2.E15
MP=(190.)/(TEMP/300.)*SORT(TEMP/300.)
VFB=3.68-(TEMP-300.)*(.014)
PHF=.3
C1=.22
KO=4.5
KS=12.
EPSO=.085
Q=1.6E-19
ESO=6.E+4
EP0X=.398
TOX=1.E-4
VTO=VFB+2.*PHF
CO=EP0X/TOX
QSS=5.*E11
INCR=.01
KPRIME=(MP*EP0X)/(2.*TOX)
C--DEVICE AND SUPPLY CONSTANTS
VOMAX=16.
VGG=12.
VSS=0.
RS1=4.
RD1=4.
RSL=75.
RST=75.
w1=28.4/394.
L1=.2/394.
wl=1.4/394.
LL=.33/394.
CPNO=2.
CMOS=1.
VMAX=24.
DEBUG=0.
VG=24.
VMIN=8.
XL=0.
XH=VOMAX
YL=0.
YH=40000.
NCASE=1
NCASES=3
NCRV=5
LO=0
LPL0T=8
X1=L1*394.
X2=(w1/L1)*KPRIME*1.E-6
WRITE(6,10)NCASES,LPL0T,LO
10 FORMAT(*10---*/1.L1,VOMAX,A1,A2)
DO 30 M=1,5
CALL DRPLOT(VG,VOMAX,A1,A2)
DO 20 N=1,100
ZJ(M)=VG
XI(M,N)=A1(N)
20 YI(M,N)=A2(N)*1.E-6
VG=VG+4.
30 CONTINUE
32 CONTINUE
WRITE(6,40)ZJ(1),ZJ(2),ZJ(3),ZJ(4),ZJ(5)
40 FORMAT(1H1,5F20.1)
DO 60 N=1,100,2
WRITE(6,50)XI(1,N),YI(1,N),XI(2,N),YI(2,N),XI(3,N),YI(3,N),
2X1(4,N),2Y1(4,N),X1(5,N),Y1(5,N)
50 FORMAT(10E10.4)
60 CONTINUE
DO 100 M=1,100
J=100+M
K=200+M
N=300+M
I=400+M
A1(M)=X1(1,M)
A2(M)=Y1(1,M)
A1(J)=X1(2,M)
A2(J)=Y1(2,M)
A1(K)=X1(3,M)
A2(K)=Y1(3,M)
A1(N)=X1(4,M)
A2(N)=Y1(4,M)
A1(I)=X1(5,M)
A2(I)=Y1(5,M)
100 CONTINUE
CALL PLOTHC(NCRV,X1,X2,VMIN,VMAX,TEMP,XL,XH,YL,YH,ZJ,1XI,Y1)
TEMP=TEMP-75.
NCASE=NCASE+1
MP=(180.)/((TEMP/300.)*SQRT(TEMP/300.))
KPRIME=(MP*EP0X)/(2.*T0X)
x2=KPRIME*(W1/L1)*1.E-6
VG=24.
IF(NCASE-NCASES)19,19,201
201 CONTINUE
STOP 88A
END
SUBROUTINE FOR DRPLOT

C——+ VERSION+4/19/71—+
SUBROUTINE DRPLOT(VG, VMAX, A1, A2)
C——THIS PROGRAM PLOTS THE DRAIN CURRENT CHARACTERISTIC
COMMON QS0,MPr CO p CB F VFB P PHF
1RS1,RDL.RSL,VD0, VGK, K1, K2, K3, K4, WI, LL, WL, LL, DEBUG, VTO
2LMIN,KPRIME, INCR, TMAX, ESO, VIN, TEMP, C1
DIMENSION A1(101), A2(101), A3(101), P1(101), P2(101), P3(101)
2A4(50U)
REAL D, L, M, C, B, VG, VFB, PHF, KD, VS, KS, EPSO, VGP, GSAT, 2VGX, K1, Q, EPSO, TOX, IDLIN, ID, VDS, VT, GMSAT, GMLIN, VDSAT, VSAT, 3QS*, X, VDMX, K2, K3QS*, X, VDMX, K4, VDSATP, IDMX, R, WI, LL, VS1, VD1 4, VINP, K1, RP, X1, KL, LMIN, VOP, KPRIME, CPNO 5, VOI, VOF, VT, DT, DVD, CPN, CMOS, CL, D, B1, B2, B3, B4, VTO 6, T1, TOS, INC, GMS, GML, ML, MP0, MPEFF, IDSAT, LDEP, LDEPF 7, TEMP, C1
INTEGER I, J, K, IFIRST, KPRINT, DEBUG
C——STATEMENT DEFINITIONS

IDLIN(WL, LG, VG, VS, MP, CO, VT, KS, EPSO, Q, CB, PHF)
2=(VG+VFB)*MP*CO*( (VG-VD-VS/2.) *VD- (VG-VD-VS/2.) *VS)
3=2.E6/(CO*3.)) *SORT((2.*KS*EPSO*Q*CB)* 4((SORT(VD+2.*PHF)*(VD+2.*PHF))-(SORT(VS+2.*PHF)) 5(VS+2.*PHF)) )

VFB(VG, VT, VFB, KS, EPSO, Q, CB, CO)
2=-VFB/VG- (KS*EPSO*Q*CB)/CO 3-(VG-VFB)/(KS*EPSO*Q*CB)*1.E12

GMSAT(I1, KS, TOX, KO, VGP, VDSAT, VD, L)
2=(1D*K5*K0*L*TOX*4*(VGP-VDSAT))*1.E-12/
3=(KS+L)*(2*(VDP-VGP)*4*(VGP-VDSAT))-KS*TOX*(VDP-VDSAT) 2=1.0/1.0*(KO*CO*VDP-VDP)

EMEFFF(VD, VS, VD, N, VG, VT, CO, KS, EPSO, ESO, MP)
2=(EMEFP/((VG-VD-VS*(CO+KS*EPSO)))*C1)*MP

IDSAT(ID, VD, VDSAT, VG, L, K0, KS, TOX, QS, CO, Q)
1=ID/1.0* ((KS*TOX)/KO)*(VD-VDSAT) 2=2*(VG+((QSS*Q)/CO)+(6*(VG-((OSS*Q)/CO)-VDSAT))/L)
LDEP(VD, VS, VG, VT, CO, KS, EPSO)
1=((KS*TOX)/KO)*(VD-VDSAT) 2=2*(VG-VG+((OSS*Q)/CO)) 3.6*(VG-((QSS*Q)/CO)-VDSAT))
MPEFF(VD, VS, VS, VG, VT, CO, KS, EPSO)
2=(VG-VG-5*(VD+VS))*(CO/(KS*EPSO)))

C——INITIALIZE RUN
VD=VD0
W=WI
L=LI
IFIRST=0
VSP=0.
K1=1./INCR
JMAX=K1
VP0=M-
VS=0.
VT=VTO
11 IF(VIN-VT=VD/2.)22,6,6
6 WRITE(6,8)VT
8 FORMAT( ' ' INPUT VOLTAGE LESS THAN THRESHOLD
2VOLTAGE=1.3.2)
STOP 10
2 CONTINUE
K1=2.E6/(C0*3.)*SQRT(2.*KS*EPSO*Q*CB)
C TEST STATEMENT FUNCTIONS
K2=(WL)*MP*C0
K3=((VG-VT-VD/2.)*VD-(VG-VT-VS/2.)*VS)
1 IF(DEBUG)9,9,10
10 CONTINUE
WRITE(6,12)K1,K2,K3
12 FORMAT( 'K1=10.3,5X,K2=1E10.3,5X,K3=1F10.3)
9 CONTINUE
VSAT=VSAT(VG,VT,VS,KS,EPSTO,Q,CB,C0)
J=0
1 IF(DEBUG)15,15,11
11 CONTINUE
WRITE(6,13)INCR,VMAX,WL,VG,VD,VS,MP
13 FORMAT( 'INCR,VMAX,WL,VG,VD,VS,MP=8E11.3)
WRITE(6,14)CO,VT,KS,EPSTO,Q,CB,PHF
14 FORMAT( 'CO,VT,KS,EPSTO,Q,CB,PHF=7E12.3)
15 CONTINUE
WRITE(6,15)INCR,VMAX,VLCO/(KS*EPSO)
16 IF(DEBUG)15,15,17
17 CONTINUE
WRITE(6,16)ESO,VG,VT,VD,VS,CO,KS,EPSTO,MP,VLCO
18 FORMAT( '16--10E11.3)
18 CONTINUE
IF(MPEFFF(VD,VS,VG,VT,CO,KS,EPSTO)-ESO)20,20,19
19 CONTINUE
MPO=MPEFF(VD,VS,VG,VT,CO,KS,EPSTO,ESO,MP)
20 CONTINUE
10=1D01(WL,VG,VD,VS,MPO,CO,VT,KS,EPSTO,Q,CB,PHF)
VDP=VDP=1D01*RD1*1.E-12
VSP=1D01*RS1*1.E-12
10=1D01(WL,CG,VDP,VS,MPO,CO,VT,KS,EPSTO,Q,CB,PHF)
A1(1)=VD
A2(1)=1D
1 IF(DEBUG)150,150,144
144 CONTINUE
WRITE(6,145)VD,1D,MPO
145 FORMAT( '145--VD,1D,MPO=1D10.3,4X,E10.3,4X,F10.3)
150  \( J=1 \)
151  \( I=I+1 \)
152  \( V_{0}=V_{0}+\text{INC}+V_{\text{MAX}} \)

C---CALCULATE TD, THEN CORRECT FOR RD1, RSI
153  \( \text{IF}(M_{\text{PEF}}(V_{0}, V_{S}, V_{G}, V_{T}, C_{0}, K_{S}, E_{P50})-E_{SO})=0 \) \( 154, 154, 154 \)
154  \( \text{CONTINUE} \)
155  \( M_{P0}=M_{\text{PEF}}(V_{0}, V_{SP}, V_{G}, V_{T}, C_{0}, K_{S}, E_{P50}, E_{SO}, M_{P}) \)
156  \( \text{CONTINUE} \)
157  \( \text{IF}(M_{\text{PEF}}(V_{0}, V_{S}, V_{G}, V_{T}, C_{0}, K_{S}, E_{P50})-E_{SO})=0 \) \( 157, 157, 157 \)
157  \( \text{CONTINUE} \)
158  \( M_{P0}=M_{\text{PEF}}(V_{0}, V_{SP}, V_{G}, V_{T}, C_{0}, K_{S}, E_{P50}, E_{SO}, M_{P}) \)
159  \( \text{CONTINUE} \)
160  \( A_{1}(I)=V_{0} \)
161  \( A_{2}(I)=10 \)
162  \( SLOPE=(A_{2}(I)-A_{2}(J))/(A_{1}(I)-A_{1}(J)) \)
163  \( A_{3}(I)=SLOPE \)
164  \( \text{IF}(V_{Q_{\text{SAT}}}=V_{0})=170, 156, 156 \)
165  \( \text{IF}(SLOPE)149, 149, 159 \)
166  \( C---\text{BACK UP ONE POINT BEFORE SLOPE}=0. \)
167  \( J=J-1 \)
168  \( V_{0}=V_{0}-\text{INC}+V_{\text{MAX}} \)
169  \( J=J \)
170  \( \text{GO TO } 198 \)

165  \( \text{IF}(SLOPE)149, 149, 159 \)
171  \( \text{CONTINUE} \)
172  \( \text{IF}(V_{\text{MAX}}-V_{0})=600, 600, 164 \)
173  \( \text{CONTINUE} \)
174  \( \text{IF}(\text{DEBUG})167, 167, 163 \)
175  \( \text{CONTINUE} \)
176  \( \text{WRITE}(3,100)1, A_{1}(I), A_{2}(I), A_{3}(I) \)
177  \( \text{FORMAT}(410)=I, A_{1}(I), A_{2}(I), A_{3}(I)=14, F10.3, 4X, 2E15.3) \)
178  \( \text{GO TO } 180 \)
C---EXIT FROM LINEAR REGION
179  \( \text{CONTINUE} \)
C---SAVE LINEAR REGION BOUNDARY POINT
180  \( K=1 \)
181  \( V_{Q_{\text{SAT}}}=-V_{0} \)
182  \( \text{IF}(\text{DEBUG})191, 191, 190 \)
183  \( \text{CONTINUE} \)
184  \( \text{WRITE}(3,190)J_{1}, K, V_{Q_{\text{SAT}}}, V_{Q_{\text{SAT}}} \)
185  \( \text{FORMAT}(410)=I, J_{1}, K, V_{Q_{\text{SAT}}}, V_{Q_{\text{SAT}}}=-216, 2E10.3) \)
186  \( \text{CONTINUE} \)
187  \( J_{1}=10 \)
188  \( J_{1}=K \)
200  \( J=1 \)
201  \( J=J+1 \)
202  \( V_{0}=V_{0}+\text{INC}+V_{\text{MAX}} \)
ID = IDSAT(T01, VD, VDSATP, VG, L, KO, KS, TOX, QSS, CO, Q)
LDEP = LDEPF(VD, VDSATP, VG, KO, KS, TOX, QSS, CO, Q)
A1(I) = VD + ID * RD1 * 1. E-12
A2(I) = ID
A3(I) = (A2(I) - A2(J)) / (A1(I) - A1(J))
P3(I) = LDEP
IF(VMAX - VD) 205, 205, 200
205 CONTINUE
C--MATCH FOR EQUAL SLOPE
I = K
J = J + 2
210 GDLIN = A3(I)
GDSAT = A3(J)
IF(GDSAT - GDLIN) 231, 231, 215
215 I = I - 1
IF(I = 1) 220, 220, 210
220 WRITE(6, 230) I, J
230 FORMAT('230 --> I = ', I4, ' J = ', I4)
GO TO 600
231 WRITE(6, 232) I, J
232 FORMAT('232 --> I = ', I4, ' J = ', I4)
GO TO 600
600 CONTINUE
RETURN
END
RATIO - MAIN PROGRAM

DIMENSION A1(1000), A2(1000), A3(1000), A4(1000)
REAL W, L, N, L1, WL, L, MP, CO, CB, VG, VFB, PHF, VD, KO, KS, VS,
1EPS0, VGP, GSAT, VDMX, K1, K2, K3, K4, Q, EPS0, PHF, TOX, IDLIN, ID, VDS,
2VTO, GMSAT, GMLIN, VDSAT, VSAT, QSS, X1, VDDMX, VDSATP, IDMX, R,
3VDL, VSL, VDOUT, VNP, RP, KI, KL, L1L, L2L, DEBUG, VTO,
4MPF, VD, VS)

INTEGER R, J, K

COMMON QSS, MP, CO, CB, VFB, PHF, KO, KS, EPS0, Q, EPS0, PHF, TOX, RDI,
1RS1, RDL, RSL, VDD, VGG, K1, K2, K3, K4, WI, LJ, WL, LI, DEBUG, VTO,
2LMIN, KPRIME, INCR, TMAX, ESO, C1

C-STATEMENT DEFINITIONS

1DLIN(WL, VG*VD, VS, MP, CO, VT, KS, EPS0, Q, CB, PHF)
2=(W/L)*MP*C0*(((VG-VT-VD/2.)*VD-((VG-VT-VS/2.)*VS)
3=(2.E6/(C0*3.))*SQRT(2.*KS*EPS0*Q*CB)*
4=(SQRT(VD+2.*PHF)*(VD+2.*PHF))-(SQRT(VS+2.*PHF)*
5=(VS+2.*PHF))

VSAT(VG, VT, VFB, KS, EPS0, Q, CB, CO)
2=VG-VT-(KS*EPS0*Q*CB/CO**2)*(1.-SQRT(1.+2.E-12*CO**2*
3/(VG-VFB)/KS*EPS0*Q*CB)/1.E12)

GMSAT(1D, KS, TOX, KO, VGP, VDSAT, VS)
2=(1D*K5*K0*V8*TOX*4*(VGP-VDSAT))/
3*(K0*KS**2*(VD-VGP)+4*(VGP-VDSAT)-KS*TOX*(VD-VDSAT))**2

VG(1D, WI, MP, CO, VD, VS, VT, PHF, K1)
2=(W/L)*MP*C0*(((VD-VGP)+4*(VGP-VDSAT)-KS*TOX*(VD-VDSAT))/2
3=K1*((VD+2.*PHF)*SQRT(VD+2.*PHF)-(VS+2.*PHF)*SQRT(VS+2.*
4PHF)))/(VD-VS)

C-INITIALIZE RUN

TEMP=300.
MP=190.
CB=1.E-15
VFB=3.68-(TEMP-300.)*(0.004)
PHF=.3
VDD=15.
VGG=27.
KO=4.5
KS=12.
ES0=6.4+4
EPS0=0.085
C1=.26
Q=1.6*1E-19
EPS0X=.396
TOX=.1E-4
VTO=VFB+2.*PHF
LMIN=.18/394.
CO=EPS0X/TOX
VS=0.
QSS=5.E11
RDL=100.
RSL=400.
RD1=4.
RSt=4.
INCR=.01
KPRIME=.3075E7
WI=26.4/394.
LI=.2/394.
WL=1.4/394.
LL=.33/394.
CPNO=2.
CMOS=1.
DEBUG=0.

5 CONTINUE
WRITE(6,8)
8 FORMAT('VIN' T11' VOUT')
READ(5,10) VIN, VOUT
10 FORMAT(2F10.5)
CALL RATIO(VIN, VOUT)
WRITE(6,20)
20 FORMAT(' 1D(PA)' ,4X, 'W',9X,' L',9X,' VD',8X,' VS',8X,' 2 MP0')
GO TO 5
STOP 888
END
SUBROUTINE FOR RATIO

SUBROUTINE RATIO(VIN,VOUT)
C—THIS PROGRAM FINDS K1/KL FOR A SPECIFIED VIN AND VOUT
COMMON QS,MP,CO,CB,VFB,PHF,K0,KS,EPSO,Q,EPQ,TOX,ROI,RSJ,
1ROL,RSQ,VDU,VP,GX,K1,K2,K3,K4,W1,L1,WL,LL,DEBUG,VT0,LMIN,
2KPRIME,INCR,TMAX,ES0,C1
DIMENSION A1(510),A2(510),A3(510)
REAL w/L,MP,CO,CB,VT0,PHF,VP,K0,VS,KS,EPSO,VP,GX
2Q,EPQ,TOX,VDU,1D,VDV,VT,GMSS,GMSSAT,GMSSAT,VSAT,GSAT,x,
3,K2,K3,K4,VDSAT,1DMX,R,W1,L1,VS1,VMX,1K1,VTDMX,VTI
4,VOUT,INCR,MP0,MPF,WL,LL,1K1,1L,LMIN
INTEGER 1,J,K
C—STATEMENT DEFINITIONS
1DLIN(w/L,VT0,VP,CO,CB,VT,KS,EPSO,VP,GSAT)
2=(w/L)*MP*CO*((VP-VP0)*VP-(VP-VP0)*VP0)*VP
3-(2.E6/(CO*3.*))**SORT(2.*KS*EPSO*Q*CB)*
4((SORT(VP+2.*PHF)*(VP+2.*PHF))-SORT(VP+2.*PHF)*
5((SORT+2.*PHF)))+
VSAT(VP0,VP0,VP,CO,KS,EPSO,VS)
2=VP0-VP0-(KS*EPSO*Q*CB/CO)**(1.1-SORT(1.+2.E-12*C0*2.*)
3*(VP-VP0)/KS*EPSO*Q*CB)**(1,E2)
VGF(IO,MP0,CO,VP,VT,PHF,K1)
2=(IO/(w/L)*MP0*(VP-VS))-*(VP-VS)*VS**2/2.-VS**2/2.
3-K1*((VP+2.)*PHF)**SORT(VP+2.*PHF)*SORT(VP+2.*
4PHF)))/(VP-VS)
MPF(VP,VP0,VP,CO,KS,EPSO,ES0,MP)
2=((ES0/((VP-VP0)**2*(CO/(KS*EPSO))))**C1)*MP
MPFDD(VP0,VP,VP0,VP,CO,KS,EPSO)
2=(VP0-VP0)**(CO/(KS*EPSO))
C—INITIALIZE RUN
V0=VP0
VP=VP0
1=0
w=WL
MP0=MP
L=LL
VT=VT0
K1=(2.E6/(CO*3.))**SORT(2.*KS*EPSO*Q*CB)
KL=w/L
VP0=VOUT
V0=VP0
K1=(2.E6/(CO*3.))**SORT(2.*KS*EPSO*Q*CB)
WRITE(6,13)VIN,VOUT
13 FORMAT ('13—VIN>VOUT=2F10.3)
20 CONTINUE
C—CALCULATE 1D,VP FROM VP=VP0 TO VP=0.
1F(V0)38,36,21
21 VS=V0
IF (MPEFF (V0, VS, VG, VT, CO, KS, EPSO) - ESO) > 24.24,22
CONTINUE
MPO = MPEFF (V0, VS, VG, VT, CO, KS, EPSO, ESO, MP)
GO TO 26
MPO = MP
CONTINUE
IF (MPEFF (V0, VS, VG, VT, CO, KS, EPSO, Q, CB, PHF))
GO TO 2b
CONTINUE
MPO = MP
CONTINUE
10 = IF (V0 < 10 * RDL = 1, E-12)
A1 (1) = V0 + 10 * RDL = 1, E-12
A2 (1) = 10
J = J + 1
IF (DEHP=10) 20, 20, 31
CONTINUE
WRITE (32) V0, 10, 1
FORMAT (132 = V0 = 'E10.5x, 10 = 'E10.3, 5x, 'J = '13)
GO TO 20
CONTINUE
C - 10 IS FOUND FOR A SPECIFIED VO
V0 = V0P
IF (A1 (1) = V0) 43, 50, 42
10 = A2 (1)
GO TO 50
X = A1 (1)
J = 1
J = J + 1
GO TO 40
CONTINUE
10 = ABS (V0 - X) / V0)
J2 = ABS (V0 - A1 (1)) / V0)
IF (J1 = J2) 46, 58, 58
THE OPERATING POINT, I AND V0, IS FOUND
10 = A2 (J)
J = J
GO TO 50
10 = A2 (1)
GO TO 50
CONTINUE
C - V1N IS FOUND FOR AN ASSUMED K1 = 1, A VALUE LOWER THAN USED.
WRITE (52) 10, 1, MPO, A1 (1)
FORMAT (52 = 10 = 'E10.4, 5x, '1 = '13, 'MPO = ', 'F10.3, 'A1 (1) = 'K1 = 1,
VS1 = RS1 * 10 * 1. E-12
V01 = V0 - RD1 = 10 * 1. E-12
V1NP = VGF (10, 1, 1, MP, CO, VDI, VSI, VT, PHF, K1)
IF (MPEFF (V0, VS, VG, VT, CO, KS, EPSO) - ESO) > 56, 56, 54
CONTINUE
MPO = MPEFF (V0, VS, V1NP, VT, CO, KS, EPSO, ESO, MP)
CONTINUE
VINP=VGF(ID,1.1.,MPO,CO,VDI,VSI,VT,PHF,K1)
C—TEST FOR ERROR, VIN(CALC) WILL BE HIGHER THAN VIN(SPECIFIED)
X=ABS(((VINP-VIN)/VIN)
IF(DEBUG)64,64,60
60 WRITE(6,61)X, VINP, VIN, MPO, KI
61 FORMAT(' 61—X, VINP, VIN, MPO, KI=,5E12.3)
64 CONTINUE
IF(X-.05)300,300,65
65 R=VINP/VIN
C—K1 IS CORRECTED UNTIL VIN(CALC)=VIN(SPECIFIED)
KI=K1*R
IF(DEBUG)66,66,66
66 CONTINUE
WRITE(6,67)R, KI, X, VINP
67 FORMAT(' 67—R, KI, X, VINP=,4F10,4)
68 CONTINUE
X=ABS(1.-R)
IF(X-.05)300,300,70
70 K1=K1*.95
71 VI=LMIN*K1
VINP=VGF(ID,1.1.,LMIN,MP,CO,VDI,VSI,VT,PHF,K1)
IF(MPEFF(VOI,VSI,VINP,VT,CO,KS,EPS0)-EPS0)72,72,71
71 CONTINUE
MPO=MPEFF(VOI,VSI,VINP,VT,CO,KS,EPS0,ES0,MP)
72 CONTINUE
VINP=VGF(ID,1.1.,MPO,CO,VDI,VSI,VT,PHF,K1)
RP=VINP/VIN
X=ABS(1.-RP)
IF(DEBUG)75,75,78
75 CONTINUE
WRITE(6,77)RP, KI, X, VINP
77 FORMAT(' 77—RP, KI, X, VINP=,E10.4,E10.4,E10.4,E10.4,E10.4)
78 IF(X-.05)300,300,80
80 X1=ABS(1.-R)
IF(X1-X)70,200,200
C—1ST ITERATION TO INITIALIZE
EPS0=1.E+20
200 K1=K1*1.01
2001 VI=LMIN*K1
IF(DEBUG)201,201,2001
2001 WRITE(6,2002)K1, VI, ID, MPO, VDI, VSI, VT, K1
2002 FORMAT(' 2002—K1, VI, ID, MPO, VDI, VSI, VT, K1=,6E11.4)
2001 CONTINUE
VINP=VGF(ID,1.1.,LMIN,MP,CO,VDI,VSI,VT,PHF,K1)
RP=VINP/VIN
X=ABS(1.-RP)
IF(DEBUG)205,205,2005
205 CONTINUE
WRITE(6,207)RP, KI, X, VINP
207 FORMAT(' 207—RP, KI, X, VINP=,4E12.4)
C--INCREMENT (.001) SETS THE ACCURACY
209  IF(X=.001)300,300,210
210   K1=K1*1.01
      W1=LMIN*K1
C--ITERATE FOR SOLUTION OF VIN
211  DO N=1,5
212    VINP=VGF(10,W1,LMIN,MPO,CO,VD1,VS1,VT,PHF,K1)
213    IF(MPEFFD(VD1,VS1,VINP,VT,CO,KS,ESO)-ESO)231,231,230
214     CONTINUE
215    MP0=MPEFF(VD1,VS1,VINP,VT,CO,KS,ESO,ESO,MP)
216     GO TO 232
217  CONTINUE
218  CONTINUE
219  IF(DEBUG)250,250,241
220    WRITE(6,242)W1,MPO,VINP,RP,K1,X,VD1,VS1
221     FORMAT('242--W1,MPO,VINP,RP,K1,X,VD1,VS1=','1E11.4)
222  CONTINUE
223  CONTINUE
224    VINP=VGF(10,W1,LMIN,MPO,CO,VD1,VS1,VT,PHF,K1)
225    RP=VINP/VIN
226    IF(RP=1.001)300,300,211
227     CONTINUE
228    X=ABS(1.-RP)
229    X1=ABS(1.-R)
230    IF(DEBUG)209,209,213
231  CONTINUE
232    WRITE(6,217)RP,K1,X,VINP,X1
233     FORMAT('217--RP,K1,X,VINP,X1=','2E15.4)
234     GO TO 209
235  CONTINUE
236    W1=LMIN*K1
237    R=K1/KL
C--DEVICE DIMENSIONS MUST BE CORRECTED FOR MASK DEFINITION
238    WRITE(6,310)R,W1,LMIN,KL,VO,VIN,MPO,K1
239    FORMAT('310--R,KL,W1,LMIN,KL,VO,VIN,MPO,K1=','1E10.3)
240    RETURN
241    END
DISCHARGE - MAIN PROGRAM

C--THIS IS THE MAIN EXECUTIVE PROGRAM

DIMENSION A1(1000), A2(1000), A3(101), Z1(10),
2XI(10,100), YI(10,100)

REAL W, WI, WL, LI, WL, LL, MP, CO, CB, VG, VFB, PHF, VD, KO, KS, VS, EPSO,
1VG, GSA, VGMX, K1, K2, K3, K4, Q, EPS0, TOX, IDLIN, ID, VDS, VT, VTO,
2GMSAT, GMLIN, VDSAT, VSAT, EPSX, X1, VDDMX, VDSATP, IDMX, R, VDI, VSL,
3VDL, VSL, VSAT, VOUT, VIN, RP, K1, KL, LMIN, VOP, INCR, KPRIME, MPO, MPRE,
4, TEMP, C1

INTEGER I, J, K

COMMON QSS, MP, CO, CB, VFB, PHF, KO, KS, EPSO, Q, EPS0, TOX, R01,
1R51, RDL, RSL, VDD, VGG, K1, K2, K3, K4, W1, L1, WL, LL, DEBUG, VT0,
2LMIN, KPRIME, INCR, TMAX, EPS0, VIN, TEMP, C1

C--STATEMENT DEFINITIONS

IDLIN(WL, VG, VS, MP, CO, VT, KS, EPS0, Q, CB, PHF)

2=(W/L)*MP*CO*( (VG-VT-VD/2.)*VD-(VG-VT-VS/2.)*VS)
3=(2.E6/(CO*3.))*SQR(2.*KS*EPS0*Q*CB)*
4((SQR(VV+2.*PHF)*(V0+2.*PHF))-(SQR(VS+2.*PHF)*
5(VS+2.*PHF)))

VSAT(VG, VT, VFB, KS, EPS0, Q, CB, CO)

2=VG-VT- (KS*EPS0*Q*CB/CO**2) * (1.- SQR(1.+2.E-12*CO**2*
3(VG-VFB)/KS*EPS0*Q*CB)*1.E12)

GMSAT(ID, KS, TOX, KO, VGG, VDSAT, VD, L)

2= (10*KS*K0*L1/TOX, 4*(VGP-VDSAT))/
3(K0*L1/(10*KS*K0*L1/TOX, 4*(VGP-VDSAT)))*KS*TOX*(VD-VDSAT))**2

VG(VD, W, L, MP, CO, VT, KS, EPS0, Q, CB, PHF, K1)

2=(W/L)*MP*CO*(VD-VG)*
3(K0*L1/(10*KS*K0*L1/TOX, 4*(VGP-VDSAT)))*KS*TOX*(VD-VDSAT))**2

C--INITIALIZE RUN

C--PROCESS CONSTANTS

TEMP=300.
CB=2.E15
MP= (190.)/( (TEMP/300.)*SQR(TEMP/300.))
DEBUG=0.
VFB=3.68
PHF= 3
C1= .22
WI= 26.4/394.
L1= .2/394.
WL= 1.4/394.
LL= .32/394.
CMOS= 9.E+3
CPNO=0.
VIN=10.
V01= 14.8
VOF= .985
KO= 4.5
VDD= 15.
VGG=27.
RDL=100.
RSL=400.
RD1=4.
RS1=4.
RDL=75.
RSL=75.
RD1=4.
RS1=4.
XL=0.
XH=1.0
YL=0.
YH=VOI
NCASE=1
NCASES=1
NCRV=5
KS=12.
EPSD=.0885
Q=1.6E-19
ESD=6.6E+4
EP0X=.398
TOX=.1E-4
VT0=VFB+2.*PHF
C0=EP0X/TOX
QSS=5.E11
INCR=.01
KPRI=ME=(MP*EP0X)/(2.*TOX)
TMAX=100.
WRITE(10,20)NCASES
20 FORMAT(12)
CP=CPNO
CM=CMOS
VGX=VIN
CPX=CPNO
CMX=CMOS
WRITE(6,30)VOI,VOF,CPNO,CMOS,VIN
30 FORMAT(1 30=VOI,VOF,CPNO,CMOS,VIN=',5E12.4)
CALL DISCH(VOI,VOF,CPX,CMX,VGX,TDCH)
WRITE(6,40)TDCH,VOI,VOF
40 FORMAT(* DISCH TIME=',E10.4,' US, VOI=',F6.3,', VOF='
STOP 888
END
SUBROUTINE FOR DISCHARGE

SUBROUTINE DISCH(VOF, VOF, CPX, CMX, VG, TOCH)
COMMON QSS, MP, CO, CB, VFB, PHF, KO, KS, EPSO, Q, EPOX, TOX, RDI, RS1,
1RD1, RSL, VDD, VG, K1, K2, K3, K4, WI, LT, WL, LL, DEBUG, VT0, LMIN,
2KPRIME, INCR, TMP, ESQ, VIN, TEMP, C1
DIMENSION A1(1001), A2(1001), A3(1001), P1(101), P2(101),
REAL W, LP, MP, CO, CB, VG, VFB, PHF, VD, KO, KS, EPSO, VGF, GSAI,
Q, EP0X, TOX, IDLIN, ID, VDS, VT, GMSAT, GML1N, VDSAT, VSAT, QSS, K1,
K2, K3, K4, VDSATP, IDMX, R, WI, LI, VSI, VDI, VG, CMX, K1, VDDMX,
4, VIN, K1, RP, X, KL, LMIN, VIN, KPRIME, CPNO,
5, VOF, VOF, DT, DV, CPN, CMOS, CL, D, B1, B2, B3, B4, VT0,
6, ID1, IDS, INCR, GMS, GML, MP, MPEFF, IDSAT, LDEP, LDEPF,
7, TEMP, C1, IDL, IDT, MP01, MP0L, WL, LI.
8, 102
INTEGER J, K, I, IFIRST, KPRINT, DEBUG
C---STATEMENT DEFINITIONS
IDLIN(W, L, VD, VS, MP, CO, VT, KS, EPSO, Q, CB, PHF)
2= (W/L)*MP*CO* ((VG- VT- VS/2.)*VD- (VG- VT- VS/2.)*VS)
3= (2.66/(CO*3.))*SQRT(2.*KS*EPSO*Q*CB)*
4= ((SQRT(VD+2.*PHF))*(VD+2.*PHF)) - (SQRT(VS+2.*PHF))
5= (VS+2.*PHF))
VSAT(VG, VT, VFB, KS, EPSO, QT, CB, CO)
2=VG- VT- (KS*EPSO*Q*CB/C0**2) *(1. - SQRT(1. + 2.E-12*C0**2))
3= (VG- VFB)/KS*EPSO*Q*CB)*1.E12
GMSAT(ID, KS, TOX, KO, VGF, VDSAT, VD, L)
2= (ID*KS*K0*L*TOX*4(VGF- VDSAT))**1.E-12/
3= (KS*TOX*(VGF- VDSAT))**2
VGIF(ID, W, L, MP, CO, VD, VS, VT, PHF, K1)
2= (ID/((W/L)*MP*CO*(VD- VS))) - (VT*(VS- VD)+ VS**2/2.- VD**2/2.
3= K1*( (VD+2.*PHF)) - SQRT(VD+2.*PHF)* (VS+2.*PHF)* SQRT(VS+2.*
4PHF)) / (VD- VS)
MPEFF(VD, VS, VG, VT, CO, KS, EPSO, ESQ, MP)
2= (ESQ/((VG- VT- 5*(VD+VS)))*(CO/(KS*EPSO)))**C1)*MP
IDSAT(ID, VD, VDSAT, VG, L, KO, KS, TOX, QSS, CO, Q)
1= (ID/1. - (KS*TOX/K0)*(VD- VDSAT)) /
2= (2*(VD- VG+((QSS*Q)/C0)) + 6*(VG- ((QSS*Q)/C0)- VDSAT))/L
LDEPF(VD, VDSAT, VG, KO, KS, TOX, QSS, CO, Q)
1= ((KS*TOX/K0)*(VD- VDSAT))/
2= (2*(VD- VG+((QSS*Q)/C0)) +
3= 6*(VG- ((QSS*Q)/C0)- VDSAT))
MPEFFD(VD, VS, VG, VT, CO, KS, EPSO)
2= ((VG- VT- 5*(VD+VS)))*(CO/(KS*EPSO))
1= 0.
CPNO=CPX
CMOS=CMX
VT=VT0
VIN=VG
VD1=0.
K1= (2.66/(CO*3.))*SQRT(2.*KS*EPSO*Q*CB)
VDSAT=VSAT(VIN,VT,VFB,KS,EP50,Q,CB,CO)
VSI=0.
WRITE(6,40)
40 FORMAT('1H1,T29,' 'DISCHARGE TIME CALCULATION'//
2,'25X,' 'TIME','4X,' 'VOLTS', '10X,' 'ID'"" //
1,'IF(DEBUG)50,50,48
48 WRITE(6,49)VIN,VOI,VOF,CPNO,CMOS,C0,ESO,MP,W1,K1
49 FORMAT(' 49','10E11.3)
50 CONTINUE
J=1
I=I+1
VDI=VDI+INCR*VSI
MPO=MPEFF(VDI,VSI,VIN,VT,CO,KS,EP50,ESO,MP)
10=IDLIN(WI,I,VIN,VDI,VSI,MPO,CO,VT,KS,EP50,Q,CB,PHF)
VSI=VSI+ID*RDI*1.E-12
50 CONTINUE
100 A1(I)=VDI
A2(I)=10
101 SLOPE=(A2(I)-A2(J))/(A1(I)-A1(J))
102 CONTINUE
103 WRITE(6,104),A1(I),A2(I),SLOPE,MPO,VDSAT
104 FORMAT(' 104 --- I, VO, SLOPE, MPO, VOSAT = 14, 5E12, 3')
107 CONTINUE
VOSAT=VSI+ID*RD*1.E-12
105 IF(VOSAT-VO)110,105,105
105 IF(VOSAT-VO)110,105,105
111 IF(SLOPE)106,106,50
106 I=I+1
101 A2(I)=10
102 CONTINUE
110 ID=10
CALL SLITE(I)
I=I+1
T=0.
105 VDL=VDI
VS=VSI
VSI=VSI+ID*RD*1.E-12
105 IF(VOSAT-VO)110,105,105
105 IF(VOSAT-VO)110,105,105
110 ID=10
CALL SLITE(I)
I=I+1
T=0.
105 VDL=VDI
VS=VSI
VSI=VSI+ID*RD*1.E-12
105 IF(VOSAT-VO)110,105,105
105 IF(VOSAT-VO)110,105,105
110 ID=10
CALL SLITE(I)
I=I+1
T=0.
105 VDL=VDI
VS=VSI
VSI=VSI+ID*RD*1.E-12
105 IF(VOSAT-VO)110,105,105
105 IF(VOSAT-VO)110,105,105
110 ID=10
CALL SLITE(I)
I=I+1
T=0.
105 VDL=VDI
VS=VSI
VSI=VSI+ID*RD*1.E-12
105 IF(VOSAT-VO)110,105,105
105 IF(VOSAT-VO)110,105,105
110 ID=10
CALL SLITE(I)
I=I+1
T=0.
105 VDL=VDI
VS=VSI
VSI=VSI+ID*RD*1.E-12
105 IF(VOSAT-VO)110,105,105
105 IF(VOSAT-VO)110,105,105
110 ID=10
CALL SLITE(I)
I=I+1
T=0.
105 VDL=VDI
VS=VSI
VSI=VSI+ID*RD*1.E-12
105 IF(VOSAT-VO)110,105,105
105 IF(VOSAT-VO)110,105,105
110 ID=10
CALL SLITE(I)
I=I+1
T=0.
105 VDL=VDI
VS=VSI
VSI=VSI+ID*RD*1.E-12
105 IF(VOSAT-VO)110,105,105
105 IF(VOSAT-VO)110,105,105
110 ID=10
CALL SLITE(I)
1211 CONTINUE
IDL=IDLIN(WL,LL,VGG,VDL,VSL,MP0,CO,VTO,KS,EPS0,Q,CB,PHF)
1212 CONTINUE
IF(EPS0=MPEFFD(VDI,VS1,VIN,VTO,CO,KS,EP50))122,123,123
122 CONTINUE
MP0=MPEFF(VDI,VS1,VIN,VTO,CO,KS,EP50,EPS0,MP0)
GO TO 1231
123 MP0=MP0
1231 CONTINUE
IDL=IDL(IN(WL,LL,VGG,VDL,VSL,MP0,CO,VTO,KS,EP50,Q,CB,PHF)
V0=V0+RSL*IDL*1.E-12
V0=V0-RDI*1.D1*1.E-12
V0=V0+RSL*IDL*1.E-12
V0=V0-RDI*1.D1*1.E-12
IF(DEBUG)195,195,191
191 WRITE(6,192)IDL,ID1,MP0,ID1,VDSAT
192 FORMAT(1M-192—ID1,MP0,ID1,VDSAT='5E12,3)
195 CONTINUE
199 DO 500 M=1,4
1 IF(IFIRST)200,250,200
C--T IS IN MICROSECONDS
200 T=DFEQ(T,DT,1.)
201 V0=DFEQ(V0,DV0,2.)
250 CONTINUE
1 IF(DEBUG)256,256,252
252 IF(M=4)256,254,
254 WRITE(6,255)DV0,V0,T
255 FORMAT(1M-255—DV0,V0,T='3E12,3)
256 CONTINUE
CL=CMOS+CPNO*(SQRT(0.6/(V0+.6)))
1 IF(EPS0=MPEFFD(V0,V0,V0,0,0,MP0,C0,VT,KS,EP50))257,258,258
257 CONTINUE
MP0=MPEFF(V0,V0,V0,0,0,MP0,C0,VT,KS,EP50,MP0)
GO TO 2581
258 MP0=MP0
25A1 CONTINUE
1 IF(EPS0=MPEFFD(VDI,VS1,VIN,VTO,CO,KS,EP50))261,262,262
262 MP0=MP0
GO TO 2621
261 CONTINUE
MP0=MPEFF(VDI,VS1,VIN,VTO,CO,KS,EP50,MP0)
2621 CONTINUE
C--SELECT FOR LINEAR OR SATURATION EQUATION...
1 IF(V0-VDSAT)260,260,270
260 ID1=IDLIN(WL,LL,VGG,VDL,VSL,MP0,CO,VT,KS,EP50,Q,CB,PHF)
GO TO 2A0
270 IF(V0-VDSAT)260,260,270
280 CONTINUE
1D1=IDLIN(WL,LL,VGG,VDL,VSL,MP0,CO,VT,KS,EP50,Q,CB,PHF)
DO 290 J=1,5
  VDL=VDD-IDL*RDL*1.E-12
  VSL=VO+IDL*RSI*1.E-12
  IDL=IDL*IN(WL,LL,VGG,VDL,VSL,MPOL,CO,VT,KS,EPSO,Q,CB,PHF)
  VDI=VO-IDI*RDI*1.E-12
  VSI=IDI*RSI*1.E-12
  IF(VO-VOSAT)272,272,278
272 IDL=IDL*IN(WL,LL,VIN,VDI,VSI,MPOL,CO,VT,KS,EPSO,Q,CB,PHF)
GO TO 279
276 IDL=IDSAT(ID1,VO1,VOSAT,VIN,LI,K0,KS,TOX,QSS,CO,G)
279 CONTINUE
  A3(J)=IDL
  P1(J)=ID1
290 CONTINUE
  DVO=((1DL-ID)/CL)
  DVO=DVO*1.E-6

C TEST FOR MINIMUM OUTPUT VOLTAGE
IF(IDL-ID1)500,499,499
499 DVO=0.
500 CONTINUE
  IF(DEBUG)495,495,491
491 CONTINUE
  WRITE(6,5000)ID2,(A3(I),P1(I),I=1,5)
5000 FORMAT(* 5000,'E12.3,5(2E10,3))
495 CONTINUE
  IF(DEBUG)505,505,501
501 WRITE(6,502)VDI,IDL,IDI,MPOL,MPOL
502 FORMAT(* 502,'VDI,IDL,IDI,MPOL,MPOL=5E12.3)
503 WRITE(6,503)B1,B2,B3,B4,CX,MPOL
503 FORMAT(* 503,'B1,B2,B3,B4,CX,MPOL=5E12.3)
505 CONTINUE
  IF(DEBUG)510,510,506
506 WRITE(6,507)VDL,VSL,VDI,VSI,VGG,VIN,VTO,CO,KS,MP
507 FORMAT(10E11.4)
510 CONTINUE
  IFIRST=1
  VDL=VDD-RDL*IDL*1.E-12
  VDI=VO-RDI*1.ID1*1.E-12
  VSL=VO+RSL*1.IDL*1.E-12
  VSI=RSI*1.ID1*1.E-12
  K=K+1
  IF(K-10)516,516,512
512 K=0
  WRITE(6,515)T,VO,ID1,IDL
515 FORMAT(T11,2F10.3,3X,2E10.3)
516 CONTINUE
  IF(VO=V0F)600,600,525
525  TDCH=T
     IF(T-TMAX)199,199,600
600  TDCH=T
     A1(1)=V0
     A2(1)=TDCH
     X1=1./JNCR
     JMAX=X1
     RETURN
     END
CHARGE - MAIN PROGRAM

C-- THIS IS THE MAIN EXECUTIVE PROGRAM

DIMENSION A1(101), A2(101), A3(101), A4(101), P1(101), P2(101)
REAL WL, W1, W1L, W1L, MP, CO, CB, VG, VFB, PHF, VD, KO, KS, VS,
1GSAT, VGMX, K1, K2, K3, K4, Q, EPOX, TOX, IMLIN, ID, VDS, VT,
2MLIN, VOSAT, VSA, QSS, X, K1, VDDSAT, VDSAT, VDMX, R, VDI, VSI,
3V0, VOUT, VIMP, K1, KL, LMIN, VOP, INCR, KPRIME, MPO, MPEFF
4, VTO, GMSAT, VDL, VSL, EPSO, VGP, TEMP, C1

INTEGER I, J, K
COMMON QSS, MP, CO, CB, VFB, PHF, KO, KS, EPSO, Q, EPOX, TOX, RDI,
1RS1, RDL, RSI, VDD, VG2, K1, K2, K3, K4, W1, W1L, W1L, DEBUG, VTO,
2, LMIN, KPRIME, INCR, TMAX, ESO, TEMP, C1

C-- STATEMENT DEFINITIONS

1MLIN(W, L, VG, VD, VS, MP, CO, VT, KS, EPSO, Q, CB, PHF)
2= (W/L)*MP*CO* ((VG- VT - VD/2.)*V0 - VG- VT - VS/2.)*VS
3= (2.E6/(CO*3.))*SORT(2.*KS*EPSO*Q*CB)*
4= (SORT(VD+2.*PHF)*(VD+2.*PHF) - (SORT(VS+2.*PHF)*
5= (VS+2.*PHF))
6= VSSAT(VG, VT, VFB, KS, EPSO, Q, CB, CO)
7= VG- VT - (KS*EPSO*Q*CB/C0**2)*(1.-SORT(V0-2.E-12*C0**2*
8= ID*KS*KO*L*TOX*M*(VGP-«VOSAT)/
9= ID*KS*KO*L**2*(VGP-VOSAT))/
10= (KS*EPSO*Q*CB)*1.12)

GMSAT(ID, KS, TOX, KO, VGP, VDSAT, VDL)
2=(10/((W/L)*MP*CO*(VQ-VS)/
3= KS*TOX*(VQ-VS))/
4= (VQ-VOSAT))
5= (VQ-VOSAT))/
6= VDD-15.
7= VG-27.
8= KO-4.5
9= KS-12.
10= TMAX=100000.
11= EPSO=.085
12= 0=1.6E-19
13= EPOX=-.398
14= TOX=-1.4E-4
15= ESO=6,E-4
16= VTO=VFB+2.*PHF
17= LMIN=.0004
18= CO=EPOX/TOX
19= VS=0.

C-- INITIALIZE RUN

CB=1.E15
VFB=3.68
TEMP=300.
MP=(190.)/(TEMP/300.)*SORT(TEMP/300.)
C1=.22
PHF=.3
VDD=15.
VG=27.
KO=4.5
KS=12.
TMAX=100000.
EPSO=.085
0=1.6E-19
EPOX=-.398
TOX=-1.4E-4
ESO=6,E-4
VTO=VFB+2.*PHF
LMIN=.0004
CO=EPOX/TOX
VS=0.
QSS=5.E11
RDI=4.
RSI=4.
RDOL=0.
RSL=0.
INCR=.01
KPRIME=ZMP*EP0X)/(2.*T0X)
M1=26.4/394.
L1=.2/394.
WL=1.4/394.
L2=.32/394.
CPNO=0.
CMOS=9.000.
DEBUG=0.
VOI=1.
VOF=14.8
VG=27.
CMX=CMOS
CPX=CPNO
CALL CHARGE(VG,VOI,VOF,CPX,CMX,T,VO)
WRITE(6,60)T,VO,VOI,VOF
60 FORMAT(• T=','E10.3,' VO=','E10.3,' VOI=','E10.3,' VOF=','
2E10.3)
R=WL/LL
WRITE(6,51)R,CMOS,CPNO,TEMP
51 FORMAT(• CHARGE TIME FOR LINEAR LOAD, R='F8.2,' CMOS=','
2F6.2,' CPNO='F6.2,' TEMPERATURE='F6.1,' DEGREES
3ABSOLUTE/)
SUBROUTINE FOR CHARGE

SUBROUTINE CHARGE(VG, VOI, VOF, CPX, CMX, TI, VO)
C--THIS PROGRAM FINDS THE TURN-ON (CHARGE) TIME FOR AN MOS GATE
COMMON QSS, MP, CO, CB, VFB, PHF, KO, KS, EPSO, Q, EPOX, TOX, RDJ,
1RS, RD, RS, SDL, VDD, VGG, K1, K2, K3, K4, WI, LI, WL, LL, DEBUG, VTO,
2LM, INKPRIME, INCR, TMAX, ES0, TEMP, C1
DIMENSION A(1000), A2(1000), A3(1000), AM(1000)
REAL W, L, MP, CO, CB, VG, VFB, KS, EPSO, VGP, GSAT,
20, EPOX, TOX, IDLIN, ID, VDS, VT, GMSAT, GMLIN, VDSAT, VSAT, QSS,
3, K2, K3, K4, VDSAT, IDMX, R, WI, LI, VS, VDI
4, VINP, K1, RP, X1, KL, MIN, VOP, KPRIME, CPNO, MP0, MPEFF
5, VOI, VOF, V0, TD, DVO, CPN, CMOS, CLD, B1, B2, B3, B4, VTO
6, TEMP, MPEFFD, C1, IDL, ID1, LI.
7, VGMX, K1, X, VDDMX
INTEGER I, J, K, IFIRST, KPRINT
C--STATEMENT DEFINITIONS
IDLIN(W, L, VG, VD, VS, MP, CO, VT, KS, EPSO, Q, CB, PHF)
2= (W/L) + MP + CO + ((VG-VT-VD/2) + VS) / (VG-VT-VS/2)*VS)
3-(2,E6/(CO*3.))*SQR(2,KS*EPS0*Q*CB)*
4(((SQR(VD+2,*PHF) + (VD+2,*PHF)) - (SQR(VS+2,*PHF))
5(VS+2,*PHF)) )
VSAT(VG, VT, VFB, KS, EPSO, Q, CB, CN)
2= VG+VT-1(KS*EPSO*Q*CB/CO**2) * (1+-(SQR(1.2*EPSO**2))
3(VG-VFAB) / KS*EPSO**2*CB)*1, E12)
GMSAT(ID, KS, EPSO, VPP, VT, PF, K1)
2= (ID/KS*KN*LT*TOX*.L*(VGP-VDSAT)) / (K1*K2*VGP-VDSAT)
3(KO* KN*LT*TOX*.L*(VGP-VDSAT)) - KS*TOX*(VGP-VDSAT)**2
VGFA(VD, W/L, MP, CO, VS, VT, PHF, K1)
2= (K2*0.2*VGP-VDSAT) - (VGP-VDSAT) / (VGP-VDSAT)
3(KO* KN*LT*TOX*.L*(VGP-VDSAT)) - (VGP-VDSAT)**2
MPEFF(VG, VS, VG, VT, CO, KS, EPSO, ES0, MP)
2= (EPS0/(VGP-VD-VS)) * (EPS0/(KS*EPSO))**C1*MP
MPEFFD(VG, VS, VG, VT, CO, KS, EPSO)
2= ((VGP-VT-5*(VGP-VS)) * (CO/(KS*EPSO))
C--INITIALIZE RUN
w=W, L=L,
N=0
VT=VTO
MP0=MP,
VS=0,
CPNO=CPX
CMOS=CMX
VDD=VDD
WR1TE(6, 8)
8 FORMAT(1H1, TI6, 'CHARGE TIME CALCULATION'/,
2, 25X, 'TIME', 6X, 'VOLTS', 12X, 'DVO')
K1=(2,E6/(CO*3.))*SQR(2,KS*EPS0*Q*CB)
IF (DEBUG) 13, 13, 9
CONTINUE
WRITE (6, 12) K1, KS, EPSO, Q, CB, WI, WL, LL, VG, VT, VD, VS
FORMAT (' 12- ', 13E9.3)
CONTINUE
K1 = (-L) * KPRIME
CALL GLITE(1)
IF (FIRST) = 0
T = 0.
VD = VD0
VS = V0
IF (MPEFFE (VD, VS, VG, VT, CO, KS, EPSO) = ESO) 16, 16, 14
CONTINUE
MPE = MPEFE (VD, VS, VG, VT, CO, KS, EPSO, ESO, MP)
CONTINUE
ID = IDLIN (W, L, VS, VD, VS, MPO, CO, VT, KS, EPSO, Q, CB, PHF)
VD = VD0 - ID * ROL * 1. E-12
VS = V01 + ID * ROL * 1. E-12
ID1 = ID
ID = IDLIN (W, L, VS, VD, VS, MPO, CO, VT, KS, EPSO, Q, CB, PHF)
IF (DEBUG) 82, 82, 75
WRITE (6, 80) VD, VS, ID1, ID
FORMAT (', 80 - VD, VS, ID1, ID = ', 12E10.3, 2E10.3)
C-TIME IS IN MICROSECONDS
82 DT = 1.
KPRINT = 1
VD0 = 0.
IF (DEBUG) 85, 85, 83
WRITE (6, 84) VD, VD0, CPNO, CMOS, VG, VT
FORMAT (' VD, VD0, CPNO, CMOS, VG, VT = ', 6E12.3)
CONTINUE
CONTINUE
DO 400 M = 1, 4
IF (FIRST) = 200, 30, 200
200 T = DIFEQ (T, DT, 1.)
CONTINUE
IF (V0) 201, 202, 202
CONTINUE
CPNO = (SORT (.6) + CPNO) / SORT (.6 + VO)
CONTINUE
WRITE (6, 203) TCL, KL, DVO
FORMAT (' 203 = ', 4E12.3)
CONTINUE
CL = CMOS + CPNO
WRITE (6, 305) CL, 305, 301
FORMAT (' 305 = ', 6E12.3)
CONTINUE
IF (MPEFE (VD, VS, VG, VT, CO, KS, EPSO) = ESO) 310, 310, 306
306 CONTINUE
MPD=MPEFF(VD,VS,VG,VT,CO,KS,EP50,ES0,MP)
GO TO 3101
310 MPD=MP
3101 CONTINUE
IDL=IDL1N(WL,VL,VD,VO,MPD,CO,VT,KS,EP50,Q,CB,PHF)
IDL=IDL
DO 320 J=1,5
VDL=VDO*IDL*RD*1.E-12
VSL=VD+IDL*RS*1.E-12
NN=0
IF(VDL)3000,3001,3001
3000 NN=1
3001 IF(VSL)3002,3003,3003
3002 NN=1
3003 IF(NN)3010,3010,3005
3005 WRITE(6,3006)IDL,VDL,VSL,RDL,RSL,T
3006 FORMAT(6E12.3)
STOP 3009
3010 CONTINUE
IDL=IDL1N(WL,VL,VD,VO,MPD,CO,VT,KS,EP50,Q,CB,PHF)
A4(J)=IDL
320 CONTINUE
VDO=(1./CL)*IDL
VDO=VDO*1.E-6
400 CONTINUE
IF(DEBUG)410,410,401
401 CONTINUE
321 FORMAT(6E12.3)
WRITE(6,323)WL,VL,VDL,VSL,MPD,CO,VT,KS,EP50,Q,CB,PHF
323 FORMAT(13E8.2)
IF(DEBUG)410,410,405
405 WRITE(6,406)VD,VS,VT,VDL,VSL,CL,VO,MPD,CO,VT,KS,EP50,Q,CB,PHF
406 FORMAT(7F10.3,E10.3,F10.3,2E10.3)
410 CONTINUE
IFIRST=1
NN=NN+1
IF(N=2)476,476,408
408 N=0
WRITE(6,411)T,VD,VDO
411 FORMAT(T21,2F10.3,10X,E10.3)
476 CONTINUE
IF(VD=VDF)475,475,600
475 IF(T>TMAX)100,100,600
600 CONTINUE
RETURN
END
DATA SUBROUTINE FOR CALCOMP 765 PLOTTER

SUBROUTINE PLOTHC (NCRV, X1, X2, VGMIN, VGMAX, TEMP, XI, XH, YL, YH, Z1, X1, Y1)

DIMENSION XI(10), X1(10, 100), Y1(10, 100)
REAL LI, X1, Y1, YL, YH
ZERO = 0.0
I = 0

20 CONTINUE
I = I + 1
DO 25 M = 1, 100
WRITE (10, 21) Z1(I), X1(I, M), Y1(I, M)
21 FORMAT (3E12.6)
25 CONTINUE
IF (I - NCRV) 20, 24, 24
CONTINUE
WRITE (10, 26) ZERO
26 FORMAT (E12.3)
WRITE (10, 27) X1, X2, VGMIN, VGMAX, TEMP
27 FORMAT (T8, ' MOS DRAIN CURRENT CHARACTERISTIC/', 1, T11, ' L=', 'F6.3', ' MILS, K=', 'F8.3', /
2, ' GATE VOLTAGE VARIES FROM', 'F5.1', ' TO', 'F5.1', /
3, ' TEMPERATURE=', 'F5.1', ' DEGREES ABSOLUTE')
WRITE (10, 30) XI, XH, YL, YH
30 FORMAT (2F10.0, T5, 'DRAIN VOLTAGE (VOLTS)'/
12F10.0, T5, 'DRAIN CURRENT (UA)')
RETURN
END
APPENDIX II

REFERENCE DEVICE MANUFACTURER'S SPECIFICATION
SPECIFICATION LIST FOR ULO3C

Adapted from July, 1969 published specification from American Micro-Systems, Inc. 3800 Homestead Road, Santa Clara, California. Test conditions are for 25 C, Load - 10 MΩ.

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Dissipation</td>
<td></td>
<td>635</td>
<td>mW</td>
</tr>
<tr>
<td>Drain Voltage ($V_{DD}$)</td>
<td>-12.</td>
<td>-18.</td>
<td>Volts</td>
</tr>
<tr>
<td>Clock Voltage ($V_{GG}$)</td>
<td>-24.</td>
<td>-30.</td>
<td>Volts</td>
</tr>
<tr>
<td>Propagation Delay (1)</td>
<td></td>
<td>100 (typical)</td>
<td>Nanoseconds</td>
</tr>
<tr>
<td>Input 1 Level</td>
<td>-9.</td>
<td></td>
<td>Volts</td>
</tr>
<tr>
<td>Input 0 Level</td>
<td>-3.5</td>
<td></td>
<td>Volts</td>
</tr>
<tr>
<td>Output 1 Level (1)</td>
<td>-10.</td>
<td></td>
<td>Volts</td>
</tr>
<tr>
<td>Output 0 Level (1)</td>
<td>-2.5</td>
<td></td>
<td>Volts</td>
</tr>
<tr>
<td>Output ON Resistance to ground</td>
<td>300 (typical)</td>
<td></td>
<td>Volts</td>
</tr>
<tr>
<td>Output Load Resistance (2)</td>
<td>2.0 (typical)</td>
<td></td>
<td>K</td>
</tr>
</tbody>
</table>

Conditions:
(1) $V_{DD} = -15v$, $V_{GG} = -27v$
(2) $V_{DD} = -15v$, $V_{GG} = -27v$, $V_{out} = 0v$. 
BIBLIOGRAPHY


