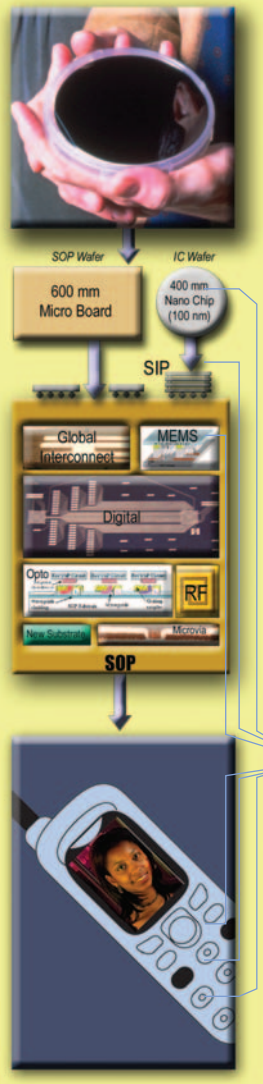
Microsystems Packaging Research Center

Distinguished Lecture Series

ELECTROSTATIC PROTECTION FOR SEMICONDUCTOR ELECTRONICS

Dr. Charvaka Duvvury
Texas Instruments Fellow, Silicon Technology Dept., Dallas, Texas

Monday, January 28, 2008 • 2:00 p.m. - 3:00 p.m.
Klaus Building 1116E, 266 Ferst Drive, Atlanta, GA, 30332, U.S.A.



Abstract:

Electrostatic-Discharge (ESD) is a particular concern for electronic semiconductor chips used in consumer, medical and military applications. Most people do not realize that when touching a chip or connecting a USB cable one can potentially damage the Integrated Circuit (IC) chip. The energy delivered by human handling or cable discharge can cause unexpected computer and electronic system failures. Understanding of this phenomena, controlling it at IC production and assembly sites, and designing circuits at the IC pins for harmlessly dissipating this energy threat is becoming extremely important for the future of technologies where the transistors are becoming more and more delicate. Demands for faster circuit performance and rapid advances in the IC packaging technology are further adding to the protection design constraints. This seminar will first outline the nature of ESD, the impact of technology advances, the challenges faced by the IC designers, and the specific package development issues that further restrict the ESD design. The package development work at Georgia Tech is especially important for these considerations. The seminar will identify the areas of package technology challenges and new areas of required innovation to maintain ESD reliability.

About the Presenter:

Charvaka Duvvury is a Texas Instruments Fellow working in the Silicon Technology Development group. He has more than 25 years of experience in the semiconductor industry with specific work on advanced silicon technology research and development. His current work is on development and companywide support on Electrostatic Discharge (ESD) for the nanometer submicron CMOS technologies. He is internationally known as an ESD design expert for semiconductor ICs, and has presented many invited seminars on the topic. He received his Ph.D. in Engineering Science from the University of Toledo and was a post-doctoral fellow in Physics at the University of Alberta. Dr. Duvvury has published over 120 papers in technical journals and conferences and holds 60 patents with several pending. He has co-authored three books on transistor reliability, modeling for electrical overstress, and ESD design. Dr. Duvvury has been very active in the ESD Symposium where he was the General Chairman both in 1994 and in 2005. He is a Director on the ESD Association Board since 1997 promoting university advanced research in ESD. He has received the Outstanding University Mentor Award from the Semiconductor Research Corporation and the Outstanding Contributions Award from the ESD Association. He is a member of Sigma XI, Eta Kappa Nu, and is a Fellow of the IEEE.

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