Electrostatic Protection for Semiconductor Electronics

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What is Electrostatic Discharge?
Purpose

• To understand what Electrostatic Discharge (ESD) is and what it means to electronics applications
• To define how the semiconductor industry takes precautions to minimize the threat to electronics
• To understand how silicon technologies are advancing and what the impact is on ESD and for future of the electronics
Outline

• What is Electrostatic Discharge (ESD)?
• ESD Control Methods
• Why is ESD important for semiconductor Integrated Circuit (IC) components?
• The impact of ESD on Electronic Systems
• Advances in silicon technology and the impact on ESD
• Advances in IC packages and the influence on ESD reliability
• Future research opportunities
How is Static Generated?

Contact and Separation of Materials
Electrostatic Charge Transfer

Triboelectric charging is the transfer of electrons between materials.

The material that loses electrons becomes positively charged and the material that gains electrons becomes negatively charged.

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Definitions

- **Electrical Overstress (EOS)**
  The exposure of an object to a current or voltage beyond its maximum ratings.

- **Electrostatic Discharge (ESD)**
  The transfer of electrostatic charge between bodies or surfaces at different electrostatic potential. ESD is a subset of EOS.
ELECTROSTATIC DISCHARGE (ESD)

What is Electrostatic Discharge?
- The sudden discharge of a charged body
- Tribo-electric and induced charging

Importance of ESD to the Semiconductor Industry
- Unexpected destruction of semiconductor devices
- Losses can occur anywhere from fabrication to field
- Millions of dollars in real losses each year
- Unknown amount of hidden losses each year

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A BRIEF REVIEW OF THE HISTORY OF ESD

• On this planet, static electricity has been a curiosity for magicians to pseudo-scientists for many hundreds of years.

• Static sparks needed special precautions in manufacturing of gun powder.

• Static electricity became a problem for the film industry in the 40’s and 50’s and for the electronic industry in the 50’s and 60’s. It became worse with newer technologies in the 70’s, it is becoming even more critical ever since…

• Today many industries or organizations take special care for ESD or for static sparks.
Dinosaurs to ICs can suffer from ESD

Did ESD really cause havoc on the prehistoric giants? Who knows? It might have caused their extinction!

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Definitions

EOS General

ESD

High Voltage (1V –15kV)
Short Duration
Very Low Power
Fast Rise Time
(1-10 ns)

Lightning

Extremely High Voltage
Extremely High Power

EOS Specific

Low Voltage (16V)
Longer Duration
Low Power
(1-10 ms)

Integrated Circuit (IC)
chips used in consumer
and medical electronics
can be damaged with ESD

Houses, Buildings,
Airplanes, Electronics, etc.

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What voltage levels are generated if ESD is not controlled?

<table>
<thead>
<tr>
<th>CONDITION</th>
<th>AVERAGE READING(V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Person Walking Across Linoleum Floor</td>
<td>5,000</td>
</tr>
<tr>
<td>Person Walking Across Carpet</td>
<td>15,000</td>
</tr>
<tr>
<td>Person Working at Bench</td>
<td>800</td>
</tr>
<tr>
<td>Ceramic Dips in Plain Plastic Tube</td>
<td>700</td>
</tr>
<tr>
<td>Ceramic Dips in Plastic Set-Up Trays</td>
<td>4,000</td>
</tr>
<tr>
<td>Ceramic Dips in Styrofoam</td>
<td>5,000</td>
</tr>
<tr>
<td>Circuit Packs as Bubble Plastic Cover Removed</td>
<td>20,000</td>
</tr>
<tr>
<td>Circuit Packs as Packed in Foam Box</td>
<td>11,000</td>
</tr>
<tr>
<td>Circuit Packs (Packaged) as Returned For Repair</td>
<td>6,000</td>
</tr>
</tbody>
</table>
But, humidity helps reduce static charge generation and accumulation
(values shown in volts)

<table>
<thead>
<tr>
<th>Event</th>
<th>Relative Humidity</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>10%</td>
</tr>
<tr>
<td>Walking across a vinyl floor</td>
<td>12,000</td>
</tr>
<tr>
<td>Motion of bench employee</td>
<td>6,000</td>
</tr>
<tr>
<td>Removing ICs from plastic tube</td>
<td>2,000</td>
</tr>
<tr>
<td>Packing PWBs in foam line box</td>
<td>21,000</td>
</tr>
</tbody>
</table>

* TED DANGELMAYER, ESD PROGRAM MANAGEMENT, KLUWER ACADEMIC PUBLISHERS, 1999

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It can be controlled by materials

Bad

- INSULATIVE: Non-conductive, removed from workplace whenever possible. (> $1 \times 10^{12}$ Ohms)

Not so bad

- CONDUCTIVE: Lowest surface resistance. (<$10^4$ Ohms)

Good

- DISSIPATIVE: Bleeds off charges at optimum rate. Strongly preferred. ($10^4$ to < $10^{11}$ Ohms)

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If it is not properly controlled in a silicon manufacturing environment...

Thousands of volts can be generated

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How is ESD controlled?

1. Grounding Person Wrist Strap to Ground (or flooring/footwear)
2. Grounded Work Surface
3. ESD Protective Packaging
With good ESD control the levels are lower

Only hundreds of volts are generated

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IC Package Impact on ESD

- IC packages can have impact on ESD requirements for
  - Human Body Model (HBM)
    - Exposed IC package pins can be touched during normal handling
  - Charged Device Model (CDM)
    - IC packages that acquire charge in automated handlers can discharge with contact to ground
Human Body Model

Carry Device to Ground, or Touch a Grounded Device

Body Capacitance  Body Resistance  Device  Contact Resistance

Current Pulse

Copyright (C) SH&A & ESDA
Electrostatic Basics for Program Managers

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Courtesy: ESD Association
IC Chip pins are protected with protection devices (diodes) on the chip.
On-Chip Protection Design

The Input and Output pins of the IC protected from ESD
The clamp turns only when ESD is detected
These clamps introduce capacitance and reduce circuit speed

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What if the IC pins are not adequately protected?

Damage to transistors

Damage to insulating oxides

Damage to internal circuits

With IC pin damage the chips would not function in a system
What about touching the systems themselves?

Electric and magnetic fields produced by ESD couple to the system in multiple ways, causing failures.

A human holding a metallic object (e.g. keys, screwdriver) discharging accumulated static charge through an electronic product (e.g. cellular phone, computer).
Cable Discharge During Computer Connections

- Cables could acquire electrostatic charges primarily due to tribo-charging
- A discharge could occur when a charged cable is plugged into an electronic equipment
- The electronics inside must be protected

Discharge from a 100m long cable charged to 2000V
ESD on Systems

Any electronic equipment can be damaged by ESD

“End Equipment”

PDAs
Cell Phones
Corded Phones
Computers
Printers
Copy machines
Automotive electronics
Telephone Switching gear
... any electronic end product!

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Digital Electronics...
Increasingly becoming part of daily lives
Music, Movies, TV Shows, Home Video, Photos, Audiobooks, Podcasts
Consumers just want to turn it on and enjoy high quality digital content
Real Time A/V streaming, Data/Control, Decoder/Encoder, Content Protection
...On the Road

We need to make sure all electronics are protected!
Stages of ESD Protection Methods and Design

**Fab environment**
- Measure: Ionizer
- Measure: Static handling

**IC Assembly & Test**
- Measure: Grounding
- Measure: Ionizer

**Board assembly & repair**
- Measure: System-level protection

**End customer operation**
- Measure: Shielding
- Measure: Prerunning ground

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Silicon Technology Advances and Challenges...

- Smaller transistors (<100 nm feature sizes) for higher speed circuits (5-10 GHz)
  - These transistors are much more delicate for ESD protection
- Complex circuit designs with multiple functions on the same chip
  - Continuous challenge to protect them and still maintain high speed performance
- Larger and advanced IC packages producing higher current levels during discharge
  - Making sure all types of packages are equally protected
3-D Transistors of the Future

These transistors are built on top of silicon-on-insulator

These devices are expected to be very sensitive to ESD

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C. Russ et. al, ESD Symp. 2005
Classical FET in Bulk Si

- Scaling expected to become difficult due to Short Channel Effects (32nm node and beyond)

C. Russ ESD Symp. 2005

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Planar FET Device in SOI

- Low junction capacitance $\rightarrow$ speed!
- Good body control in fully depleted SOI

C. Russ ESD Symp. 2005

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MuGFET Device (or “FIN”-FET)

- Channel enclosed by multiple (2, 3, 4) gates
  → Best body control (fully depleted)
  → Suppression of Short Channel Effect
- Best candidate for continued technology scaling

2 gates @ sides: double-gate
3 gates @ sides + top tri-gate

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Multi-gate Transistors (MUGFETs) with very small dimensions

- Fin height: 66-80nm (present), 30-40nm (target)
- Fin width: 50nm (present), 20-30nm (target)
- Capability to carry ESD current?
MuGFET: Damage Under ESD

- Unprecedented high ESD sensitivity
- Fused fins if process is not optimized

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H. Gossner IEDM 2006
Circuit Challenges: New Designs

- Increased Analog IO applications
- Analog Integration
- High speed IO interfaces
- Increased RF integration
- New IO features
- USB applications
Example: Impact of ESD protection on circuit speed

- Data Rates are influenced by the loading capacitance
- The capacitance in turn degrades ESD levels
Digital, Analog, and RF on the same chip require three different ESD protection strategies.

Interactions through the different ground planes require complex ESD bus architecture.

Every pin needs protection.
ESD performance is dependent on package type and the package lead design.
## Technology Scaling Effects: IC Packages

<table>
<thead>
<tr>
<th>Technology Node</th>
<th>Common Packages</th>
<th>New Developments</th>
<th>Comments on ESD</th>
</tr>
</thead>
<tbody>
<tr>
<td>3-5 um</td>
<td>DIP TQFP QFP</td>
<td>-</td>
<td>DIP devices relatively more sensitive to HBM</td>
</tr>
<tr>
<td>1 um</td>
<td>DIP TQFP QFP</td>
<td>PBGA Flip-Chip-BGA</td>
<td>TQFP more sensitive to CDM than the BGA’s</td>
</tr>
<tr>
<td>1 um to 100nm</td>
<td>TQFP QFP</td>
<td>2000 pin Flip-Chip Packages</td>
<td>Large pin count devices very harsh for CDM protection</td>
</tr>
<tr>
<td>Technology Node</td>
<td>Common Packages</td>
<td>New Developments</td>
<td>Comments on ESD</td>
</tr>
<tr>
<td>-----------------</td>
<td>-----------------</td>
<td>------------------</td>
<td>-----------------</td>
</tr>
<tr>
<td>3-5 um</td>
<td>DIP TQFP QFP</td>
<td>-</td>
<td>DIP devices relatively more sensitive to HBM</td>
</tr>
<tr>
<td>1-2 um</td>
<td>DIP TQFP QFP</td>
<td>PBGA Flip-Chip-BGA</td>
<td>TQFP more sensitive to CDM than the BGA’s</td>
</tr>
<tr>
<td>1 um - 0.5 um</td>
<td>TQFP QFP</td>
<td>2000 pin Flip-Chip Packages</td>
<td>Large pin count devices very harsh for CDM protection</td>
</tr>
</tbody>
</table>
## IC Package Impact on ESD

<table>
<thead>
<tr>
<th>Technology Node</th>
<th>Common Packages</th>
<th>New Developments</th>
<th>Comments on ESD</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.5 um</td>
<td>TQFP QFP BGA</td>
<td>Stacked Die / Stacked Packages</td>
<td>Complexity in ESD testing</td>
</tr>
<tr>
<td>100 nm</td>
<td>BGA</td>
<td>Silicon Vias</td>
<td>Major challenge for ESD evaluation</td>
</tr>
<tr>
<td>&lt;50 nm</td>
<td>No packages</td>
<td>Bare die</td>
<td>Unknown ESD evaluation</td>
</tr>
</tbody>
</table>
Protection design is difficult for large packages!

Jahanzeb et al, ESD Symp. 2007

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Both Stacked Die and Stacked Package trends can lead to unknown ESD stress discharge currents
Package on Package (POP)

Top Pads

Complications with stacked die and stacked packages

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## Package ESD Sensitivity*

<table>
<thead>
<tr>
<th>Condition</th>
<th>Classification</th>
<th>Sensitivity Scale</th>
</tr>
</thead>
<tbody>
<tr>
<td>No IC Chip</td>
<td>Discretes</td>
<td>0 (None)</td>
</tr>
<tr>
<td>IC in Package</td>
<td>Memory OMAP</td>
<td>3 (Low)</td>
</tr>
<tr>
<td></td>
<td>Analog Digital</td>
<td></td>
</tr>
<tr>
<td>IC in Package</td>
<td>CMOS BiCMOS</td>
<td>4 (Low)</td>
</tr>
<tr>
<td>IC in Package</td>
<td>65nm and beyond</td>
<td>6 (Moderate)</td>
</tr>
<tr>
<td>IC in Package</td>
<td>RF CMOS</td>
<td>7 (Moderate)</td>
</tr>
<tr>
<td>IC in Package</td>
<td>RF GaAs</td>
<td>8 (High)</td>
</tr>
<tr>
<td>IC in Package</td>
<td>5-10 GHz</td>
<td>9 (Very High)</td>
</tr>
<tr>
<td>Wafer Scale</td>
<td>TBD</td>
<td>9 (Very High)</td>
</tr>
</tbody>
</table>

ESD levels <500V HBM are considered sensitive

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Transient Stress Modes

ESD: require on-chip protection
IEC: requires off-chip and on-chip protection
EOS: requires care during customer applications
A number of IC design constraints can reduce the ESD protection levels for the sensitive high speed chips will continue to degrade.

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ESD Threshold Population Trends

Analysis by Dr. Terry Welsher, Dangelmayer Associates

Bimodal Distribution

High Speed Population

Slide Courtesy Dangelmayer Associates
New Research: Polymer Voltage Suppressors (PVS) low capacitance ESD protection increases GHz Electronics availability by increasing reliability.

1) Solution specific trigger voltage
2) Sub 1 ns response times
3) Extremely low capacitance
4) Freed circuit board space
5) Lower Impedance

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Courtesy: Electronics Polymers Inc.
Air Gap based ESD protection

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Features

- Polymer Voltage Suppressors (PVS) can offer low capacitance ESD protection

1) Solution specific trigger voltage
2) Sub 1 ns response times
3) Extremely low capacitance
4) Freed circuit board space
5) Lower Impedance

EPI-FLO

Circuit to be protected

“Z”
Why is this better?

- **Lower trigger voltage**
- **Extremely low capacitance**
- **Faster response time**
- **Freed circuit board space**
- **Lower impedance**
Can this polymer be integrated into IC package?

No protection Damages IC

Polymer in IC Package

Polymer ESD Protection

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Summary and Outlook

• ESD is always a major concern for IC components and electronics systems that are built with these components
• Every consumer must be aware of ESD as they handle their personal electronics
• Rapid advances in technologies and circuit performance requirements are making ESD reliability into a constant challenge
Summary and Outlook

• Newer IC packages will make ESD testing even more complicated
• Integration of ESD suppressive materials into the IC package itself is one option that needs to be explored
• Package research must also address innovation towards non-exposed pins or sealed IC pins to minimize the ESD threat
• Research into ultra low capacitance package types will also be crucial for maintaining safe ESD levels for very large packages
Acknowledgments

• ESD Association (ESDA)
• More information on ESD can be obtained from www.esda.org
• Mr. Dave Swenson, Affinity Static Control Consulting, LLC.
• Mr. Ted Dangelmayer, Dangelmayer and Associates
• Dr. Karen Shrier, Electronics Polymers Inc.