INVESTIGATION OF THE EFFECT OF RESISTIVITY AND THICKNESS ON THE PERFORMANCE OF CAST MULTICRYSTALLINE SILICON SOLAR CELLS

Manav Sheoran[1, 2], Ajay Upadhyaya[1], Brian Rounsaville[1], Dong Seop Kim[1], Ajeet Rohatgi[1], S. Narayanan[3]
[1]University Center of Excellence for Photovoltaic Research and Education (UCEP)
School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332
[2]School of Physics, Georgia Institute of Technology, Atlanta, GA 30332
[3]BP Solar, 630 Solarex Court, Frederick, MD 21703

ABSTRACT

A low resistivity of 0.2-0.3 Ω.cm has been shown to be optimum for high quality single crystal silicon for solar cells. However, for lower quality cast mc-Si, this optimum resistivity increases owing to a dopant-defect interaction, which reduces the bulk lifetime at lower resistivities. In this study, solar cells fabricated on 225 µm thick cast multicrystalline silicon wafers showed very little or no enhancement in efficiency with the decrease in resistivity. However, V_{oc} enhancement was observed for the lower resistivity cells despite significantly lower bulk lifetimes compared to higher resistivity cells. After gettering (during P diffusion) and hydrogenation (from SiN_x) steps used in cell fabrication, the bulk lifetime in 225 µm thick wafers from the middle of the ingot decreased from 253 µs to 135 µs when the resistivity was lowered from 1.5 Ω.cm to 0.6 Ω.cm. This paper shows that solar cells fabricated on 175 µm thick, 1.5 Ω.cm, wafers showed no appreciable loss in the cell performance when compared to the 225 µm thick cells, consistent with PC1D modeling.

INTRODUCTION

The cost of PV generated electricity must decrease by a factor of 2-4 to become competitive with conventional energy resources. To reach this goal, the direct module manufacturing cost must be reduced to less than $1/W, along with decreases in BOS costs and system installation costs. The module cost target can be met if 18-20%-efficient cells can be produced on 100-200 µm thick Si wafers using low-cost processing like screen-printing (SP). The surge in the manufacture of modules based on cast multicrystalline silicon (mc-Si) solar cells owes to the fact that mc-Si is cheaper than single crystal float zone and Czochralski silicon. This reduced cost comes at the expense of reduced material quality, which often leads to a lower efficiency for solar cells made on cast mc-Si. In addition, the quality of the wafer depends on its location in the mc-Si ingot. Usually, regions of the ingot in contact with the crucible (sides and bottom) are of poorer quality, as is the top region, due to impurity segregation.

An enhancement in efficiency can be realized by reducing the base resistivity for high quality FZ, single crystal, Si solar cells, which show an optimum at 0.2-0.3 Ω.cm [1]. This increase in performance is due to the increase in the open circuit voltage (V_{oc}) of the solar cell, without significant loss in the short circuit current (J_{sc}). The benefits of going to lower resistivity are, however not realized in Cz Si due to dopant-induced light induced degradation [2] and also in mc-Si solar cells because at higher doping, dopants may engage with impurities to form lifetime limiting centers/traps within the bandgap. This paper analyses the impact of increasing the base doping through lifetime monitoring and the fabrication and analysis of mc-Si solar cells.

Currently, silicon constitutes about 53% of the total module cost, and therefore a significant cost reduction could be realized if the wafer thickness is reduced while yield and cell performance are maintained. This reduction in thickness often results in a decrease in cell performance compared to the cells of conventional thickness and design with an aluminum back surface field (Al-BSF). However, this reduced cell efficiency with a thinner wafer can be more cost effective compared to a higher efficiency thick wafer, if the yield is maintained [3]. In this study, the effect of reducing the wafer thickness on cell performance is investigated by comparing 225 µm and 175 µm thick wafers.

EXPERIMENTAL

Solar cells were fabricated using a standard, manufacturable process with SP contacts on wafers from the top, middle, and bottom regions of four different boron doped p-type ingots from BP Solar as shown in Table 1. These wafers were first chemically etched in acid for a short time to remove the saw damage and then received a standard RCA clean. Lifetime measurements were taken using the Quasi-Steady-State Photo-conductance (QSSPC) technique, with surfaces passivated by an iodine-methanol solution. These wafers then received $POCl_3$ diffusion to form a ~45 Ω/sq. n^+-emitter, followed by low frequency PECVD SiN_x antireflection (AR) coating deposition on the front. Nine 4 cm^2 cells were fabricated on each 10 cm x 10 cm wafer by Al screen-printing on the back and silver (Ag)

grid printing on the front. A special low bow Al paste was used on the back and Ag paste was used on the front. These cells were then co-fired using an optimized process in a lamp-heated IR belt furnace, resulting in simultaneous formation of an Al-BSF and the front Ag grid metallization. Cells were then isolated with a dicing saw and annealed in forming gas at 400°C before I-V measurements. Finished cell lifetime was measured after etching off the emitter and the Al-BSF on the processed cells.

Table 1: Thickness and resistivity of ingots used in this study.

Ingot #	Thickness (µm)	Resistivity (Ω.cm)	Region*
1	225	0.6	T,M,B
2	225	1.5	T,M,B
3	175	0.6	T,M,B
4	175	1.5	M
* T = Top; M = Middle; B = Bottom			

RESULTS AND DISCUSSION

I-V results of solar cells with SP contacts on 225 µm and 175 µm thick wafers in Table 2 show that wafers from the middle of each ingot yielded the best cells with peak efficiencies in the range of 16.4 to 16.7%. No dependence on wafer resistivity or thickness was observed for the cells from the middle of each ingot. Cells made on wafers from the top of each ingot showed lower J_{sc} and V_{oc} values, suggesting that the bulk lifetime in these wafers was lower than those from the middle of the ingots. Figure 1 summarizes the as-grown, post diffusion and finished cell carrier lifetime in wafers from ingots 1-4. The results show that wafers from the middle of the ingots have high bulk lifetimes after growth (38-83 µs), while wafers from the top and bottom of the ingots have much lower lifetimes (1-4 µs). Gettering during $POCl_3$ diffusion improved the lifetime in all regions of the four ingots, but was particularly effective in wafers from the bottom of the ingots where the lifetime increased to 63-136 µs. The middle region also benefited significantly from the gettering process. Lifetime was further enhanced during the co-firing cycle due to SiN_x-induced hydrogenation of defects in both middle and bottom regions. Figure 1 shows that the gettering and passivation treatments in this study were more effective in the middle and bottom regions of the ingots. After both P-gettering and hydrogenation steps, the lifetime in middle and bottom regions of most of the ingots was close to or in excess of 100 µs, while the lifetime in the top regions was below 50 µs. This is contrary to the expectation that P gettering should be more effective in the top regions of the ingot. This could however be due to high density of dislocations (>10^6 cm^{-2}), typical to wafers from the top of the ingots, which cools down faster at the end of the solidification process. These dislocations or impurity decorated dislocations, would then dominate the lifetime, even after other impurities have been gettered or passivated [4]. In the past however, we have observed the top region of some of the ingots to respond more favorably to the lifetime enhancement steps, especially after the P-gettering step, compared to the bottom regions. Hence this lifetime recovery effect in the top or bottom or both regions would be dependent on the nature of impurities and crystallographic defects, which in turn could be different for different suppliers.

Table 2: Best I-V parameters of solar cells fabricated on various thicknesses and resistivities and from different regions of ingots 1-4, using screen-printed contacts.

V_{oc} (V)	J_{sc} (mA/cm^2)	FF	Eff (%)	Region
Ingot-1 Thickness: 225 µm. Resistivity : 0.6 Ω.cm				
0.623	32.7	0.7908	16.1	TOP
0.624	33.3	0.7868	16.4	MID
0.620	32.5	0.7867	15.9	BOT
Ingot-2 Thickness: 225 µm. Resistivity : 1.5 Ω.cm				
0.615	32.7	0.7813	15.7	TOP
0.624	34.1	0.7847	16.7	MID
0.615	33.9	0.7817	16.3	BOT
Ingot-3 Thickness: 175 µm. Resistivity : 0.6 Ω.cm				
0.617	31.2	0.7810	15.0	TOP
0.627	33.0	0.7922	16.4	MID
0.623	32.8	0.7812	16.0	BOT
Ingot-4 Thickness: 175 µm. Resistivity : 1.5 Ω.cm				
0.623	33.9	0.7840	16.5	MID

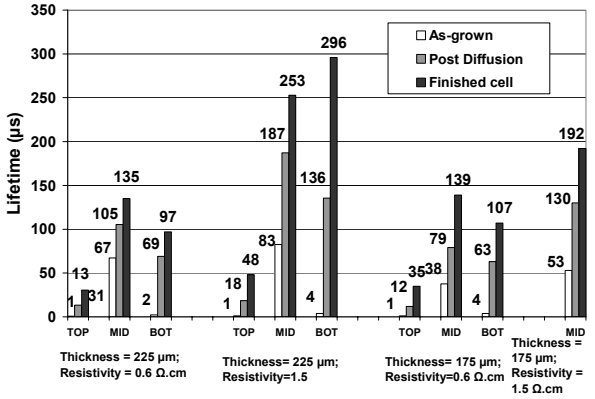

Figure 1: As-grown, post diffusion and finished cell lifetime of solar cells fabricated in this study.

Figure 1 also shows that the bulk lifetime in wafers from the middle of ingots 1 and 2 decreased from 253 µs to 135 µs when the resistivity was lowered from 1.5 Ω.cm to 0.6 Ω.cm. This decrease in lifetime is attributed to a dopant defect interaction and is analyzed in the following sections.

Effect of lifetime and base resistivity on the performance of mc-Si solar cells

The results in Table 2 show that there was no significant difference in the best cell efficiency of the solar cells made on different resistivity substrates,

despite a significantly lower finished cell lifetime in low resistivity wafers, shown in Figure 1. This can partly be explained from the dependence of efficiency on bulk lifetime. Once the bulk lifetime exceeds 100 µs, efficiency is no longer a strong function of lifetime [5]. In this study the lifetime in wafers from the middle of ingots 1 (0.6 Ω-cm) and 2 (1.5 Ω-cm), both exceeded 100 µs after processing leading to >16% efficient 4 cm^2 cells. Even with a lower final lifetime, no change in V_{oc} was observed for the lower resistivity wafers. For example, an increase in *average* V_{oc} of 2 mV was found in the bottom region wafers of 0.6 Ω.cm (ingot 1) wafers, compared to the 1.5 Ω.cm (ingot 2) wafers, even though lifetime was ~200 µs lower in the lower resistivity case.

Effect of reducing the wafer thickness on the performance of mc-Si solar cells

The performance of mc-Si solar cells could increase or decrease when the wafer thickness is reduced depending on the values of device parameters such as bulk lifetime and back surface recombination velocity (S_r) [6,7]. An improvement in V_{oc} when decreasing the thickness can be observed if S_r on the back of the p-type wafer is kept below a critical value given by $S_{r,cr}$ = D/L (D: Diffusion constant for minority carriers, L = diffusion length of minority carriers in the base region) as is evident from equation 1, where J_{ob} (dark saturation current of base) increases for values greater than $S_{r,cr}$. On the other hand for S_r values less than $S_{r,cr}$, an enhancement in V_{oc} would be observed due to a decrease in J_{ob}.

$$J_{ob} = \frac{qDn_i^2}{LN_A}.F \qquad \ldots(1)$$

With

$$F = \frac{\frac{S_r L}{D} + \tanh(\frac{W}{L})}{1 + \frac{S_r L}{D}\tanh(\frac{W}{L})} \qquad \ldots(2)$$

S_r : Rear surface recombination velocity
W: Device thickness
N_A: Doping concentration

Hence, V_{oc} is a key parameter to assess whether reducing the thickness was beneficial or not. For low lifetime top region wafers (eg. ingot 1- lifetime: 31 µs; resistivity: 0.6 Ω.cm), $S_{r,cr}$ is ~800 cm/s. Whereas, for higher lifetime middle region (ingot 1- lifetime: 135 µs; resistivity: 0.6 Ω.cm), $S_{r,cr}$ is ~ 400 cm/s. For the screen-printed solar cells fabricated in this study, the Al-BSF was expected to yield S_r values > 700 cm/s for the 0.6 Ω.cm wafer. This was estimated from the calculated Al-BSF profile and an SRV model. Hence, a slight improvement in V_{oc} was expected on reducing the thickness for the low lifetime top region, whereas a reduction in V_{oc} would be expected for high lifetime middle region. This was indeed found to be the case, where the *average* V_{oc} practically remained unchanged for the top region, whereas it showed a decrease (6 mV) in the middle region. This was further supported by V_{oc} data of high lifetime cells from middle and bottom regions of other ingots, where 4-6 mV decrease in the V_{oc} was observed on reducing the thickness. For example, the average V_{oc} reduced from 615 mV for 225 µm-thick wafers in the middle of Ingot 2 to 610 mV for 175 µm-thick wafers in the middle of Ingot 4, a decrease of 5 mV. The values of J_{sc} did not decrease much with the reduction in thickness from 225 µm to 175 µm. Hence it can be concluded that for the set of wafers studied here, thickness variation in the range of 225 to 175 µm does not degrade the cell efficiency, it only reduces the cost.

DEVICE MODELING

Device modeling was performed using PC1D [8] to study the effects of changing the base doping and thickness on the device performance. A front surface recombination velocity of 45000 cm/s and S_r of 600 cm/s were assumed. It should be noted that the S_r values are expected to be slightly higher for lower resistivity wafers, but in these simulations, the same value of S_r is assumed for all resistivities and the effect of doping on bulk lifetime is described by a model for dopant defect interaction given by equation 3 [9].

$$\tau_{n0} = \tau_{p0} = \frac{\tau_{0\infty}}{1 + N_A / N_{ref}} \qquad \ldots(3)$$

Where N_{ref} is the measure of dopant-defect interaction. $\tau_{0\infty}$ is the lifetime when there is no dopant defect interaction. A higher value of N_{ref} implies lower dopant-defect interaction. N_{ref} value of infinity would imply no dopant-defect interaction. Figures 2, 3 show the efficiency dependence on resistivity and thickness for lifetimes ($\tau_{0\infty}$) of 25 µs and 250 µs, representing the two extremes in lifetimes observed in cast mc-Si cells. In these calculations an N_{ref} value of 2e16 cm^{-3} was assumed. The data in Figure 1 shows that the lifetime of the low resistivity 0.6 Ω.cm wafers is approximately half the lifetime for 1.5 Ω.cm wafers. Hence an approximate value of N_{ref}, comparable to the base doping is used, which reduces the bulk lifetime by a factor of two (Equation 3). Figure 2 shows that for lower lifetime materials (25 µs), cell efficiency improves for lower values of thickness (< 100 µm) and base resistivity (~ 0.5 Ω.cm). On the contrary, for higher lifetime case of 250 µs, the maximum efficiency is shifted to higher values of base thickness (> 300 µm) and there is a broad maxima for doping and thickness (Fig. 3). The calculated optimum resistivity for the high lifetime case still remains at ~0.5 Ω.cm. Furthermore from the data in Figure 2, for the thickness and doping ranges studied here, efficiency lies in the narrow range of 15.5% to 15.7%. For the high lifetime case in Fig. 3, when the resistivity swings from 1.5 to 0.6 Ω.cm and thickness swings from 225 to 175 µs, the calculated efficiency swings only in the range of 16.5% to 16.8%. This is

consistent with the cells fabricated here, supporting that no significant change in efficiency should be expected for these wafers when thickness is changed from 225 µm to 175 µm and doping changed from 1.5 Ω.cm to 0.6 Ω.cm for N_{ref} value of 2e16 cm^{-3}. Results may change for different N_{ref} values.

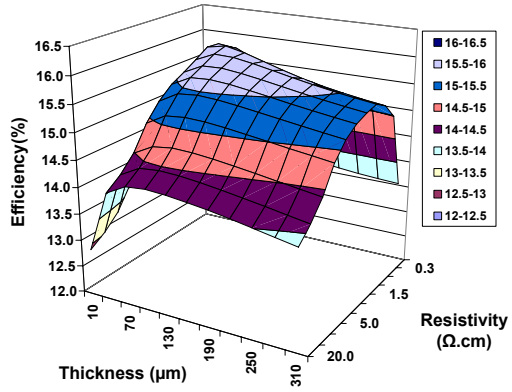

Figure 2: Efficiency dependence on resistivity and thickness- bulk lifetime of 25 µs, S_r of 600 cm/s and N_{ref} of 2e16 cm^{-3}.

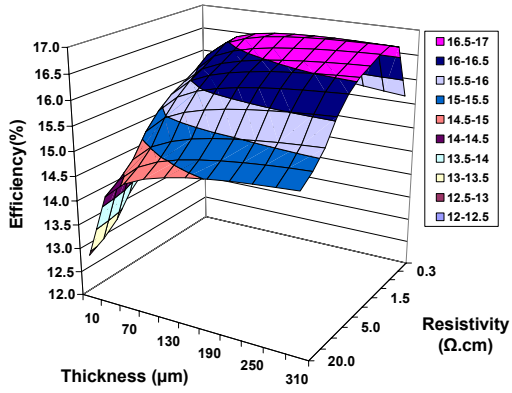

Figure 3: Efficiency dependence on resistivity and thickness- bulk lifetime of 250 µs, S_r of 600 cm/s and N_{ref} of 2e16 cm^{-3}.

Further device modeling was performed using an N_{ref} value of infinity (no dopant-defect interaction). The same conclusions as above regarding thickness were reached but the optimum resistivity decreased to a lower value (~0.3 Ω.cm). Hence dopant-defect interaction has the effect of increasing the optimum base resistivity. An optimum resistivity of 0.5 Ω.cm was found to be true for the set of wafers from this study. This optimum resistivity would however increase or decrease based on the value of N_{ref}.

CONCLUSIONS

Solar cells were fabricated on wafers from top, middle and bottom regions of cast multicrystalline silicon ingots with resistivities of 1.5 Ω.cm and 0.6 Ω.cm and thicknesses of 225 µm and 175 µm. A standard manufacturable industrial cell fabrication process was used involving screen-printing of front and back contacts. The expected increase in the performance with increased doping was not realized. This was attributed to the dopant-defect interaction, which lowered the lifetime in mc-Si. An increase in the average V_{oc} of up to 4 mV was observed on decreasing the base resistivity, which was counterbalanced by the loss in lifetime and J_{sc}. Device modeling revealed that an optimum thickness occurs at lower thickness and lower resistivity for low bulk lifetime wafers. For higher bulk lifetime wafers, an optimum still occurs at lower resistivities, but is shifted to higher thickness. Device modeling also showed that the dopant-defect interaction has the effect of increasing the optimum base resistivity to higher values.

REFERENCES

[1] J. Brody et al., "Bulk Resistivity Optimization for Low Bulk-Lifetime Silicon Solar Cells", *Progress in Photovoltaics*, vol. **9**, 2001, pp. 273-285.

[2] J. Schmidt, K. Bothe, "Structure and transformation of the metastable boron and oxygen related defect center in crystalline silicon", Phys. Rev. B **69**, 024107 (2004).

[3] A. Upadhyaya et al., "Greater than 16% efficient screen printed solar cells on 115-170 µm thick cast multicrystalline Silicon" ,current proceedings.

[4] D. Macdonald et al., "Response to phosphorous gettering of different regions of cast multicrystalline silicon ingots", *Solid state electronics* **43,** 1999 pp 575-581.

[5] A. Rohatgi et al., "High-efficiency screen-printed belt co-fired solar cells on cast multicrystalline silicon," in *Applied Physics Lett*. **86**, 054103 (149901), 2005.

[6] M. Sheoran et al. "High efficiency thin multicrystalline solar cells", *15th Workshop on Crystalline Silicon Solar Cells and Modules: Materials and Processe, Vail, Colorado*, August 2005, pp 257-260.

[7] L. Mittelsätdt et al., "Thin multicrystalline silicon solar cells with silicon nitride front and rear surface passivation" Proc. *29th IEEE PVSC, New Orleans*, 2002, pp 166-169.

[8] P.A. Basore and D. A. Clugston, *PC1D V5.6, University of New South Wales, Sydney, Australia* , 1998.

[9] A. Rohatgi et al. "Doping and oxygen dependence of efficiency of EFG silicon solar cells". *Proceedings of the IEEE Photovoltaic Specialist Conference 1990*; pp 581-587.