GREATER THAN 16% EFFICIENT SCREEN PRINTED SOLAR CELLS ON 115-170 µm THICK CAST MULTICRYSTALLINE SILICON

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ABSTRACT

In this paper we report on the impact of mc-Si wafer thickness on efficiency. We have obtained 16.8%, 16.4%, 16.2% and 15.7% efficient screen printed 4 cm^2 solar cells on 280 µm, 170 µm, 140 µm and 115 µm thick cast mc-Si respectively. Analysis of these cells showed that the efficiency of the 115 µm thick cell is limited by a BSRV of 750 cm/s, FSRV of 120,000 cm/s and a BSR of 67%. A module manufacturing cost model for a 25 MW plant was used to demonstrate that 15.7% efficient cells on 115 µm thick wafers are more cost effective than 16.8% cells on 280 µm wafers. The module manufacturing cost reduced from $1.82/W to $1.63/W when the wafer thickness was reduced from 280 µm (efficiency 16.8%) to 115 µm (efficiency 15.7%). A roadmap is developed for 115 µm thick wafers to demonstrate how cell efficiency can be increased to greater than 18% resulting in a module cost of less than $1.40/W.

INTRODUCTION

One of the most promising ways to achieve the goal of cost effective photovoltaics (PV) is to use low-cost Si material such as multicrystalline (mc-Si) and reduce the thickness of crystalline silicon wafers used for solar cell fabrication. Currently, the mc-Si wafers account for approximately 53% of the cost of the PV module. Wafer production costs can be reduced if better utilization of the ingot is achieved by reducing the wafer thickness. For example, if the wafer thickness is reduced from 350 µm to 150 µm, the number of wafers sliced from the ingot could increase by 40% if the kerf loss is 200 µm [1]. Multicrystalline Si is used in about 56% of PV modules sold today and offers a potential for lower production cost than monocrystalline Si (mono-Si). Typically the as grown lifetime in 1-2 Ω-cm mono-Si is in the range of 200-500 µs compared to only 10-30 µs for cast mc-Si with a similar resistivity. This is mainly due to the presence of defects, grain boundaries and impurities like iron that lower the as grown lifetime in the material. Our results have shown that optimized cell processing such as in-situ gettering and hydrogenation can improve the bulk lifetime in mc-Si after cell processing to 80 to 300 µs [2], resulting in efficiencies as high as 16.9% for mc-Si cells with screen-printed contacts on 280 µm thick wafers. Our device modeling shows that this efficiency can be increased to greater than 18% if the wafer thickness is reduced to 100-140 µm and very effective surface passivation and light trapping schemes are implemented.

Several authors have attempted to study the effect of wafer thickness on the electrical performance of mc-Si cells, and the best efficiencies on wafers with thickness' less than 200 µm are typically in the range of 14-15.5%. For example, Tool et al. reported an efficiency of 14.2% on textured 175 µm thick mc-Si with a 60 Ω/sq emitter and screen-printed contacts [3]. A solar cell efficiency of 15.2% on a 180 µm thick mc-Si wafer has been reported by Finckenstein et al using a simple cell process involving screen-printed contacts on a 35 Ω/sq emitter and a single layer anti-reflection coating. This involved optimizing the PECVD SiN for higher hydrogen content and better hydrogenation in addition to increasing the belt speed for the thin wafers compared to the normal wafers [1]. The best result on 200 µm thick mc-Si wafers was an efficiency of 16.7% reported by Duerinckx et al. , who used a combination of texturing, a 60-70 Ω/sq emitter, screen-printed contacts, and a double layer anti-reflection coating [5]. A significant cost advantage for thin mc-Si cells can be realized only if wafering, cell processing, and module assembly yields can be maintained. In this study, solar cells are fabricated on mc-Si wafers with thickness from 115 µm to 280 µm. A combination of light I-V, IQE, and QSSPC are used to analyze key optical and electrical parameters of the cells. Device modeling is used to predict the performance of cells if the surface passivation and light trapping are maintained at current levels or improved.

EXPERIMENTAL

Solar cells were fabricated by the standard baseline process, shown in Fig. 1, on 115 µm, 140 µm, 170 µm and 280 µm thick mc-Si wafers. All the wafers were not sliced form the same ingot or same location. The base resistivity of all the wafers was in the range of 1-2 Ω-cm. After the standard RCA cleaning, all the wafers were subjected to diffusion with liquid $POCl_3$ dopant source, resulting in emitter sheet resistance of ~ 45 Ω/sq. The phosphorous glass was then removed

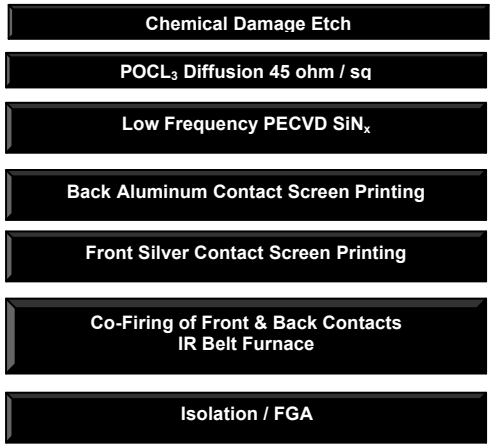

Figure 1:- Process sequence for solar cell fabrication in this study

using dilute HF. A low-frequency PECVD SiN_x film with a thickness of ~78 nm and an index of 2.0 was deposited, which serves as an anti-reflection coating and as a source of hydrogen for bulk defect passivation during the contact co-firing process. A "low-bow" aluminum (Al) paste from Ferro Corp. was screen printed on the back and a suitable commercially available silver (Ag) paste was used for the front contact metallization. Wafers were then co-fired in a belt furnace using the same firing conditions. It should be noted that the actual wafer temperature may be dependent on the wafer thickness. After firing, 4 cm^2 cells were isolated using a dicing saw and annealed in forming gas for a very short time at ~ 400°C before the I-V measurements.

RESULTS AND DISCUSSION

Effect of wafer thickness on mc-Si solar cell performance

Table 1 shows the solar cell parameters for the best cells achieved in this study on 115 µm, 140 µm, 170 µm, and 280 µm thick wafers. The results show that the cell efficiency decreased from 16.8% to 15.7% as the wafer thickness decreased from 280 µm to 115 µm. This decrease in efficiency was reflected in a decrease in J_{sc} (2 mA/cm^2) and V_{oc} (10 mV), while FF was not

Table 1:-Solar cell parameters for cells fabricated on 115 µm, 140 µm, 170 µm, and 280 µm thick mc-Si wafers.

Thickness (µm)	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	Eff (%)
115 µm	617	32.70	0.780	15.7
140 µm	620	33.29	0.782	16.2
170 µm	624	33.55	0.785	16.4
280 µm	627	34.70	0.770	16.8

affected. We measured the internal quantum efficiency (IQE) of three of the four cells in Table 1 to determine the front (FSRV) and back surface recombination velocities (BSRV) and the back surface reflectance (BSR). The IQE of the three cells are shown in Fig. 2. The IQE for the 140 µm is not shown because of nominal difference relative to 140 and 115 µm thick cell. The measured lifetimes of 100 µs for 115 µm cell and 250µs for the 280 µm were used to extract the BSRV and FSRV data. The IQE analysis shows that BSRV increased from 600 to 700 and 750 cm/s, the FSRV increased from 45,000 to 75000 and 120,000 cm/s, when the wafer thickness decreased from 280 to 170 and 115 µm respectively. According to our model calculations in PC1D, the difference in lifetime cannot cause the loss in performance, once the lifetime is above 100 µs. Therefore the loss in V_{oc} and J_{sc} as shown in Table 1 can be attributed to higher BSRV and

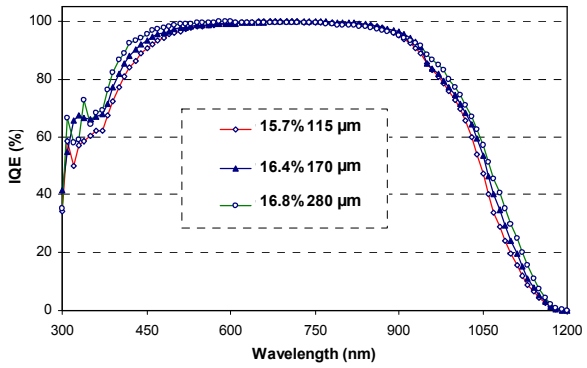

Figure 2: Internal quantum efficiency of 115 µm, 170 µm and 280 µm thick mc-Si cells.

FSRV. It is important to note that the firing profile was different for the thick and thin wafers which could have caused the differences in the SRV values and the efficiency difference between the thick and thin cells.

PC1D calculations were performed to further understand and avoid the loss in performance of thinner cells. Two different back contact parameters were used, one with a BSRV of 600 cm/s and a BSR of 68%, similar

to the current cells. The other back contact structure had a BSRV of 100 cm/s and a BSR of 98% indicative of improved or next generation cells. Fig. 3 clearly

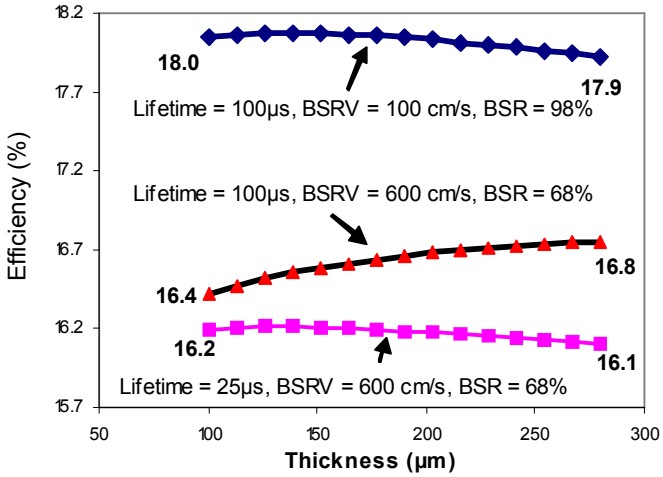

Figure 3: - PCID simulations of effect of changing the cell thickness on J_{sc}, V_{oc} and efficiency

shows that with our current back contact parameters, reducing wafer thickness results in performance loss. It is important to note that if the lifetime of the material is 25 µs with a BSRV and BSR of 600 cm/s and 68% respectively, which might be true for some mc-Si wafers from top and bottom regions of an ingot, then reducing the thickness will not cause any loss in efficiency and can even give a slight enhancement. However the improved back contact with a BSRV of 100 cm/s and a BSR of 98% can prevent the loss in performance of thinner cells on the 100 µs lifetime wafers. This could have a significant impact on the module manufacturing cost, as discussed below.

Calculation of the manufacturing cost of PV module based on thin mc-Si wafers

We have developed and used a PV manufacturing cost model for a 25 MW module manufacturing plant based on screen printed mc-Si solar cells [6] to assess the benefit of thin wafers. According to our calculations,

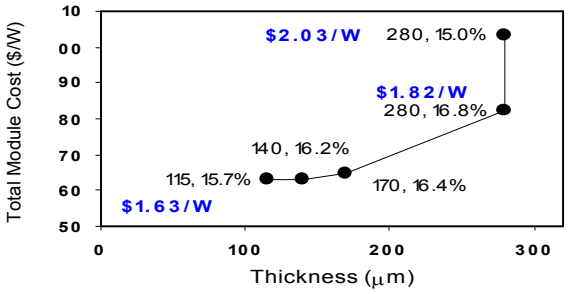

Figure 4:- Efficiency dependence on thickness and the resulting cost saving

for a cell thickness of 280 µm , cell efficiency of 15%, wafer yield of 92%, cell process yield of 95% and module process yield of 98% leads to a direct manufacturing cost of $2.03/W, which is close to the current industry situation. Fig. 5 shows that 53% of the cost of the module is associated with the silicon wafer alone, which endorses the drive toward thinner cells provided efficiency and yield can be maintained. Through improved understanding and implementation of in-situ gettering and hydrogenation we have demonstrated an efficiency of 16.8% on 4 cm^2 mc-Si solar cells on 280 µm thick wafers. If a 16.8% efficient cells can be mass produced on large area wafers, then according to Fig. 4 the direct manufacturing cost could decrease to $1.82/W, if the yield can be maintained. The cost can be reduced further by thinning down the wafers. Some studies have suggested that 100-150 µm thick wafers can be handled without a decrease in yield if proper wafer handling systems are utilized [1][7]. If yield can be maintained then 115 µm thick solar cells with an efficiency of 15.7% can bring the direct manufacturing cost down to $1.63/W, as shown in

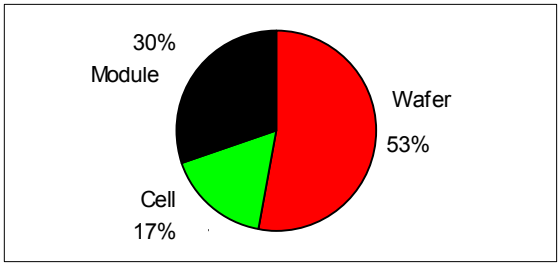

Figure 5:- Current manufacturing cost breakdown for a mc-Si PV module.

Fig. 4. Thus the benefit of reducing the wafer thickness can be realized in the module manufacturing cost even if cell efficiency decreases. It should be noted that if the cell process yield drops from 95% to 90%, and the module yield drops from 98% to 95% when the cell thickness is reduced to 115 µm with an efficiency of 15.7%, the cost of the module will rise to $1.74/W this is still less than the module manufacturing cost of 280 µm thick 16.8% efficient cells ($1.82/W).

Roadmap to cost-effective thin mc-Si solar cells

Device simulations and cost calculations were extended to determine the requirements for cost-effective thin mc-Si cells that can result in a module manufacturing cost less than $1.40/W. Fig. 6 shows that superior back contact with a BSRV of 100 cm/s and a BSR of 98% improves the efficiency from 15.7% to 17.5% and reduces cost to $ 1.46/W. Trend towards ≥ 500 MW PV plants reduce the direct module manufacturing cost by 20-25% [8][9], resulting in ≤ $1.00/W for the 17.5% 115µm thick wafer. Fig. 7 shows the effect of intermediate BSRV and BSR values

on efficiency and cost. It should be noted that in this modeling the enhancement comes at no additional cost. In Fig. 6 use of iso-texturing which decreases the average weighted reflectance to 8% could increase the

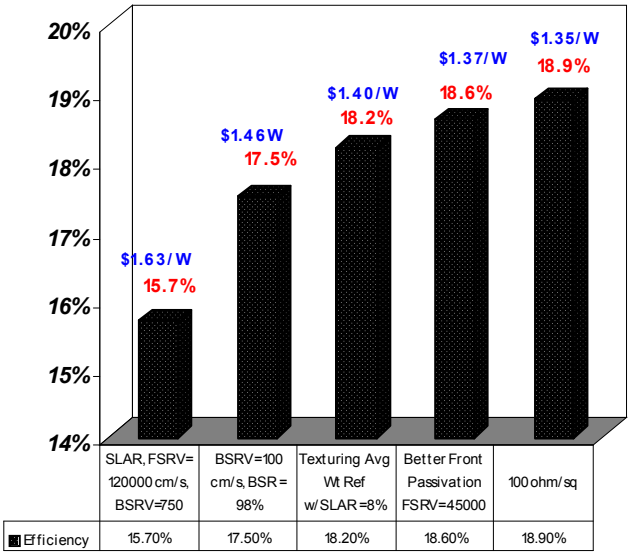

Figure 6:- Roadmap for 115 µm thin mc-Si with efficiencies greater than 18%

efficiency by 0.7% and reduce the cost to $1.40/W. Reduction in FSRV to 45000 cm/s would increase the efficiency to 18.6% and reduce the cost to $1.37/W. Finally using a 100 ohm/sq emitter could reduce the direct manufacturing cost to $1.35/W with an efficiency of 18.9%.

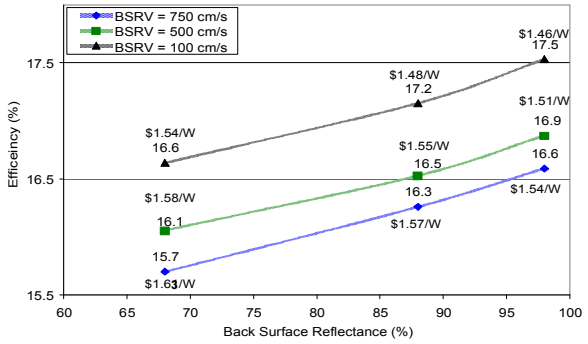

Figure 7:- Effect of BSRV and BSR on the efficiency and cost for 115 µm thick solar cells.

CONCLUSION

In this paper we have demonstrated that 4 cm^2 solar cell with efficiencies as high as 15.7% can be achieved on 115 µm thick mc-Si wafers by using a simple process with a 45 Ω/sq emitter, a single layer silicon nitride antireflection coating, and screen-printed co-fired front and back contacts. An identical process on 280 µm thick mc-Si wafers resulted in efficiencies as high as 16.8%. Analysis of these cells showed that the efficiency of the 115 µm thick cell is limited by a BSRV of 700 cm/s, FSRV of 120,000 cm/s and a BSR of 67%. In spite of its lower efficiency, the 115 µm thick cell can result in a lower module manufacturing cost than the 16.8% efficient 280 µm thick cell provided same yield can be maintained. A roadmap is presented, which shows that efficiency can be improved beyond 18% resulting in a cost of less than $1.40/W for mc-Si modules based on 115 µm thick mc-Si cells. A scale up to 500 MW PV can reduce the direct module manufacturing cost to less than $1.00/W for the 17.5% 115 µm thick wafer.

ACKNOWLEDGEMENT

This work was partly supported under the NREL subcontract - ZDO-2-30628-03.

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