DEVELOPMENT OF RIE-TEXTURED SILICON SOLAR CELLS

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ABSTRACT

A maskless plasma texturing technique using Reactive Ion Etching for silicon solar cells results in a very low reflectance of 5.4 % before, and 3.9 % after SiN deposition. A detailed study of surface recombination and emitter properties was made, then solar cells were fabricated using the DOSS solar cell process. Different plasma-damage removal treatments are tested to optimize low lifetime solar cell efficiencies. Highest efficiencies are observed for little or no plasma-damage removal etching on mc-Si. Increased J_{sc} due to the RIE texture proved superior to a single layer anti-reflection coating. This indicates that RIE texturing is a promising texturing technique, especially applicable on lower lifetime (multicrystalline) silicon. The use of non-toxic, non-corrosive SF_6 makes this process attractive for mass production.

INTRODUCTION

Increasing solar cell efficiency while maintaining a low production cost is the primary objective of solar power research. The use of low cost materials such as silicon ribbon and multi-crystalline silicon, mc-Si, provides a cheaper means of producing crystalline silicon solar cells. In terms of cell efficiency, though, mc-Si suffers from lower charge carrier lifetimes compared to single-crystalline Si. In addition, the surface is not easy to texture. In order to increase cell efficiency, texturing is a major factor: It allows for a lower overall reflection that leads to higher short circuit current. High efficiency solar cells often include some sort of texturing. Either random pyramid or inverted pyramid texturing is used for single crystal Si. Both random pyramid and inverted pyramid texturing on (100) single-crystalline Si involve alkaline etches that preferentially etch in the (111) direction [1] and result in micrometer scale pyramids. Because of the random crystal orientation of the different grains, alkaline etches are not successful for texturing mc-Si. Of course, by applying an etch mask to the surface and using isotropic etching, structures can be etched in mc-Si for light confinement [e.g. 2]. Mask-less etching of textures regardless of grain orientation is possible by some acids [e.g. 3, 4, 5] or by Reactive Ion Etching, RIE, which results in so-called "black silicon" [6]. The later method has the advantage of being a dry -chemical process that leads to extremely low reflectance. Inomata et al. have demonstrated large area mc-Si solar cells textured by Cl_2-RIE [7]. However, surface damage may be caused by RIE texturing [8] and result in a high surface recombination velocity due to the enlarged surface. Another concern with RIE texturing is the ability of such a surface to withstand subsequent processing. Both of these issues are explored, characterized, and finally implemented into solar cells in this work.

Fig. 1. SEM picture of RIE-textured silicon.

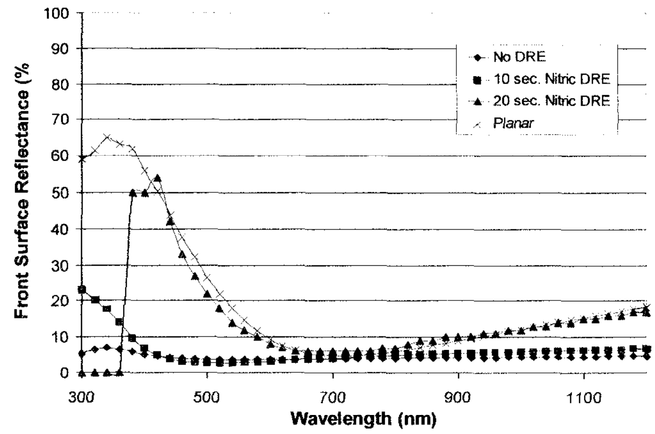

Fig. 2. Front surface reflectance curves for RIE textured + SiN ARC on multi-crystalline solar cells with varying damage removal etching schemes applied.

SURFACE TEXTURING AND SAMPLE PREPARATION

Texturing of multicrystalline silicon is an important and prevailing research topic to improve solar cell efficiency in production. Sandia developed a maskless SF_6/O_2 plasma process using Reactive Ion Etching, RIE, that leads to a needle-like texturing in the nanometer scale (Fig. 1) with a black look and excellent low reflection on mc-Si (Fig. 2).

In order to remove plasma-induced damage, different damage removal etches (DRE) were evaluated: etching in KOH or etching in an HNO_3/HF mixture for varying amounts of time. Even though damage etching removes some texture, fairly low reflectance can be maintained. Another crucial step in solar cell processing is the wafer cleaning, which should not remove the texture. A sequence with diluted H_2SO_4/H_2O_2 and HCl/H_2O_2 treatments, respectively, followed by HF dips has been found not to affect the visual appearance of the textured wafers.

Table 1. Weighted reflectance of different silicon surfaces before and after processing (spectral reflectance integrated between 400 nm and 1100 nm and weighted with the AM 1.5 global spectrum).

Texturing Process	Before cell processing	After processing and SiN ARC
RIE	10.0 %	3.9 %
RIE + KOH	20.9 %	5.8 %
RIE + HNO_3/HF	25.4 %	6.9 %
planar	34.8 %	10.4 %

In terms of reflectance control, texturing competes with antireflection coatings (ARC). A standard silicon nitride (SiN) ARC reduces the weighted reflectance on a planar surface from 35 % to 10 % (Table1). However, the initial reflectance of an RIE-textured surface is already 5.4% and drops to as low as 3.9% after SiN deposition. Samples with slightly removed texturing still show excellent reflectance of 11%. After SiN ARC, the reflectance is reduced to 4.3%. The reflectance curve of the mc-Si wafer with no DRE is flat and shows no dependence on wavelength. The planar mc-Si with the single layer ARC shows the characteristic minimum around 600nm. As the DRE time increases the reflectance curves approach the planar reflectance curve as is apparent in Fig. 2. The 20 second DRE etch matches the planar reflectance curve over a large wavelength range. This shows that the RIE texturing can effectively be cancelled if the DRE time is not properly considered.

DOSS DIFFUSION

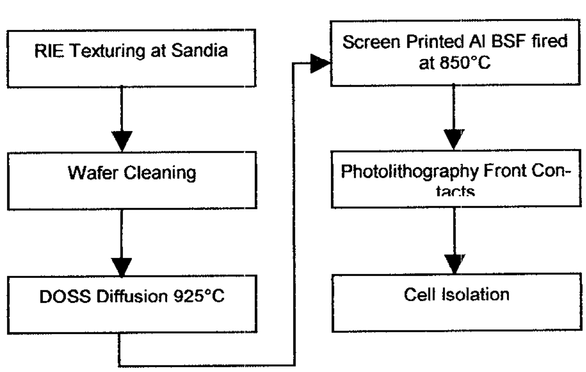

Fig. 3. Process Flow Chart

The emitter diffusion was performed by using the dopant oxide solid source (DOSS) process. Source wafers with spin-on dopant applied to both sides have been introduced to the furnace together with the samples so that every sample is stacked in front of a source wafer on one side only. This diffusion technique was used to take advantage of the in-situ oxide grown in the same furnace cycle as the phosphorus diffusion. An added benefit of this process is no phosphorsilicate glass (PSG) removal step is required. PSG removal could also remove some of the RIE texturing inadvertently. Phosphorus released from the source wafers at 925 °C diffuse into the samples leading either to the symmetric $n^{++}nn^{++}$ structure for J_{oe} measurements or to the emitter formation only, depending on the stacking. For J_{oe} and lifetime measurements high resistivity (>100 Ω·cm) n-type float zone silicon wafers were used, while solar cells were made from ~1.0 Ω·cm mc-Si. The actual diffusion time was one hour, followed by an oxidation step for 15 min to obtain the in-situ oxide. This one step furnace process leads to phosphorus diffusion, textured, in-situ oxide passivated solar cells that are immediately ready for metallization with no further processing steps. The complete process sequence is shown in Fig. 3.

SURFACE PASSIVATION AND EMITTER PROPERTIES

The challenge in surface texturing of solar cells is to find a way to increase photon absorption in the cell while maintaining low recombination losses at the surface. A rougher surface is harder to passivate. The DOSS process already includes an approximately 10 nm in-situ oxide for passivation, which (after a 15 min forming gas anneal (FGA)) leads to sufficiently low surface recombination velocities (SRV) on planar surfaces (Fig. 4).

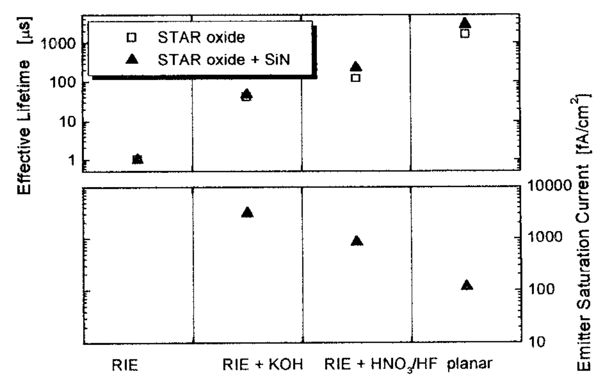

Fig. 4. Effective lifetime and corresponding emitter saturation current of differently textured silicon wafers after DOSS diffusion with in-situ oxide, and additional SiN deposition, respectively.

However, oxide passivation was not sufficient on these RIE-textured surfaces. Only samples with a DRE by HNO_3/HF show sufficiently high effective lifetimes, which correspond to sufficiently low J_{oe} or SRV (notice the logarithmic scale in Fig. 4). To make use of the well-known passivation ability of silicon nitride deposited by plasma enhanced chemical vapor deposition (PECVD), a 63 nm layer of SiN was deposited on top of the oxidized surfaces. This stack passivation leads to excellent effective lifetimes on planar samples and to good results on the HNO_3/HF etched textured samples. RIE-textured surfaces with no post-treatment or with subsequent KOH etching still show insufficiently low effective lifetimes, corresponding to high J_{oe} and SRV's. The same results were found with a stack passivation consisting of an RTO and ~70 nm of PECVD SiN, but are not shown here. The high quality of the DOSS-diffused emitter and the SiO_2/SiN stack passivation results in low emitter saturation current (J_{oe}) on the planar samples ~100 fA/cm^2 for a 100 Ω/sq. emitter (Fig. 4). However, surface passivation and emitter quality of the textured samples is poor leading to high J_{oe} values (for the samples with no DRE after RIE, it was impossible even to extract a J_{oe}). Emitter saturation current for the best RIE sample is still 5 times higher than a J_{oe} for a random pyramid sample processed similarly. Even the samples that were HNO_3/HF etched after RIE texturing and show decent surface passivation have excessively high J_{oe} values that may limit the performance of high lifetime cells. This indicates poor emitter quality due to plasma-induced damage from the RIE texturing process. Multi-crystalline silicon with much smaller lifetimes is dominated by the base saturation current J_{ob} rather than by J_{oe}. Therefore, RIE texturing may be well suited for such materials because the gain in J_{sc} due to texturing and light absorption is still able to maintain a sufficient V_{oc}, as will be addressed and demonstrated below.

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Table 2. I-V Data for RIE Multi-Crystalline Solar Cells

Wafer Treatment	Voc (mV)	Jsc (mA/cm²)	FF	η (%)	Increase
planar controls	574	22.20	0.759	9.7	**0%**
conditioned texture 20 sec nitric	566	23.43	0.733	9.7	**0%**
Al-assisted 20 sec nitric	560	27.02	0.695	10.5	**9%**
Cr-assisted 8-min KOH	576	24.77	0.756	10.8	**11%**
conditioned texture ~ 20-25 sec nitric	577	25.12	0.748	10.8	**12%**
Al-assisted 15-sec nitric,	573	25.83	0.739	10.9	**13%**
conditioned texture 15 sec nitric	582	26.96	0.748	11.7	**21%**
conditioned texture 10 sec nitric	578	27.14	0.748	11.7	**21%**
Cr-assisted no DRE	583	29.18	0.756	12.9	**33%**

Table 3. I-V Data for SiN Coated Solar Cells

Wafer Treatment	Voc (mV)	Jsc (mA/cm²)	FF	η (%)	Increase
planar controls	584	28.25	0.772	12.7	**0%**
conditioned texture 20 sec nitric	575	28.93	0.757	12.6	**-1%**
conditioned texture 10 sec nitric	587	30.84	0.751	13.6	**7%**
Cr-assisted, No DRE	591	30.63	0.759	13.7	**8%**

Table 2 shows the averaged efficiencies obtained on mc-Si with RIE texturing for various damage removal etches. Table 3 shows the efficiencies after the application of a 55nm SiN layer which was determined to be the optimal single layer anti-reflection coating (SLARC) by using the Sunrays modeling program. Also shown in the tables is the percent increase in efficiency gained by using RIE texturing compared to the planar surface, relatively. The results clearly show that there is a definite increase in both current collection and overall efficiency by using RIE texturing regardless of the DRE. The efficiency improvement is due largely to the increased current collection while maintaining similar open circuit voltages. In examining table 2 it is apparent that the shorter the DRE the higher the current collection which is supported by the reflectance data (Fig. 2). The longer the DRE time, the higher the average weighted AM1.5 Global reflectance. The improved efficiency is somewhat surprising, because of the extent of the surface damage expected in the "no DRE" case. Excessive carrier recombination and a drop in V_{oc} would be predictable. This is not the case. The in-situ oxide is able to passivate the textured surface sufficiently to maintain ~575 mV V_{oc} that is observed on the planar mc-Si. The increased current collection allows for even higher V_{oc}'s ~585 mV. A more clear understanding is obtained by examining the external quantum efficiency, EQE, depicted in Fig. 5. The blue response of the samples is in agreement with the surface passivation measurements made earlier in Fig. 4. The samples that received a DRE show a better blue response below 450nm demonstrating the superior front surface passivation. The IQE data for these samples, not shown here, also support this claim. However, the improved blue response is not sufficient to compensate for the increased current collection in the "no DRE" case. The RIE textured samples out perform the planar sample by collecting over 2 mA/cm^2 more photocurrent. Examining the efficiencies in table 3 and the reflectance curves in Fig. 2 the "10 second nitric" sample closely resembles the "no DRE" in all aspects. The weighted reflectance is 4.2% compared 3.9% after SiN SLARC application. This suggests that a short DRE may achieve an even better efficiency by slightly improving the blue response while still maintaining a low reflectance. The application of the RIE textured surfaces results in 33% initial

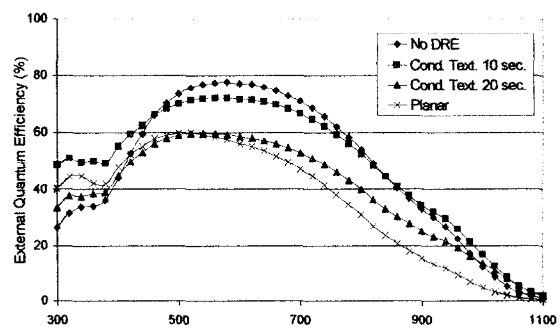

Fig. 5. External Quantum Efficiency of RIE textured samples with different Damage Removal Etches applied.

improvement and a 8% relative improvement over planar mc-Si samples used in this experiment.

CONCLUSIONS

RIE textured surfaces show excellent reflectance but poor surface quality in general, unless the RIE textured surface receives the proper damage removal etch (DRE). Even after diffusion and surface passivation by a stack of either (thermal) DOSS oxide and PECVD silicon nitride, or rapid thermal oxide (RTO) and PECVD SiN, the surface recombination is still about a factor 5 times higher than that of typical random pyramid surface. Chemical etching after RIE removes the texture to some extent leading to higher initial reflectance. However, these can still have much lower reflectance than planar samples, and the surface passivation is improved at least a little. Especially samples with a HNO_3/HF DRE show decent SRV and therefore might be a good compromise relative to reflectance and surface passivation properties. This is most evident after the application of a SLARC. Solar cell performance is enhanced to a much greater extent when compared to a sample that had no DRE. Efficiency jumps 1.9% absolute for a short DRE with nitric and only 0.8% for no DRE. Even though these samples suffer from damage of the emitter region from the RIE process, solar cells show improved performance compared to planar references. Recent improvements to the DRE process show promise for more complete damage removal, which should result in better cell performance, especially for (lower lifetime) mc-Si solar cells.

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