

# EFFECTIVE PASSIVATION OF THE LOW RESISTIVITY SILICON SURFACE BY A RAPID THERMAL OXIDE/PECVD SILICON NITRIDE STACK AND ITS APPLICATION TO PASSIVATED REAR AND BIFACIAL SI SOLAR CELLS

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**ABSTRACT:** A novel stack passivation scheme, in which plasma silicon nitride (SiN) is stacked on top of a rapid thermal SiO<sub>2</sub> (RTO) layer, is developed to attain a surface recombination velocity (S) approaching 10 cm/s at the 1.3 Ω-cm p-type (100) silicon surface. Such low S is achieved by the stack even when the RTO and SiN films *individually* yield considerably poorer surface passivation. Critical to achieving low S by the stack is the use of a short, moderate temperature anneal (in this study 730°C for 30 seconds) after film growth and deposition. This anneal is believed to enhance the release and delivery of atomic hydrogen from the SiN film to the Si-SiO<sub>2</sub> interface, thereby reducing the density of interface traps at the surface. Compatibility with this post-deposition anneal makes the stack passivation scheme attractive for cost-effective solar cell production since a similar anneal is required to fire screen-printed contacts. Application of the stack to *passivated rear* screen-printed solar cells has resulted in V<sub>oc</sub>'s of 641 mV and 633 mV on 0.65 Ω-cm and 1.3 Ω-cm FZ Si substrates, respectively. These V<sub>oc</sub> values are roughly 20 mV higher than for cells with untreated, highly recombinative back surfaces. The stack passivation has also been used to form fully screen-printed *bifacial* solar cells which exhibit rear-illuminated efficiency as high as 11.6% with a single layer AR coating.

Keywords: Passivation - 1: Rapid Thermal Processing - 2: Bifacial - 3.

## 1. INTRODUCTION

The back surface recombination velocity (S<sub>b</sub>) is a key loss component in Si solar cells. One way to reduce S<sub>b</sub> is to implement an Al-BSF in the device design [1]. This structure is effective, but the stresses imparted to the Si substrate during Al-BSF formation can preclude application to thin wafers. Process-induced stress can be virtually eliminated by employing a *passivated rear* structure (Fig. 1) in which the rear side metallization covers only a small fraction of the surface area. In addition to reducing process-induced stress, this structure is well suited for bifacial operation since the rear surface is transparent to incoming light. However, in order to take advantage of this structural feature and attain a significant power output, the passivation at the rear surface must be effective.

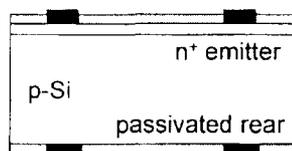


Fig. 1. Passivated rear and bifacial solar cell.

In this paper, we report the use of a dielectric stack comprised of a rapid thermal SiO<sub>2</sub> (RTO) and a plasma silicon nitride (SiN) for effective passivation of the low resistivity (0.65-1.3 Ω-cm) p-type (100) Si surface. These films are attractive from the standpoint of low-cost production since both can be applied in short times.

The essential feature of the stack passivation scheme is its ability to withstand moderate temperature annealing (700-800°C) without any degradation in S. In fact, the stack *relies* on such thermal treatment to achieve low S values. This novel method is used to fabricate passivated rear and bifacial screen printed solar cells. The finished devices are characterized so that the impact of the fractional metal coverage on S<sub>b</sub> can be deduced. Model calculations are performed to demonstrate that the stack can be successfully applied to thin substrates without sacrificing performance.

## 2. S<sub>b</sub> REQUIREMENTS FOR PASSIVATED REAR AND BIFACIAL SOLAR CELLS

Before discussing the passivation methodology, it is instructive to quantify the S<sub>b</sub> levels required for effective passivated rear and bifacial solar cells. A commonly used figure of merit to describe bifacial devices is the ratio of rear efficiency to front efficiency, or similarly rear J<sub>sc</sub> to front J<sub>sc</sub>. For effective bifacial performance, these ratios must approach or exceed 0.70.

Fig. 2 shows the simulated efficiency of an n+p solar cell illuminated by the AM1.5G spectrum from the front and rear. For S<sub>b</sub> values higher than 2x10<sup>3</sup> cm/s, the rear performance is negligible and J<sub>sc</sub>(rear)/J<sub>sc</sub>(front) < 0.30. As S<sub>b</sub> goes below 10<sup>3</sup> cm/s, the back response begins to show marked improvement. When S<sub>b</sub> goes below 500 cm/s, the rear performance becomes significant and J<sub>sc</sub>(rear)/J<sub>sc</sub>(front) > 0.70. At these S<sub>b</sub> levels, the power boost supplied from the rear side is appreciable. In Fig. 2, the total output power is plotted as a function of S<sub>b</sub> for a device with 20% (of 1-sun) rear illumination. Under these conditions, and

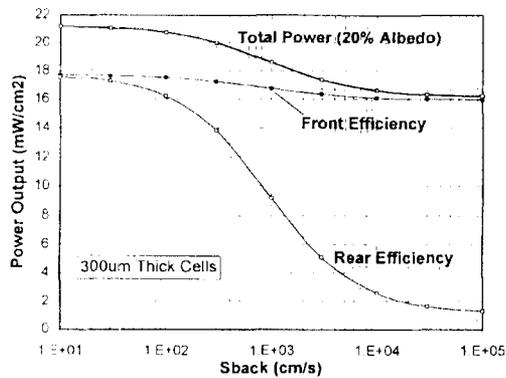


Fig. 2. Impact of  $S_b$  on passivated rear solar cell performance.

for  $S_b$  values below 500 cm/s, the bifacial power output per unit area is enhanced by 15-20% over a conventional non-bifacial cell design.

It is important to note that the  $S_b$  in Fig. 2 represents the cumulative recombination at the Si/dielectric interface and at the Si/metal contact. The metal contact will increase  $S_b$  above the value measured at the Si/dielectric interface alone. Therefore, an ideal passivation scheme should achieve  $S$  values at the Si/dielectric interface which are significantly lower than the requirements in Fig. 2. In this study,  $S$  values of less than 50 cm/s are targeted for film passivation.

### 3. QUANTITATIVE ASSESSMENT OF SURFACE PASSIVATION BY RTO/SiN STACK

The passivation quality of SiN, RTO, and an RTO/SiN stack were compared. The substrate materials used were 0.65 and 1.3  $\Omega$ -cm FZ Si. The surfaces were chemically polished, *not* mirror polished. All SiN films were deposited in a direct, high-frequency (13.5 MHz), parallel-plate reactor at 300°C. The RTOs were grown in a rapid thermal processing (RTP) unit at 900°C in 2 minutes. Ensuing thermal treatments (simulating contact firing) were carried out in a three-zone beltline furnace in which the "hotzone" temperature and time were fixed at 730°C and 30 sec. The passivation quality of each scheme was monitored by the transient photoconductance decay (PCD) technique. The effective lifetimes measured by PCD were converted to  $S$  values using a conventional analysis method [2]. In this paper, all  $S$  values are calculated assuming an infinite minority carrier lifetime in the substrate. The resulting  $S$  values are therefore maximum or "worst-case" limits.

The passivation quality of an RTO *alone* is shown in Fig. 3 for a growth temperature of 900°C. The as-grown oxide results in  $S$  higher than 10,000 cm/s which can be reduced to approximately 100 cm/s by a forming gas anneal (FGA) treatment at 400°C. However, the ensuing 730°C beltline anneal degrades the interface quality and increases  $S$  above 3000 cm/s.

A similar trend is observed here for the SiN film *alone* (also Fig. 3). The as-deposited SiN results in  $S$  greater than 10,000 cm/s which can be reduced to approximately 200 cm/s by an ensuing anneal in forming gas at 400°C. Again, the 730°C beltline treatment degrades the interface quality and increases  $S$  by approximately one order of magnitude.

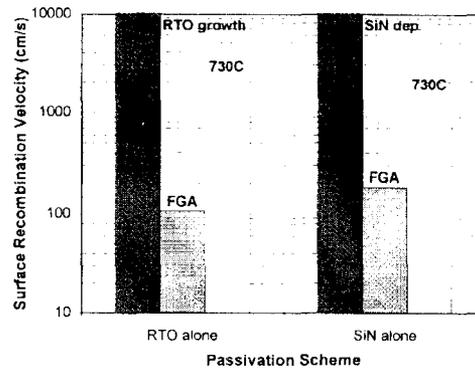


Fig. 3. Passivation by SiN and RTO films individually. The FGA treatment was 400°C in 30 min. The  $S$  values were measured at the 1.3  $\Omega$ -cm surface.

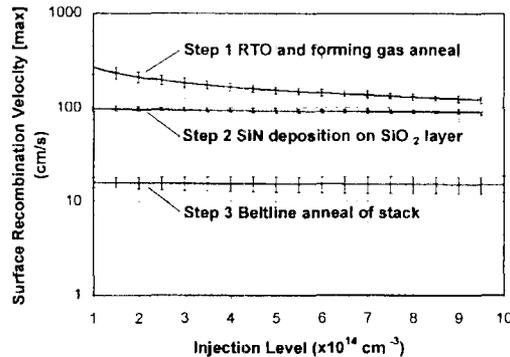


Fig. 4. Progression of  $S$  values for stack passivation of 1.3  $\Omega$ -cm Si.

Clearly, these two treatments (RTO alone or PECVD SiN alone) are not compatible with screen-printing requirements since neither can withstand a contact firing cycle without a significant increase in  $S$ . On the contrary, annealing the RTO/SiN stack actually *enhances* the passivation quality. The stepwise effect of stacking PECVD SiN on top of the RTO layer and then annealing at 730°C is shown in Fig. 4. The  $S$  value attained after the final beltline anneal (Step 3) is clearly superior to RTO growth (Step 1) or SiN deposition on top of the oxide layer (Step 2). The 730°C anneal is believed to enhance the release and delivery of atomic hydrogen from the SiN film to the Si-SiO<sub>2</sub> interface, thus reducing the density of states at the surface. *Maximum*  $S$  values of 11 cm/s and 20 cm/s are achieved by the stack passivation at the 1.3  $\Omega$ -cm and 0.65  $\Omega$ -cm p-type surfaces, respectively. These are among the lowest  $S$  values ever reported for solid film passivation of the low-resistivity Si surface.

Also evident in Fig. 4 is the weak injection level dependence of  $S$  within the measurement range ( $10^{14}$ - $10^{15}$  cm<sup>-3</sup>). This behavior is quite different than that reported for the highest quality remote SiN films where  $S$  increases by a factor of 5 as the injection level falls from  $10^{15}$  to  $10^{14}$  cm<sup>-3</sup>[3].

The initial RTO growth temperature is observed to have an effect on the final  $S$  value of the annealed stack. For an 850°C RTO growth, final  $S$  values of  $\approx$  40 cm/s are achieved on 1.3  $\Omega$ -cm Si after the 730°C beltline anneal.

This is approximately a factor 3 higher than for the 900°C RTO growth.

#### 4. ANALYSIS OF REAR CONTACT PASTE

With the development of the stack passivation scheme, the cell structure shown in Fig. 1 can potentially be achieved with the simple 5-step process sequence given in Table 1

Table 1. Simplified fabrication sequence.

Step Number	Process
1	Wafer Clean
2	Emitter Diffusion
3	RTO Growth 900°C (Front/Back)
4	SiN Passivation & SLAR (Front/Back)
5	Contact Printing (Front/Back) & Co-firing

However, in order to attain an operational device, the contact resistance at the back must be low. This requirement is complicated by two factors: 1) usually the substrate doping level is low ( $<3 \times 10^{16} \text{ cm}^{-3}$ ) which may create a barrier to current flow, and 2) the printed lines must physically punch through the SiN layer before reaching the Si surface. Both of these requirements need to be satisfied in the same cycle used to fire the front contacts. Hence, the use of an appropriate rear contact conductor paste is critical to proper device operation.

Two types of conductor paste (*Ferro Corp.*) were investigated for application to the rear surface. The first was a pure Al paste, and the second was a Ag paste containing a small fraction of Al additive. Contact resistance was monitored as a function of substrate resistivity and surface condition (bare surface versus SiN covered surface). The pastes were printed and fired in a beltline furnace using the standard 730°C front contact firing cycle. The measurement results are shown in Fig. 5.

In all cases, the contact resistance decreases with substrate resistivity. The lowest contact resistance values were measured for the Al paste fired on bare Si (*i.e.*  $\rho_c < 5 \text{ m}\Omega\text{-cm}^2$  on 0.65  $\Omega\text{-cm}$  Si). However, this Al process is not successful when the SiN layer is present. This SiN layer acts as a barrier to Al alloying with the underlying Si lattice. As a result, the Al features printed on SiN can be easily "wiped" away after the firing process. Thus, use of Al does not seem feasible in a 730°C (co-fire) punch-through process.

The results are different for the Ag paste. Printing and firing this material on bare Si results in a slightly higher contact resistance ( $\rho_c \approx 10 \text{ m}\Omega\text{-cm}^2$  on 0.65  $\Omega\text{-cm}$  Si) than pure Al. More importantly, however, is the ability of the Ag paste to successfully punch-through the SiN layer. This punch-through ability is aided by the glass frit content in the Ag paste which helps to etch through the SiN layer. Additionally, Ag particles sinter together effectively to form well defined, low-resistivity line structures which exhibit good adherence to the substrate. The resulting contact resistance for the Ag punch-through process ( $\rho_c \approx 27 \text{ m}\Omega\text{-cm}^2$  on 0.65  $\Omega\text{-cm}$  Si) is higher than for the other

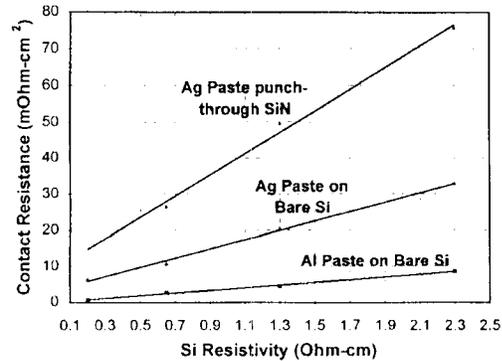


Fig. 5. Effect of paste (Ag or Al) and process (punch-through or bare Si) on contact resistance.

cases shown in Fig. 5, but it is still within appropriate limits for device application. Model calculations show that for a metal coverage of 8%,  $\rho_c$  values of 30  $\text{m}\Omega\text{-cm}^2$  can be tolerated without suffering from excess resistive loss.

#### 5. SOLAR CELL FORMATION

Passivated rear solar were fabricated on 0.65  $\Omega\text{-cm}$  and 1.2  $\Omega\text{-cm}$  FZ Si as well as 0.8  $\Omega\text{-cm}$  CZ grown by Siemens Corporation. The cell process outlined in Table 1 was implemented. (Before the diffusion, the rear surface of the wafers were masked with a plasma SiO<sub>2</sub> layer grown at low temperature. This mask was removed prior to the RTO growth.) The gridline spacing of both front and rear contacts was maintained at 2.5 mm. The results of the fabrication are shown in Table 2. For comparison, the performance of cells which lack an effective back surface treatment are also listed. In all cases, the  $V_{oc}$ 's for the passivated rear cells are significantly higher than for those formed with highly recombinative back contacts. This clearly demonstrates the ability of the stack passivation to lower  $S_b$ .

Bifacial solar cells were also formed on the 0.65  $\Omega\text{-cm}$  FZ Si. The SiN used for the stack passivation served as AR coating to both sides. The results of this initial fabrication are shown in Table 3. To date, this rear efficiency of 11.6% is the highest reported for a fully screen-printed n<sup>+</sup>-p bifacial solar cell. The ratio of the rear  $J_{sc}$  to front  $J_{sc}$  is 0.75.

#### 6. CELL CHARACTERIZATION AND ANALYSIS

It is important to extract the true  $S_b$  for the bifacial cell. As previously discussed, this parameter is a combination of the recombination activity at the dielectric/Si interface and the metal gridline/Si interface. For the present device, the rear metal coverage fraction is 8.3%. As such,  $S_{eff}$  for the device is expected to be considerably higher than the  $S$  value measured for the stack passivation layer alone, which approaches 20  $\text{cm/s}$  at the 0.65  $\Omega\text{-cm}$  Si surface. A combination of rear internal quantum efficiency measurements (IQE) and solar cell simulation (shown in Fig. 6) reveals that the device experiences an  $S_b$  of 340  $\text{cm/s}$ , which is approximately a factor of 17 higher than the  $S$  value of the stack alone. The

**Table 2.** Passivated rear screen-printed solar cell performance. The PV grade CZ material was grown by Siemens Corporation.

Material	Rear Surface	V <sub>oc</sub> (mV)	J <sub>sc</sub> (mA/cm <sup>2</sup> )	FF	Eff (%)
0.65 Ω-cm FZ-Si	Passivated	641	33.3	0.776	16.6
	No Pass	621	32.8	0.785	16.0
1.3 Ω-cm FZ-Si	Passivated	631	33.8	0.770	16.5
	No Pass	609	32.8	0.786	15.7
0.8 Ω-cm CZ-Si	Passivated	622	32.0	0.776	15.5
	No Pass	611	31.0	0.782	14.8

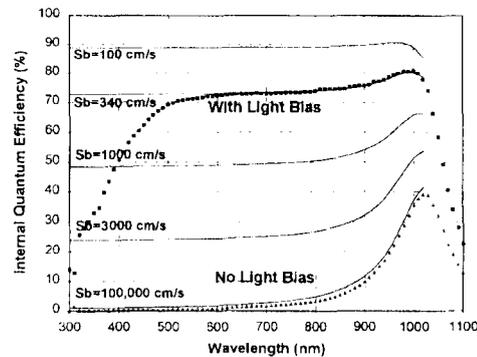
**Table 3.** Bifacial solar cell performance (verified by Sandia National Labs).

Illumination	V <sub>oc</sub> (mV)	J <sub>sc</sub> (mA/cm <sup>2</sup> )	FF	Eff (%)
Front	640	33.7	0.761	16.4
Rear	624	25.1	0.743	11.6

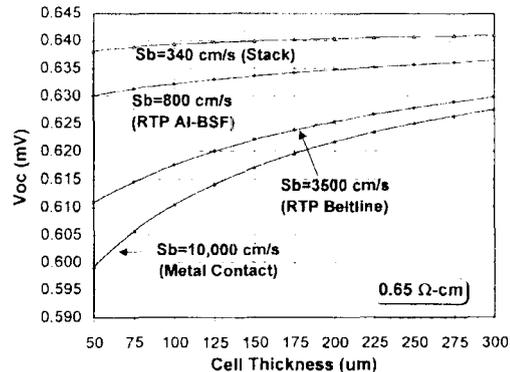
8.3% metal area coverage significantly increases the effective recombination at the rear side of the device. In spite of this effect, screen-printed device V<sub>oc</sub> levels of 640 mV indicate that the passivation scheme is still effective.

Again, the primary goal of this study is to demonstrate a passivation scheme which can be applied to thin cells without suffering from increased recombination losses. In general, as the rear surface is brought closer to the collecting junction, the effects of S<sub>b</sub> on device performance become more pronounced. If the S<sub>b</sub> is high, then reducing the substrate thickness will lower cell performance. If S<sub>b</sub> is low, then the cell performance will remain the same (or possibly improve) when the thickness is reduced. In this section, model simulations are performed to predict the effect of reducing substrate thickness for the rear passivated device (S<sub>b</sub> of 340 cm/s on 0.65 Ω-cm Si). PCID-4 was used for the simulations. All of the primary input parameters (emitter profile and S<sub>front</sub>) were gathered from appropriate measurements. The results in Fig. 7 show that for the high S<sub>b</sub> case (10<sup>4</sup> cm/s, representative of a full metal coverage surface), the V<sub>oc</sub> response falls sharply as the substrate thickness is reduced. On the contrary, the simulation for the stack passivation with 8.3% metal coverage (S<sub>eff</sub> of 340 cm/s) shows that the cell thickness can be reduced without V<sub>oc</sub> degradation.

Also shown in Fig. 7 are V<sub>oc</sub> responses for devices with mid-range S<sub>b</sub> values. In a previous study, we showed that screen-printed Al-BSFs on 2.3 Ω-cm Si result in S<sub>b</sub> values of 200 cm/s and 1000 cm/s when alloyed at 850°C in an RTP unit or beltline, respectively [1]. For 0.65 Ω-cm Si, these S<sub>b</sub> values translate to 800 cm/s (RTP) and 3500 cm/s (beltline) due to the doping level difference. These S<sub>b</sub> values have been used for the calculations shown in Fig. 7. Two points are evident from the results. First of all, the stack passivation results in the highest V<sub>oc</sub> levels. Second, stack passivated cells show the greatest ability to retain V<sub>oc</sub> as the substrate thickness is reduced.



**Fig. 6.** S<sub>b</sub> determination from rear IQE measurements. The reduced response between 300-500 nm is due to SiN absorption



**Fig. 7.** Simulating the effect of thickness and S<sub>b</sub> on solar cell performance levels. (L<sub>d</sub> = 900 μm, 0.65 Ω-cm Si).

## 7. CONCLUSIONS

A novel stack passivation scheme (consisting of RTO and SiN) has been developed which can attain S values approaching 10 cm/s at the 1.3 Ω-cm Si surface. The stack has been applied to rear passivated and bifacial screen-printed solar cells. Front and rear illuminated efficiencies of 16.6% and 11.6%, respectively, have been demonstrated on 0.65 Ω-cm Si. Device S<sub>b</sub> values of 340 cm/s were measured for cells with 8.3% rear metallization coverage. It is clear that higher performance could be attained if a more precise (less coverage) contact scheme were devised.

## ACKNOWLEDGMENT

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