Low-Temperature Electronics

John D. Cressler

School of Electrical and Computer Engineering
777 Atlantic Drive, N.W., Georgia Institute of Technology
Atlanta, GA 30332-0250 USA

cressler@ece.gatech.edu
Tel (404) 894-5161 / FAX (404) 894-4641
http://users.ece.gatech.edu/~cressler/

This work was supported by JPL, NASA-ETDP, NASA-GSFC, DARPA, and DTRA
Outline

• Extreme Environment Electronics (EEE)
• Using Si CMOS at Low Temperatures
• Using SiGe HBTs at Low Temperatures
• Building the Infrastructure for EEE
• Summary
Extreme Environments

**Defn:** Operation Outside Commercial or Mil-Spec Conditions
- **temperature** (high-T, low-T, wide-T range)
- **radiation exposure** (TID, SEE)

- **Aerospace** (aircraft, satellites, etc.)
- **Space Exploration** (Moon, Mars, etc.)
- **Automotive** (on-engine electronics, etc.)
- **Drilling** (oil, etc.)
• Some Low-Temperature Electronics Applications
  – deep-space probes and planetary missions (Moon, Europa, …)
  – satellite communications systems + space-based radar
  – ultra-high-speed / high sensitivity instrumentation systems
  – medical electronics (e.g., CT scanner)
  – superconductor-semiconductor hybrids (e.g., 20 Gb/sec ADC)
  – very low-noise receivers (radio astronomy)
  – cooled IR detector arrays

Landers / Rovers

James Webb Space Telescope
Space Radiation Effects

- The Holy Grail of the Space Community
  - IC technology space-qualified without additional hardening (major cost adder)
  - high integration levels to support SoC / SiP (low cost)

  proton + electron belts

- Total Ionizing Dose (TID) – ionizing radiation
  - TID is measured in “rads” (1 rad = 100 ergs per gram of energy absorbed)
  - 100-1000 krad(Si) over 10 years for typical orbit (300 rad(Si) is lethal to humans!)

- Single Event Effects (SEE) – high energy heavy ions
  - SEU: measure data upset cross-section (σ) vs. Linear Energy Transfer (LET)
  - σ = # errors / particle fluence (ions/cm²): LET = charge deposition (pC/μm)
  - Goals: low cross-section + high LET threshold
Space Exploration

All Represent Extreme Environments!
(Very Wide Temperature Swings + Radiation)

<table>
<thead>
<tr>
<th>Planet</th>
<th>$T_{\text{surface}}$ (K)</th>
<th>$T_{\text{sphere}}$ (K)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mercury</td>
<td>100-700</td>
<td>445</td>
</tr>
<tr>
<td>Venus</td>
<td>740</td>
<td>325</td>
</tr>
<tr>
<td>Earth</td>
<td>288-293</td>
<td>277</td>
</tr>
<tr>
<td>Mars</td>
<td>140-300</td>
<td>225</td>
</tr>
<tr>
<td>Jupiter</td>
<td>165</td>
<td>123</td>
</tr>
<tr>
<td>Saturn</td>
<td>134</td>
<td>90</td>
</tr>
<tr>
<td>Uranus</td>
<td>76</td>
<td>63</td>
</tr>
<tr>
<td>Neptune</td>
<td>72</td>
<td>50</td>
</tr>
<tr>
<td>Pluto</td>
<td>40</td>
<td>44</td>
</tr>
</tbody>
</table>

A Roadmap to Discovery — The President’s Vision for Space Exploration sets the following goals that will help define and guide space exploration activities through 2020 and beyond, including both robotic and manned missions.

- 2008: First test flight of the Crew Exploration Vehicle (CEV)
- 2009: Robotic landing mission to the Moon
- 2010: International Space Station assembly complete
- 2010: Space Shuttle retired
- 2011: First unmanned flight of the CEV
- 2011: Robotic mission to Mars
- 2014: First manned flight of the CEV
- 2015: Earliest human mission to the Moon
- 2015: Launch of Jupiter Explorer (JIMO)
- 2016: International Space Station human research complete
- 2020: Robotic missions to Jupiter’s moons
- 2020: Human missions to Mars
- 2020 and beyond...

John D. Cressler, MSME
Upcoming Missions

The Moon
Temperature:
• +120°C to –180°C (93K)
• 28 day cycles
• -230°C in shadowed polar craters
Radiation:
• 100 krad total dose (modest)
• single event effects (solar storms)

Europa
Temperature:
• -220°C at the poles
• -160°C at the equator
Radiation:
• 5 Mrad / 2 wks (extreme)
• single event effects
Technology Options

Commercial Technology Options for EEE:

- **Si CMOS** (bulk and SOI)
  - *cooling improves*: $I_{DS,sat}$, $g_m$, $\mu_{eff}$, $S$, $I_{off}$
  - *cooling degrades*: $V_T$, hot carrier reliability
  - *radiation tolerance*: problem without RHBD

- **SiGe HBT** (bulk and SOI)
  - *cooling improves*: $\beta$, $V_A$, $g_m$, $f_T$, $f_{max}$, $NF_{\text{min}}$
  - *cooling degrades*: $\beta$ at low currents
  - *radiation tolerance*: built-in to multi-Mrad (TID), RHBD for SEE
Outline

• Extreme Environment Electronics (EEE)
  • Using Si CMOS at Low Temperatures
  • Using SiGe HBTs at Low Temperatures
  • Building the Infrastructure for EEE
  • Summary
Cooling Bulk Si CMOS

- Devices Function Well Down to 43 K (and below)
$g_m$ / Mobility

- $\mu$ Increases as $T$ Decreases (reduction in scattering)
- $g_m$ Increases as $T$ Decreases (driven by mobility)
Reliability (Fixed L)

- Max $I_{\text{SUB}}$ Increases as $T$ Decreases (more impact ionization)
- Lifetime Degrades as $T$ Decreases (more hot carrier damage)
Reliability (Variable L)

- Max $I_{SUB}$ Increases as L Decreases (decreased drain field)
- Lifetime Degrades with Gate Length Scaling

![Graph showing the relationship between $V_{GS}$ and $I_{SUB}$](image)

- NFET
  - $W = 10$ um
  - $V_{DS} = 3.3$ V
  - $T = 300$ K

![Graph showing Lifetime vs. $1/V_D$](image)

- 10 year lifetime
- $V_D = 4.25$ V
- $V_D = 3.50$ V
- $V_D = 2.91$ V
- 5AM NFET
  - $W = 10$ um
  - Stressed at 300 K
  - @ $I_{SUB\_max}$ condition
nFET 77K Irradiation

- STI Damage Causes Serious Off-State Leakage Issues
- Leakage Can Be Mitigated Using RHBD Techniques

**nFET Biased @ $V_{GS} = 3.3V$**

- Standard W/L=10/0.5
  - $V_{DS} = 0.1V$
  - Dose rate = 1 krad/s

**Proton, $T_{RAD} = 77K$**

- Irradiated@$V_G = 3.3V$

**nFET @ $V_{GS} = 3.3V$**

- Dose rate = 1 krad/s
- Annular $W_{eff}/L=6.2/0.5$
- $V_{DS} = 0.1V$

63 MeV protons
SOI CMOS

- Similar Behavior at Cryo-T to Bulk CMOS
- Improved Radiation Response (SEE)
- Improved Operation at High-T (leakage)
SOI Radiation Response

- No Off-State Leakage (edgeless H-gate device layout)
- Some $I_D$ Degradation in Strong Inversion
  - mobility $\downarrow$, $R_{SD} \uparrow$, $V_{th} \uparrow$ with increasing total dose

63 MeV protons @ 300K
Outline

• Extreme Environment Electronics (EEE)
• Using Si CMOS at Low Temperatures
  • Using SiGe HBTs at Low Temperatures
• Building the Infrastructure for EEE
• Summary
Si BJTs at Cryo-T

- Degradation in Current Gain with Cooling (bad news)
  - driven by emitter-to-base bandgap narrowing differences
- Degradation in Speed with Cooling (bad news)
  - driven by diffusivity decrease in base transit time and base freeze-out

\[
\beta_{ideal}(T) = \frac{q D_{nb}(T) L_{pe}(T) N_{de}^+(T)}{D_{pe}(T) W_b(T) N_{ab}^-(T)} \, e^{(\Delta E_{gb}^{app} - \Delta E_{ge}^{app})/kT}
\]

\[
\tau_{b, Si}(T) = \frac{W_b^2(T)}{2 D_{nb}(T)} = \frac{q W_b^2(T)}{2 kT \mu_{nb}(T)}
\]
Putting SiGe on Si

- SiGe on Si ➔ Compressive Strain in the SiGe Layer

Bulk SiGe

Strained SiGe

Defects

Relaxed SiGe
Electrical Consequences

- **Type-I Band Alignment** (Valence Band Offset = 74 meV / 10% Ge)
- **Hole Mobility Enhancement** (good news)

150 meV grading across 100 nm = 15 kV/cm electric field!
The SiGe HBT

The Idea: Put Graded Ge Layer into the Base of a Si BJT

Primary Consequences:

- smaller base bandgap increases electron injection \( (\beta \uparrow) \)
- field from graded base bandgap decreases base transit time \( (f_T \uparrow) \)
- base bandgap grading produces higher Early voltage \( (V_A \uparrow) \)
- decouples device performance metrics from base doping profile

\[
\frac{\beta_{\text{SiGe}}}{\beta_{\text{Si}}} \bigg|_{V_{BE}} = \Xi = \left\{ \frac{\tilde{\gamma} \tilde{\eta} \Delta E_{G,\text{Ge}}(\text{grade})/kT \; e^{\Delta E_{G,\text{Ge}}(0)/kT}}{1 - e^{-\Delta E_{G,\text{Ge}}(\text{grade})/kT}} \right\}
\]

\[
\frac{\tau_{b,\text{SiGe}}}{\tau_{b,\text{Si}}} = \frac{2}{\tilde{\eta}} \frac{kT}{\Delta E_{G,\text{Ge}}(\text{grade})} \left\{ \frac{kT}{\Delta E_{G,\text{Ge}}(\text{grade})} \left[ 1 - e^{-\Delta E_{G,\text{Ge}}(\text{grade})/kT} \right] \right\}
\]

\[
\frac{V_{A,\text{SiGe}}}{V_{A,\text{Si}}} \bigg|_{V_{BE}} = \Theta \approx e^{\Delta E_{G,\text{Ge}}(\text{grade})/kT} \left[ 1 - \frac{1 - e^{-\Delta E_{G,\text{Ge}}(\text{grade})/kT}}{\Delta E_{G,\text{Ge}}(\text{grade})/kT} \right]
\]

SiGe is a Natural Fit for Analog / RF Apps
The SiGe HBT

- Conventional Shallow and Deep Trench Isolation + CMOS BEOL
- Unconditionally Stable, UHV/CVD SiGe Epitaxial Base
- **100% Si Manufacturing Compatibility**
- SiGe HBT + Si CMOS on wafer

SiGe = III-V Speed + Si Manufacturing Win-Win!
Performance Trends

- SiGe HBTs Out-Perform RF-CMOS by 2 Generations
SiGe Applications

Some Application Bands for SiGe IC’s

Defense

Navigation

Automotive

Communications

SiGe Analog/RF ICs Are a Major Driver!
SiGe Performance Limits

- Half-TeraHertz SiGe HBTs Are Clearly Possible (at modest lith)
- Both $f_T$ and $f_{\text{max}}$ above 500 GHz at Cryo-T ($T =$ scaling knob)
- Goal: Useful BV @ 500 GHz ($BV_{\text{CEO}} > 1.5\,\text{V} + BV_{\text{CBO}} > 5.5\,\text{V}$)

200-500 GHz @ 130 nm Node!
New Opportunities

- **SiGe for Radar Systems**
  - DoD phased arrays (2-10 GHz and up) + automotive (24, 77 GHz)

- **SiGe for Millimeter-wave Communications / THz Imaging**
  - Gb/s wireless (60, 94 GHz) / imaging systems (100-300 GHz)

- **SiGe for Analog Applications**
  - data conversion (ADC limits) + the emerging role of C-SiGe (nnp + pnp)

- **SiGe for Extreme Environment Electronics**
  - extreme temperatures (4K to 300C)
  - radiation (e.g., space systems)
  - explore performance limits of SiGe (goal: 1 THz aggregate \( f_T + f_{\text{max}} \))

- **SiGe for Enhanced Dynamic Range Systems**
  - improved understanding of linearity / extreme wideband transceivers
The Idea: Put Graded Ge Layer into the Base of a Si BJT

Primary Consequences:

• smaller base bandgap increases electron injection ($\beta \uparrow$)
• field from graded base bandgap decreases base transit time ($f_T \uparrow$)
• base bandgap grading produces higher Early voltage ($V_A \uparrow$)

\[
\frac{\beta_{SiGe}}{\beta_{Si}} \bigg|_{V_{BE}} = \Xi = \left\{ \frac{\Delta E_{g,Ge}(grade)/kT}{1 - e^{-\Delta E_{g,Ge}(grade)/kT}} \right\}
\]

\[
\frac{\tau_{b,SiGe}}{\tau_{b,Si}} = \frac{2}{\tilde{\eta}} \Delta E_{g,Ge}(grade) \left\{ 1 - \frac{kT}{\Delta E_{g,Ge}(grade)} \left[ 1 - e^{-\Delta E_{g,Ge}(grade)/kT} \right] \right\}
\]

\[
\frac{V_{A,Ge}}{V_{A,Si}} \bigg|_{V_{BE}} = \Theta \approx e^{\Delta E_{g,Ge}(grade)/kT} \left[ \frac{1 - e^{-\Delta E_{g,Ge}(grade)/kT}}{\Delta E_{g,Ge}(grade)/kT} \right]
\]

All $kT$ Factors Are Arranged to Help at Cryo-T!
SiGe HBTs at Cryo-T

SiGe Exhibits Very High Speed at Very Low Power!

IBM SiGe 5AM
Reliability

- Extreme Mixed-Mode Stress Applied (High $J_C$ + High $V_{CB}$)
- SiGe HBTs Meets System Reliability Needs at Cryo-T
Impact of Scaling

- 200 GHz SiGe HBTs (3rd Generation) Work **VERY** Well at 77K

Will Support Cryo-T mm-wave Circuits!
Cryogenic SiGe LNAs

Record SiGe LNA Noise Figure at 15 K (Not Optimized!)

- $T_{eff} < 20$ K (noise T)
- $NF < 0.3$ dB (8.5-10.5 GHz)
- Gain $> 20$ dB
- $dc$ power $< 2$ mW

Getting Close to HEMT Noise Records!

… with 3rd Generation SiGe
High-Temperatures

- How About SiGe for High-temperature (200-300C) Circuits?
- Degradation, But Plenty of Performance Left!
- Device-level Reliability Looks Good

![Graphs showing gain and frequency plots for high-temperature SiGe circuits.](image-url)
Total-Dose Response

- Multi-Mrad Total Dose Hardness (with no intentional hardening!)
  - ionization + displacement damage very minimal over T; no ELDRS!
- Radiation Hardness Due to Epitaxial Base Structure (not Ge)
  - thin emitter-base spacer + heavily doped extrinsic base + very thin base

63 MeV protons @ 5x10^{13} p/cm^2 = 6.7 Mrad TID!
Cryo-T Irradiation

• SiGe HBT Still Multi-Mrad Hard at 77K

![Graph showing forward Gummel plots for 5AM SiGe HBT at 77 K and 300 K with labels for IC, IB, and VBE. ]
Extreme Dose / Fluence

- Peak $\beta > 50$ after $1 \times 10^{15} \text{p/cm}^2 / 100 \text{ Mrad}$

\[ \frac{\beta_{\text{post}}}{\beta_{\text{pre}}} \text{ near peak } f_T \]

- CERN
- ATLAS upgrade
- UC Santa Cruz
- DOE Leverage

100 Mrad!
Single Event Effects

- Observed SEU Sensitivity in SiGe HBT Shift Registers
  - low LET threshold + high saturated cross-section (bad news!)

SEU: TCAD to Circuits

“TCAD Ion Strike”

New RHBD SiGe Latch

Standard Master Slave Latch

SEU “Soft”
SEU RHBD Success!

- Reduce Tx-Tx Feedback Coupling Internal to the Latch
- Circuit Architecture Changes + Transistor Layout Changes

Future - Eliminate TMR & Be Faster!
Path - Build a Rad-Hard System!

(no errors!)
SEU at Cryo-T

- Proton $\sigma_{EI}$ is 5 Orders of Magnitude Less Than Heavy Ion $\sigma_{EI}$
- 3X Increase in Proton Cross-section at 77K for Std. M/S ... BUT
- DI RHBD is Error-free < 2 Gbit/s and Insensitive to Temperature

![Graph showing data rate vs. proton cross-section]
Outline

• Extreme Environment Electronics (EEE)
• Using Si CMOS at Low Temperatures
• Using SiGe HBTs at Low Temperatures
• Building the Infrastructure for EEE
• Summary
Develop and Demonstrate Extreme Environment Electronic Components Required for Distributed Architecture Lunar / Martian Robotic / Vehicular Systems Using SiGe Technology

Objectives:

Extreme Environment Requirements: (e.g., Lunar)
- +120C (day) to -180C (night) + cycling
- radiation (TID + SEU tolerant)

Major Project Goals / Approach:
- prove SiGe BiCMOS technology for +120C to -180C applications
- develop mixed-signal electronics with proven extreme T + rad capability
- develop best-practice extreme T range circuit design approaches
- deliver compact modeling tools for circuit design (design suite)
- deliver requisite mixed-signal circuit components (component library)
- deliver robust packaging for these circuits (integrated multi-chip module)
- deliver a functional SiGe REU prototype meeting lunar specs
- validate device + circuit + package reliability
- develop a robust maturation path for NASA mission insertion (TRL-6)
A World Class Team!

- **Georgia Tech** (Device Technology IPT lead)
  - John Cressler *et al.* (PI, devices, reliability, circuits)
  - Cliff Eckert (program management, reporting)

- **Auburn University** (Packaging IPT lead)
  - Wayne Johnson *et al.* (packaging); Foster Dai *et al.* (circuits); Guofu Niu *et al.* (devices)

- **University of Tennessee** (Circuits IPT lead)
  - Ben Blalock *et al.* (circuits)

- **University of Maryland** (Reliability IPT lead)
  - Patrick McCluskey *et al.* (reliability, package physics-of-failure modeling)

- **Vanderbilt University**
  - Mike Alles, Robert Reed *et al.* (radiation effects, TCAD modeling)

- **JPL** (Applications IPT lead)
  - Mohammad Mojarradi *et al.* (applications, reliability testing, circuits)

- **Boeing**
  - Leora Peltz *et al.* (applications, circuits)

- **University of Arkansas / Lynguent** (Modeling IPT lead)
  - Alan Mantooth / Jim Holmes *et al.* (modeling, circuits)

- **BAE Systems**
  - Richard Berger, Ray Garbos *et al.* (REU architecture, maturation, applications)

- **IBM**
  - Alvin Joseph *et al.* (SiGe technology, fabrication)

A World Class Team!
Remote Electronics Unit

The X-33 Remote Health Unit, circa 1998

The NASA ETDP SiGe Remote Electronics Unit, circa 2009

**Specifications**

- 5” x 3” x 6.75” = 101 in³
- 11 kg
- 17 Watts
- -55°C to +125°C

**Goals**

- 1.5” x 1.5” x 0.5” = 1.1 in³ \((100x)\)
- < 1 kg \((10x)\)
- < 2 Watts \((10x)\)
- -180°C to +125°C, rad tolerant

**Supports Many Sensor Types:**
Temperature, Strain, Pressure, Acceleration, Vibration, Heat Flux, Position, etc.

Use This SiGe REU as a Remote Vehicle Health Monitoring Node
Summary

• Low-Temperature Electronics
  - a key niche in the extreme environment electronics portfolio
  - a key need for envisioned planetary exploration
  - cryo-T is often needed in tandem with radiation exposure

• Si CMOS
  - many performance metrics improve with cooling
  - reliability issues can be a concern (address with longer L)
  - radiation exposure can be a concern (may need RHBD)
  - SOI can help on the radiation vulnerability

• SiGe HBTs
  - all performance metrics improve with cooling (natural for EEE)
  - major new lunar application for +120C to -180C = infrastructure
  - built-in multi-Mrad total dose hardness
  - use RHBD for SEE mitigation
  - SiGe Technology = SiGe HBT + Si CMOS (bulk + SOI)