Project No. A-3498 (under E-21-669/Paris/EE)

Project Director: N. W. Cox

Sponsor: AFSC, Rome Air Development Center, Griffiss AFB, NY

Type Agreement: Contract F30602-81-C-0185, Mod. P00013

Award Period: From 3/9/83 To 9/30/84

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Title: RADC Post-Doctoral Program

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OCA Contact: William F. Brown, Ext. 4820

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2) Sponsor Admin/Contractual Matters:

T. A. Bryant
ONR RR
Campus

Defense Priority Rating: DO-A7

Military Security Classification: None

(or) Company/Industrial Proprietary: ---

RESTRICTIONS

See Attached Gov't Supplemental Information Sheet for Additional Requirements.

Travel: Foreign travel must have prior approval – Contact OCA in each case. Domestic travel requires sponsor approval where total will exceed greater of $500 or 125% of approved proposal budget category.

Equipment: Title vests with None proposed

COMMENTS:

Mod. P00013 adds $50,000 to fund Task Assignment #N-3-5713 (3/9/83 - 9/30/83) distributed as follows:

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$50,000

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SPONSORED PROJECT TERMINATION/CLOSEOUT SHEET

Date 7/1/85

Project No. A-3498

Includes Subproject No.(s) N/A

Project Director(s) N. W. Cox GTRC / IXKIX

Sponsor AFSC, Rome Air Development Center, Griffiss AFB, NY

Title RADC Post-Doctoral Program

Effective Completion Date: 9/30/83 (Performance) 10/31/83 (Reports)

Grant/Contract Closeout Actions Remaining: Closeout this sub number only.

- [ ] None
- [ ] Final Invoice or Final Fiscal Report
- [ ] Closing Documents
- [ ] Final Report of Inventions
- [ ] Govt. Property Inventory & Related Certificate
- [ ] Classified Material Certificate
- [ ] Other ____________

Continues Project No. ____________________________ Continued by Project No. ____________________________

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Other _______________

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FORM OCA 69.285
RELIABILITY PHYSICS OF MICROWAVE MICROCIRCUITS

By
N. W. Cox

Prepared for
Air Force System Command
Rome Air Development Center
Griffis AFB, NY 13441

Under
Contract No. F30602-81-C-0185 Mod. P00013

Report for Period 9 March 1983 - 30 March 1984

30 March 1984

GEORGIA INSTITUTE OF TECHNOLOGY
A Unit of the University System of Georgia
Engineering Experiment Station
Atlanta, Georgia 30332
RELIABILITY PHYSICS OF MICROWAVE MICROCIRCUITS

FINAL REPORT

N. W. Cox
Engineering Experiment Station
Georgia Institute of Technology
Atlanta, Georgia 30332

Report for Period 9 March 1983 - 30 March 1984

Prepared for

Air Force System Command
Rome Air Development Center
Griffis AFB, NY 13441

30 March 1984
The objective of this study is to examine the methodology for studying reliability of GaAs integrated circuits with emphasis on analog functions (MMICs). Involved in this study are elements bearing on GaAs IC design and processing, functional and parametric testing, reliability characterization and fault isolation, and failure analysis methods. Major tasks in the study are to generate recommendations for funding by DoD in the area of GaAs IC reliability, to present the state-of-the-art for this technology, and to define the status of and plans for
reliability testing by industrial firms.

Based on the state-of-the-art, the rapid growth anticipated, and recommendations from industrial firms, the timing is appropriate to initiate small lot qualification studies involving step stress testing of 10-30 GaAs MMICs. It is suggested that such studies be initiated promptly since these devices are beginning to emerge from the R&D laboratory and enter production. Other recommendations include:

- Standardization of wafer test patterns to be used by all DoD vendors.
- Characterization of functional blocks is best accomplished by chip layouts which allow scribing or sawing for isolation or by placing blocks on individual chips.
- RF bias should be involved in stress tests.
- Polyimides should be investigated.
- Studies of radiation effects are needed.
- Better methods of channel temperature measurement are needed.
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I. INTRODUCTION

The objective of this study is to examine the methodology for studying reliability of GaAs integrated circuits with emphasis on analog functions (MMICs). Involved in the study are elements bearing on GaAs IC design and processing, functional and parametric testing, reliability characterization and fault isolation, and failure analysis methods. Major tasks in the study are to generate recommendations for funding by DoD in the area of GaAs IC reliability, to present the state-of-the-art for this technology, and to define the status of and plans for reliability testing by industrial firms.

In order to implement logical decisions regarding reliability studies on GaAs MMICs, it is imperative to have a firm understanding of the current state of this technology as well as its direction and rate of growth. The sections which follow attempt to accomplish this objective utilizing published papers and interviews with the major firms involved in this technology. As defined in the original statement of work, the study has concentrated on analog circuits, but due to the similarity of GaAs digital technology, it has also been considered to a lesser extent, particularly to show the magnitude of the effort focused on GaAs IC technology.
II. STATUS OF GaAs IC TECHNOLOGY

II.1 Advantages and Disadvantages of GaAs

The interest in GaAs stems from its fundamental advantages for low-noise, high speed, and high frequency applications. It is also well suited for transmitter applications where medium power levels are required. These advantages for GaAs are based on the velocity versus electric field characteristic for electrons which reveals an electron drift mobility which is approximately six times higher than for Silicon. The maximum drift velocity for GaAs is also considerably higher, thus shortening the transit time of carriers and increasing the maximum frequency of operation for devices. This short transit time provides for nonequilibrium conditions in devices with dimensions less than 0.5 μm, particularly at low temperatures, thus increasing the speed of operation. The availability of semi-insulating GaAs substrates provides another obvious advantage over Si since it yields inherent device isolation. This semi-insulating GaAs substrate reduces interconnect capacitance which becomes critical as the level of integration increases.

Gallium Arsenide devices also appear to provide advantages over Si with respect to radiation hardness. This improved radiation hardness is a consequence of the relatively short lifetime of carriers in GaAs. However, additional research is required to thoroughly assess the effects of neutron and ionizing radiation on device and circuit performance. These advantages
make GaAs a logical choice for high radiation environments including spacecraft and missiles. In addition to its advantages in a radiation environment, GaAs offers improved high and low temperature operation. The high temperature characteristics suggest its use for integration in hostile environments such as engines for sensors and controls. Numerous investigations are also underway to explore the advantages of low temperature operation of GaAs digital logic and low noise amplifiers for ultra high speed and low noise applications.

A major disadvantage of GaAs has been difficulties in obtaining an adequate supply of large (> 3 inch), low price, high quality, semi-insulating substrates. In the past five years, significant improvements have been made in substrate quality, size and yield. Prior to that time, substrate quality and variability were a major deterrent to the development of a viable GaAs IC technology. More recently, Czochralski-grown (LEC) ingots are resulting in reproducible, three inch, round GaAs semi-insulating wafers with purity and crystal perfection approaching those required for IC applications. Even though progress has been made in improving GaAs substrates, work continues to reduce the dislocation densities. Typical EPD counts for LEC wafers are $10^4 - 10^5$/cm$^2$.

Another problem area for GaAs ICs is the sophisticated processing required to fabricate these complex ICs which in many instances have submicron geometries. State-of-the-art processing technology including electron beam lithography, ion beam milling,
RIE, plasma etching, etc. are typically required. The complexity of the processing, in addition to requiring significant investments in capital equipment, results in relatively low yields. Much effort is being focused on the development of processes, such as the self-aligned gate, which can increase yields and thus reduce costs. In addition, work is required to develop automated wafer handling and computerized RF and dc testing techniques.

II.2 Status of Technology

Over the past eight years the GaAs IC technology has advanced from experimentation with small scale circuits to development of LSI circuits containing tens of thousands of devices. The first LSI circuit demonstrated by Rockwell in 1980 was an 8x8 multiplier containing approximately 6,000 transistors and diodes. Technology has progressed to the point where NTT and Fujitsu have both recently announced 4kb static RAMs employing over 26,000 FETs. Over the same time frame, GaAs analog ICs have advanced in the level of integration to subsystems such as receivers.

GaAs monolithic integrated circuits offer the potential of drastically altering the design, implementation and applications of microwave systems. Generally speaking, however, these GaAs ICs are not yet finding their way into system hardware. For the most part, the technology remains in the laboratory with the primary emphasis being to demonstrate more complex or higher performance circuits. Only recently has attention seemed to turn
towards increasing chips yields to make this technology viable for system applications. If this technology is to ever make the transition from the research lab to hardware, this emphasis on yield is essential. Many manufacturing technology problems must be solved before large volumes of circuits can be produced at cost levels commensurate with system needs. The practical level of integration and the costs are primarily determined by the yields. As monolithic chip complexity increases to the subsystem level, yields will decrease and cost will increase to the point where it becomes advantageous to partition the monolithic circuit into multiple chips and use hybrid MIC technology for interconnection. There are indications that this level is currently being reached as some researchers are expressing misgivings regarding integration complexity and are beginning to suggest the development of common modules such as amplifiers, mixers, sources, etc. where volumes would be high and cost low. Additional development and prototype production runs will be required to determine where the breakpoint on chip complexity will occur.

The support by DoD of manufacturing technology programs for MMICs is considered essential. The importance of DoD involvement in this technology is indicated by the fact that virtually all of the research and development on GaAs FETs and ICs has been funded by DoD. The DARPA GaAs foundries are expected to provide this emphasis for digital circuits, but only indirect assistance will be available for analog circuits.
II.3 Direction of Development Efforts

To gain a better understanding of the types of monolithic GaAs ICs under development, a review of the published literature from 1980-1983 was performed. Each paper was classified by year according to the type of component. A summary of these data are given in Tables 1 and 2. This survey was by no means exhaustive, and these two charts serve only to illustrate where the general emphasis is being placed. As seen from the charts, the analog ICs have concentrated on amplifiers, switches, phase shifters and receivers. The digital ICs have emphasized RAMs, counters, dividers, ring oscillators and gate arrays. These data don't appear surprising since there are obvious commercial and military markets for both amplifiers and memories. An interesting observation is the obvious concentration of 1983 efforts on RAMs, gate arrays, and low and medium power amplifiers. Apparently, research efforts are becoming more focused on specific components as laboratories gain experience with the technology and become more production conscious.

II.4 Market Projections

A key factor in the decisions regarding MMIC reliability studies are the direction and growth projections for this technology. In a recent presentation at the 1983 GaAs IC Symposium, G.E. Avery of Technology Insight Consultants reviewed major application areas and presented forecasts of the GaAs IC market including digital, analog and optoelectronic circuits.¹
Table 1. GaAs MONOLITHIC ANALOG INTEGRATED CIRCUITS

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<td>Power Amplifier</td>
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<td>3</td>
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<tr>
<td>Switch</td>
<td>2</td>
<td>3</td>
<td>1</td>
<td></td>
<td>6</td>
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<tr>
<td>Phase Shifter</td>
<td>4</td>
<td>1</td>
<td></td>
<td></td>
<td>5</td>
</tr>
<tr>
<td>Receiver</td>
<td>2</td>
<td>2</td>
<td>1</td>
<td></td>
<td>5</td>
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<tr>
<td>Modulator/Demodulator</td>
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<td></td>
<td>4</td>
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<tr>
<td>Oscillator</td>
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<td>1</td>
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<tr>
<td>Mixer</td>
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Sources: GaAs IC Symposium  
Solid State Circuits Conference  
MTT Transactions  
ED Transactions  
Electronic Letters
Table 2. GaAs MONOLITHIC DIGITAL INTEGRATED CIRCUITS

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<td>5</td>
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<td>Gate Array</td>
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<td>Pseudo-Random Generator</td>
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<td>Word Generator</td>
<td></td>
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<td>Demodulator</td>
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sources: GaAs IC Symposium  
Solid State Circuits Conference  
MTT Transactions  
ED Transactions  
Electronic Letters
The market forecasts presented below were derived from this address which was not published in the symposium proceedings.

The rapid progress made in development of GaAs ICs has opened numerous areas of application including government/military, communications, computers and instrumentation. These applications all utilized the high speed performance characteristics of the GaAs technology. Specific applications in these general areas are enumerated below.

Military/Government
- Expendable decoys
- Satellite signal processors
- Advanced phased arrays
- Space-based radars
- Military computers
- Communications
- Navigation

Communications
- Direct Broadcast Satellite receivers
- Broadband fiber optic links
- Microwave receivers
- Digital radios

Computers
- Supercomputers
- Signal processing
- Modeling and simulation
The early development of GaAs IC technology was largely a result of military requirements. The military market will continue to dominate for this decade, but communications and data processing applications will also provide strong incentives.

Based on these applications, Avery predicted the general growth curves of Figures 1 and 2 for GaAs ICs. Note that these are rough sketches based on his slides, but they are adequate to show the important trends he is predicting. The assumptions stated for this market forecast are:

- Real US GNP growth resumes in 1983
- Market growth will be demand driven and supplier limited
- Japanese market will be served by Japan
- Market growth is only loosely coupled to Si IC market growth, i.e. not competitive technologies

A key feature of these predictions is that a total GaAs IC market of $10B is forecast in 1993, up from something considerably less than $100M in 1983. Of this $10B 1993 market, approximately $5B is projected to be in the digital IC area with
Figure 1. Predicted Growth of GaAs IC Market.

Figure 2. Predicted Growth of GaAs IC Market Segments.
the remaining $5B approximately equally split between analog and optoelectronic circuits. Note that this represents a tremendous growth in optoelectronic circuits since the present state of this technology is certainly not commensurate with production. Optoelectronic ICs have only within the past three or four years been demonstrated, and much research and development remains. The future impact of GaAs (perhaps AlGaAs, GaInAs or GaInAsP) optoelectronic ICs does not appear to be in doubt, however, I seriously question whether the technology will mature rapidly enough to generate a $2-3B market in 1993.

As seen from Figure 2, the analog GaAs IC market will dominate over the digital market for the next five years at which time production of digital circuits will begin to surpass analog. Note, however, that these projects could be drastically modified if a commercial application such as direct broadcast satellite (DBS) develops more or less rapidly than anticipated.

These market projects obviously must be used only as guidelines for future planning. The major conclusion to be drawn is that GaAs IC technology is expected to produce an impressive market, both commercial and military, in the next ten years.

If this market is to grow as projected, it is essential that reliability efforts begin immediately due to the extensive time required for these studies. Full scale reliability testing of specific circuits can easily consume three years in the study, definition, testing and analysis phases. Furthermore, it is doubtful, as described later in this report, that such full scale
testing is appropriate at the present time.

Another conclusion from these market projections is that the reliability of optoelectronic ICs should begin to be considered in the next three or four years. The high current densities and temperatures in laser diodes, for example, makes such reliability studies essential at an early time frame so as to guide the process development.

The number of firms involved in GaAs IC technology is large (by one count 43 in the U.S., 8 European and 10 Japanese). However, these firms are for the most part captive suppliers, and only five in the U.S. have indicated a commitment to the merchant market. Harris Microwave is the only one with GaAs ICs currently available commercially. These digital ICs being offered by Harris are expected to be followed shortly by a wideband IC amplifier from Avantek.

As discussed in Section II.2, improvements in yield are essential if the market forecasts discussed above are to be achieved. Yields as high as 60–65% have been reported, with 1 μm technology, however, normal yields are in the range of several percent. This is not surprising in light of the fact that most researchers have simply been trying to demonstrate the capabilities of this technology and have not been concerned with yield. This emphasis appears to be changing, but much concentration on controlling yield factors will be required. Since DoD is the prime source of funding for this technology, yield improvements should be emphasized in future programs.
III. GaAs FET RELIABILITY

III.1 GaAs FET Reliability Studies

The absence of reliability data on GaAs monolithic integrated circuits suggests an examination of GaAs FET reliability to ascertain applicability to the IC problem. Obviously, the question of GaAs IC reliability is a much more complex problem than that of discrete FETs. This difference results from the utilization of different metal systems and processes in some instances, interconnections, requirements for insulators to provide for a second level metal system, utilization of passive components, the large areas of chips, and requirements for different dc and RF test procedures. Furthermore, there exist major differences in the reliability of low noise and power FETs as would be expected. Reliability data regarding low noise FETs are not applicable to power devices as a result of the dissimilar regimes of operation with regard to rf amplitude, dc operating conditions, and temperature. The failure modes of the two types of discrete devices differ, with catastrophic burnout (defined as a sudden thermal runaway process leading to fusing of the metalization of one or more cells) being a primary cause of failure in power FETs only.

Relatively few studies have been conducted to examine reliability of GaAs power FETs; the situation with low noise devices is however quite different. Firms such as Bell Telephone Laboratories and Hughes Space and Communication Division has
conducted extensive reliability testing of low noise FETs. Hughes for example has analyzed the best low noise devices available from both domestic and foreign manufacturers for use in satellite receivers. The consensus of opinion resulting from these and others studies on low noise devices is that if the devices are fabricated "properly" (i.e. without processing errors) they are extremely reliable and have no inherent reliability problems. Reliability data such as $10^8$ hours MTTF are reported at $40^\circ C$ channel temperatures for these devices using Al, TiW/Au or TiPt/Au schottky barrier gates.\(^{(2)}\) The major difference in the various low noise devices is the Schottky gate metalization. Aluminum has been shown to be reliable, however, the refractory metals TiW or TiPt appear to be favored for high reliability applications. Bell Laboratory has achieved excellent reliability with aluminum gates and continues to utilize this approach. The ohmic contacts for GaAs FETs are almost universally Au-Ge-Ni with N$^+$ contact layers utilized for the highest performance devices. In general, if the ohmic contact metals are deposited and alloyed properly, they have been shown to produce very reliable contacts. However, this contact technology is an art with each manufacturer having their own procedure for achieving good contacts. Parameters such as the thickness of each component of the tri-metal system, deposition temperature, alloying temperature, alloying time, and rate of change of alloying temperature are all parameters which differ for various manufacturers. A less sophisticated contact process is certainly desirable, but the
The present approach appears to present no major reliability problem even through it likely is an important yield factor.

As indicated above, low noise discrete FETs have been shown to be very reliable assuming the absence of processing problems. The predominant failure mechanism observed during thermal stress of these devices is a degradation of resistance between the gate and drain apparently resulting from the electrical annihilation and redistribution of shallow impurity donors in the channel region \(^{(3)}\). This loss of charge in the channel after high temperatures under bias extends from under the gate towards the drain and is manifest as a reduction in \(I_{dss}\). The failure mode is believed to be out diffusion of doping impurities from the channel or in-diffusion of compensating impurities from the substrate into the channel. Regardless, the rate of charge loss is sufficiently slow that it is not considered a problem.

The two major GaAs power FET reliability studies reported in the open literature were conducted by Bell Laboratories \(^{(4)-(7)}\) and the Jet Propulsion Laboratory \(^{(8)}\). Both tests indicated extremely reliable operation with proper device design and fabrication. The Bell Laboratories study, reported in 1980-1981, was originated in 1979 and is the more comprehensive involving 265 devices fabricated in house. The devices tested had the following characteristics:

- Gate width - 2mm with 12 parallel fingers
- Gate length - 2 \(\mu\)m aluminum
- Material - VPE with buffer and Cr-doped substrate
o Structure - recessed gate
o Ohmic contacts - Au-Ge, Ag, Au with Ti, Pt, Au overlay and n+ region under source and drain
o Passivation - silicon nitride
o Performance - 5W output at 4 GHz

These devices were stressed under dc bias with and without RF drive at channel temperatures of 175, 210, and 250°C for a total of one-million device-hours. The screening procedure utilized with these devices was to apply at room temperature a drain source voltage approximately twice the normal bias point and drain current which was roughly 0.5 \( I_{dss} \). This screening bias power was at least 2.5 times the normal bias power and was applied for 10s. Approximately 10% of the devices were rejected by this test.

The results of the Bell Laboratories tests were excellent. None of the 265 devices failed catastrophically, previously the dominate failure mode of power GaAs FETs. This implies a conservative catastrophic failure rate below 100 FIT's (failures in \( 10^9 \) hours of operation). Degradation of device parameters was extremely slow at 210 and 250°C with no change observed at 175°C for 3000-4000 hours of aging. The primary device parameters monitored were \( I_{dss} \) and \( P_s \) with the very conservative criterion for gradual degradation being five-percent decrease in \( P_s \). These data imply an ML (mean life) of \( 5 \times 10^8 \)h and a gradual degradation failure rate of 10 FIT's at 110°C. The very slow
gradual degradation failure mode was primarily due to deterioration of the epitaxial material similar to that discussed previously for the low noise devices. This failure mode was sufficiently slow to be of no practical concern. Both the schottky gate and ohmic contacts showed no noticeable degradation over periods of 164h at 285°C.

A most surprising result of the Bell Laboratories RF life tests is that no significant reliability difference was observed between aging test with and without RF drive for periods of 3000h at 250°C channel temperatures. These tests, however, do not assure such agreement over longer time periods. Forward gate conduction was observed in these RF tests with up to 60 ma of rectified dc gate current, implying $2.5 \times 10^5$ A/cm² for each gate finger; no gate electromigration was observed.

A JPL life test was reported in 1983 (8) and involved twenty-four, 0.75w, X-band, three-stage, hybrid power amplifiers. The GaAs FET's were commercial-grade MSC devices without burnin. The duration of the test was 24,000 hours involving ambient temperatures of 75 and 125°C in RF operation. Parametric data used for evaluation included Rf power level, phase and amplitude transfer characteristics, input impedance and individual stage dc bias. The failure criterion for the amplifiers involved a combined phase and amplitude deviation. The specified channel temperature is conservative since it is based on manufacturer quoted thermal resistance measured using an infrared microscope with a spot size 30 times the gate length.
The measured temperature is thus an average temperature with the gate channel being somewhat hotter. The quoted channel temperatures ranged from 83 to 95°C for the 3 stages with a 75°C ambient and 133 to 149°C for a 125°C ambient.

No catastrophic failures occurred during the 24,000 hours of testing. Only one amplifier (containing three FET's) out of 16 held at 75°C ambient (83°C channel) for 24,000h showed degradation. This failure was traced to tungsten and nickel deposits on the gate fingers. Eight of the amplifiers were subjected to 16,000h at 125°C ambient after surviving 8000h at 75°C. Of the eight amplifiers aged at the higher 125°C ambient (133 to 149°C channel), four developed failures. Note that the actual channel temperature was higher than this range due to the thermal resistance measurement technique. Failure analysis had not been completed on these devices to ascertain cause of the failures prior to publication. These tests are certainly encouraging regarding reliability of GaAs power FETs. Obviously, the failure analysis results are needed to determine the failure modes and ascertain the seriousness of the failures. Furthermore, testing of much larger numbers of devices is required to obtain good statistical data for reliability projection.

A major conclusion from these two studies is that the catastrophic burnout problem, which had been the dominate failure mode of earlier GaAs power FET's, has been alleviated with improved device design and processing. Additional effort is obviously required to look at other device structures and
Hughes Space and Communications Division has performed extensive reliability tests on both low noise and power GaAs FETs as well as some digital GaAs ICs. Early Cr-Au metalization deteriorated rapidly, while Ti-W-Au gates were stable at 175°C. They are redesigning the test fixture for 250°C in order to continue testing. One vendor used SiO₂ for isolation, and some cracks were observed after the tests. Other devices with air bridges experienced no failures. Electromigration has been observed on FETs from two vendors when subjected to thermal soak at 250°C. Also, cracks have been observed in several chips after 1000 hours at 250°C. A major problem is the development of screening procedures for these reliability tests.

III.2 RF Drive Considerations

A question of considerable significance in defining reliability testing procedures for both GaAs FETs and MMIC's is the importance of RF drive during aging. The requirement for RF drive at microwave frequencies greatly increases the cost and complexity of such tests. As discussed above, Bell Laboratories determined that reliability tests on GaAs power FETs with and without Rf drive showed no significant difference up to 3000h at 250°C channel temperature. This conclusion is not necessarily valid for more extended periods of aging. Many other researchers feel strongly that RF drive is critical to such aging experiments, and that tests with dc stress only are not very useful for reliability projections. Raytheon SMDO for example has
performed accelerated life tests under RF drive on 14 power, Ku-band FETs. Devices were tested at a net dc gate current of 1 mA, typical of high drive conditions.\(^9\) Raytheon felt that degradation modes, not normally observed under dc stress, would likely be produced under these conditions. As reported by several other researchers, a failure mode involving gradual gain degradation was observed at 228°C channel temperatures. This mode did not appear to be related to the RF drive or gate current. An MTTF of 2100h at 228°C was established for these devices using a failure criteria of 1 dB drop in gain.

A catastrophic failure mode was also observed in the Raytheon tests at 280°C. This failure mechanism could be related to the gate current and such a tentative explanation was proposed, but additional testing is necessary to verify. An approximate MTTF for this failure mode was 120 at 280°C.

At the present time no definite conclusions can be drawn regarding the necessity of RF drive during aging experiments. However, there are adequate data and opinionated researchers to suggest that RF drive should be included in reliability testing of discrete devices as well as ICs until definite decisions can be made.
IV. GaAs IC RELIABILITY

IV.1 Comparison of Discrete and Monolithic Testing

As discussed in Section III, little if any reliability data or experience exist for GaAs integrated circuits. Consequently, reliability studies and techniques for discrete GaAs FETs are being considered for their applicability to monolithic circuits. This extrapolation must be approached carefully since there are areas in which the GaAs monolithic circuits are unique in comparison to discrete devices as well as conventional Si integrated circuits.

The most obvious difference between testing of discrete devices and integrated circuits is the involvement of additional elements: resistors, capacitors, inductors, transmission lines, and diodes. With a more mature integrated circuit technology, the passive elements would not be expected to be a driving factor for reliability. This is not necessarily the case with GaAs circuits since the processing technology remains very much in a state of flux. The firms involved in this technology have not standardized on critical factors such as metalization systems and deposition techniques, insulating and passivating films and their deposition, gate structure, etc. Consequently, stress testing of these passive elements remains an area of concern even though most researchers don't anticipate any fundamental problems. Rather simple tests could be defined to investigate reliability of these passive elements.
Avantek's approach to reliability testing of MMICs has been to evaluate the discrete devices (FETs, resistors, capacitors, inductors, etc.) and then integrate and project reliability for the MMIC based on the discrete device data. Obviously this approach is helpful in establishing a general level of confidence in reliability of the MMIC, but testing of the complete MMIC chip is required due to the more sophisticated processing required for chip fabrication and due to interactions (thermal and electrical) among the components. Note that this evaluation of the discrete devices is important and should precede full scale reliability testing. Considerable testing of discrete devices, such as FETs, has been performed previously as discussed in Section III.1. The wafer test patterns discussed in Section IV.5 often contain discrete devices which can be used for such evaluation.

Several firms interviewed have experienced problems with capacitor dielectrics which have limited the yield and reliability of their GaAs circuits. However, the capacitor dielectric problem appears to have been solved by most, at least with respect to yield, simply by changing their deposition process or by better process control.

Both thin film and ion implanted resistor technologies are being utilized in GaAs integrated circuits. Reliability problems have been mentioned with the thin film approach, but there is no reason to suspect this is a fundamental problem. Metalization systems such as Ti are known to be stable on GaAs. The problems being experienced are likely due to improper choice of the
RF and dc testing of the GaAs integrated circuits will be much more complex than for discrete GaAs devices or Si integrated circuits. Circuits such as a phased array module will involve S-parameter, power level and noise figure measurements at frequencies as high as Ku-Band. The accuracy required is on the order of several degrees in phase and 0.1 - 0.5 dB in amplitude, noise figure and power level. The measurement accuracy and repeatability requirements imply automated systems such as the Hewlett Packard automated network analyzer and automated noise figure measurement systems. The cost of such measurement systems are very high ($200 K for the ANA) but will be well justified and likely required. Utilization of dc tests will be emphasized for GaAs ICs, but relating dc characteristics to RF performance is typically extremely difficult. The need for extensive RF characterization is thus assured. Stress tests on these circuits will require special RF inputs for proper evaluation. This could include picosecond risetime pulses and modulated microwave signals, low and high power. Careful considerations must be given to details of RF stress tests to determine which signals are required for proper device stressing.

As discussed previously for discrete GaAs FETs, determination of the channel temperature is difficult due to the precise spatial resolution required (on the order of 0.5 to 3 μm). This problem becomes much more severe and critical with monolithic GaAs circuits, particularly when power devices are
involved. These monolithic power circuits are subject to thermal coupling between devices, creating problems when attempting to determine the temperature distribution across the chip. Furthermore, there can be significant variation in channel temperatures of the FETs, thus complicating determination of the location of the maximum chip temperature. Electrical techniques are generally not applicable to temperature determination in ICs since the FET terminals are not necessarily accessible, and liquid crystal and infrared microscopy must be used. Liquid crystals have better resolution and are the more useful even though there are serious questions, as discussed in Section IV.2, regarding their use on devices which are to undergo reliability testing. Studies are certainly needed in this area.

Failure analysis/fault isolation will obviously be much more difficult with GaAs ICs than with discrete devices. However, the failure modes are likely to be very similar since the FETs are expected to be the primary reliability determining component. Dissection of the GaAs ICs for failure analysis can likely rely on some of the techniques developed for Si ICs. However, due to different metalization and insulator systems, considerable effort will be required to refine specific techniques, and the introduction of damage during dissection is always a major concern. Consequently, isolation of faults may be very limited for GaAs ICs. Hughes reported little success in this area; in many instances, dissection of the circuits introduced more problems than it solved. The refractory based metal systems being
used by many manufacturers complicate dissection of GaAs ICs. As discussed in Section IV.6, noncontacting techniques such as voltage contrast and laser probing will be helpful in fault isolation. An additional difficulty with GaAs ICs is that the technology is in a state of flux as discussed previously, and a wide variety of processing technologies are being utilized, thus complicating the development of dissection techniques.

IV.2 Channel Temperature Measurements

Determination of the maximum FET channel temperature is essential for reliability studies of discrete devices as well as integrated circuits. The power dissipation in FET structures is not uniformly distributed in the channel region but is skewed towards the drain contact. The temperature is thus nonuniform with a peak in the region between the gate and drain. State-of-the-art GaAs ICs have 0.5 to 1.0 μm gate lengths with 1 to 3 μm spacing between the gate and drain. Thus, in order to determine the peak channel temperatures in medium and high power devices and circuits, thermal measurements are desired with spatial resolution in the range of one micron. Ideally, this thermal measurement technique should have the following characteristics:

- Nondestructive - usable on actual circuits under test
- Convenient - applicable to LSI circuits as well as discrete devices
- Spatial resolution - < 1 μm
- Measurement time - < 30 minutes
- Accuracy - ±4 °C
o Response time - require < 1 μs if interested in pulsed performance

An excellent summary of the three commonly used techniques for channel temperature measurements was presented by A.C. Macpherson\(^ {10} \) and is included as Table 3. A careful examination of this table reveals that none of the three techniques; liquid crystal, infrared microscopy, and electrical satisfy all of the criteria listed above. The only techniques which appears capable of the desired spatial resolution is liquid crystal. Unfortunately, this technique requires coating of the device or circuit with the liquid crystal material and subsequent stripping if this device or circuit is to be used in actual testing. This poses a serious question regarding the effect of this coating on reliability testing, and farther studies are needed if the liquid crystal technique is to be used in this manner. Furthermore, utilization of the liquid crystal technique is time consuming, has a slow response time which prohibits its application for pulsed measurements, and is not useful in the 275 - 300°C range. The liquid crystal technique has been primarily used to characterize representative devices and not to measure thermal resistance of the devices to be used in actual testing.

Thus, none of these techniques meet the desired criteria even though they are useful and are being used for lack of better techniques. The more convenient techniques have poor spatial resolution and average the temperature over a relatively large
<table>
<thead>
<tr>
<th>Spacial Resolution</th>
<th>Requires Viewing the Device</th>
<th>Response Time</th>
<th>Temp. Error, °C</th>
<th>Degrades Device</th>
<th>Est. Overall Accuracy</th>
<th>Conveni.</th>
<th>Useful to 300°C</th>
<th>Time to Build or Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>LC</td>
<td>Yes</td>
<td>Minutes + 1</td>
<td>Possibly</td>
<td>Excellent for CW &lt;100°C</td>
<td>Poor</td>
<td>No</td>
<td>1 Day</td>
<td></td>
</tr>
<tr>
<td>IR 1 Mil for .5&quot; Working Distance</td>
<td>Yes</td>
<td>10 µs Standard</td>
<td>&lt;1, Degraded for Pulses</td>
<td>No</td>
<td>Poor</td>
<td>Good</td>
<td>Yes</td>
<td>Several K</td>
</tr>
<tr>
<td>Electrical Resolves Entire Channel (Junction) Region</td>
<td>No</td>
<td>&lt;µs</td>
<td>+2°C</td>
<td>No</td>
<td>Good</td>
<td>If no hot Excellent</td>
<td>Yes</td>
<td>2 weeks</td>
</tr>
</tbody>
</table>

Table 3. Summary of temperature measurement techniques for GaAs devices. (10)
area. Additional effort focused on infrared microscopy might provide improved resolution and is an area that should be considered for funding. However, there appear to be wavelength constraints which will limit resolution to 5-10 μm; these theoretical limits should be studied initially.

Electrical techniques are not very useful with monolithic circuits since the individual FET I-V characteristics are often not readily accessible. The electrical technique utilizes the forward voltage drop of the gate to determine the average channel temperature. Note that the reverse bias voltage, which is normally used with IMPATT diodes to measure junction temperature, is not useful since the reverse breakdown characteristics are generally not sharp with FETs. The technique being set up by Raytheon involves pulsing the gate to forward bias and measuring its I-V characteristic.

An approach which bears investigation is to consider the utilization of thermal models, which would require electrical model inputs, to extrapolate hot spot temperatures from the poorly resolved infrared data. Rather crude thermal models have been used for this purpose by at least one firm interviewed (TRW).

Additional investigations are needed to ascertain whether or not the liquid crystal can be stripped from actual devices without perturbing their characteristics and to evaluate the effects of the coating on RF performance. Such experiments could be performed on discrete FETs and should involve analytical
characterization such as ion microscopy to determine whether or not the liquid crystal material is completely removed and whether or not it diffuses into or reacts with the surface. A research program to move fully develop this techniques appears in order since it is the only alternative with adequate spatial resolution.

Reported experiments on the use of liquid crystals as a failure analysis tool (11)-(12) for location of hot spots/shorts on silicon MOS ICs imply that the liquid crystal and an underlying carbon black film can be completely removed without modifying the devices. Removal is accomplished with pentane, benzene or chloraform in an ultrasonic bath. The desire to operate the GaAs devices and circuits at microwave frequencies with the liquid crystal in place poses a much more severe environment which must be evaluated. The presence of the coating could alter transmission line impedances, dielectric properties, parasitic elements, etc.

Two companies, Liquid Crystal Applications and Pressure Chemical Co., have been identified as sources for these liquid crystals. Cholesteric liquid crystals are available with transition temperatures from -7 to +70°C. However, Raytheon is working with Liquid Crystal Applications to investigate crystals with transition temperatures up to 100°C which will involve less extrapolation to the operating temperature and therefore better accuracy. These studies need to be intensified.
IV.3 Polyimides

In an effort to develop improved processes for GaAs ICs, many researchers are either utilizing or considering polyimide films. This material has characteristics which are very attractive for interlayer dielectrics as well as passivation layers. It characteristics include:

- Ease of application
- Useful for planarization of underlying topographies to improve step coverage
- Low interelectrode capacitance
- Compatible with metal systems
- Alpha particle protection
- Mechanical protection

Polyimides are in use on silicon ICs, and reliability oriented studies of structures containing polyimide films have been reported. However, many questions remain regarding the long term reliability of polyimides in such circuits even though IBM has been using the materials since 1979, and its use has been increasing in the last two years. Dupont recently introduced an ultrapure grade polyimide coating aimed at increasing yields within the semiconductor industry. Ionic chloride levels are less than 5 ppm with potassium, iron and copper levels below 0.5 ppm.

The degree of concern with the use of polyimides depends on how they are being used. In some instances the polyimide is used as a multilevel insulator and is not in direct contact with the GaAs, thus reducing potential problems of interaction with the
semiconductor. In other cases it is used as a protective coating, in which case it is often in direct contact with the GaAs surfaces in the gate-drain and gate-source regions. In this instance, interaction between the polyimide and the GaAs surface is possible in a very critical region of the device. The diffusion of impurities from the polyimide into the GaAs is thus of major concern. Polyimides are hygroscopic and thus absorption of moisture is obviously a potential problem area.

The interest being expressed by industrial firms in the use of polyimides for GaAs ICs suggests a study program to investigate their impact on reliability. Such a program could utilize high power FETs as test vehicles, at least for preliminary studies, and should not involve full scale reliability testing. The objective of this study would be to identify potential problems and define additional investigations if required. Analytical facilities will be required to investigate surface reactions as well as diffusion of impurities into the channel region. The fabrication of special test structures will be desirable in order to investigate surface reactions and the characteristics of the polyimides as capacitor and/or multilevel insulators. The use of adhesion promoters such as pyralin are of concern as is the curing process used with the polyimide.

IV.4 Microwave Probes

The evaluation of functional blocks such as amplifiers, mixers, switches, and phase shifters, when combined on MMIC
chips such as phased array modules, poses a formidable problem. Ideally, direct Rf probing of internal points of the chip at frequencies in the X- and Ka-band ranges would be extremely desirable so as to provide for measurement of the input and output characteristics of each functional block on the chip. Such probing techniques would be extremely useful during development as well as for reliability/failure analysis studies.

RF probe development efforts have increased during the past three years as firms have begun to consider production of GaAs ICs and the need for automated on-wafer microwave measurements. Firms such as Tektronix and Hewlett Packard have made significant progress in this area and several other firms interviewed have development efforts either in progress or planned. However, these probes are all oriented towards probing of the chip bond pads with a standard 50 ohm impedance, and in some instances special chip layouts are required such as a ground contact pad adjacent to the bond pad. As presently designed, the probes are not appropriate for contacting individual points within an IC.

Several firms, including Avantek and Hughes, are planning to utilize 10 MHz probes for on-wafer probing of GaAs integrated circuits. This frequency can be handled with existing probes. The measurement of $S_{21}$ and $S_{12}$ at 10 MHz should be useful, but $S_{11}$ and $S_{22}$ will not. Both of these firms do not feel that microwave probing will be required, but they do agree that internal chip probe pads for 10 MHz probing may be desirable or even necessary. Raytheon mentioned that they strive to make FET
terminals in their MMICs accessible for DC probing, thus avoiding difficulties in layer stripping when performing failure analysis. This is a very useful approach, but it can complicate the chip design and fabrication.

The most sophisticated and mature microwave wafer probing equipment was introduced in 1983 by a new company "Cascade Microwave" which is owned and operated by two Tektronix engineers. These engineers developed the probes, at least partially, under contract to AFWAL while at Tektronix. Their system uses coplanar transmission line probes to bring 50 ohm lines directly to bond pads on the wafer. Interfacing of these probes with an automated network analyzer allows s-parameter measurements referenced to the bond pads at frequencies up to 18 GHz. The probe station and probe cards available from Cascade Microwave provide a complete system for fast, precise and economical on-wafer s-parameter microwave measurements.

These microwave probes are potentially compatible with internal chip probing if the chip layout is such that the probe can make contact and if the probe impedance is correct. In general, this is not likely to be the case. The chip layout will require special design for internal probing to provide probe pads at desired points. The small transmission lines will probably not be of adequate size to allow for contacting and lines may be buried within the circuit. Furthermore, the probes can be expected to severely load the circuit unless some type of high impedance probe is designed. Thus, in order to utilize these
microwave probes, special chip designs and layouts will be required, increasing complexity and sacrificing real estate. Microwave couplers may be necessary to avoid loading the circuit. This technique is therefore compatible only with special chips.

An alternate approach to consider is the use of close proximity coupling probes which might be precisely positioned above the chip to sample the transmission line fields. This technique would provide a relative indication of the signal amplitude and phase which could be used for chip to chip comparisons. The problems with such a system are numerous and include reproducibility of mechanical positioning, weak signal levels with the less than 20-30 dB coupling, and interference from other parts of the circuit due to the high density.

Internal microwave probing of GaAs digital circuits is considerably easier since only discrete signal levels must be considered and probe loading effects are not as critical. Tektronix has in fact used their microwave probes with digital circuits in this manner with the circuit designed using high value on chip resistors and probe pads to sample specific circuit points.

The utilization of internal chip microwave probing for reliability testing does not therefore appear practical since special circuits would be required. A more logical application of this technique is during chip development when special test circuits could be fabricated. However, the manufacturers do not appear interested in this approach. The typical development
approach currently being utilized is to develop each functional block individually, thoroughly characterize each block, perform an overall computer simulation of the complete circuit using measured data on the individual blocks, and then integrate on a single chip. Often the fully integrated chip is fabricated on the same wafer with the individual fundamental blocks to allow for process evaluation.

Without the ability to RF probe the functional blocks within an integrated circuit, reliability studies involving the individual blocks become extremely difficult. Such studies blocks are critical for fault isolation and failure analysis. DC measurements are useful but must be supplemented with RF characteristics. The presence of other functional blocks in the integrated circuit will likely prohibit external measurement of individual block drift with time and stress. In restricted instances, it may be possible to use a combination of external measurements and circuit modeling to make educated guesses regarding block performance, but likely not with the desired precision (< 0.5 dB gain variation for an amplifier).

If reliability studies of GaAs ICs require examination of functional blocks on the chip, the only practical procedure appears to be the fabrication of special test chips. These test chips could take either of two approaches: (1) functional blocks without interconnects could be pinned out either on a common or individual chips or (2) critical points within the circuit could be pinned out by using special couplers to sample a portion of
the signal (-20 or -30 dB) without creating loading effects. The use of couplers for sampling critical points which can then be pinned out is feasible but requires considerable area. Also, the reliability of the couplers becomes a factor, some loading can be expected, and the coupling will be temperature sensitive.

Note that the idea of partitioning the chip such that the individual components can be separated by scribing or sawing is usually not desirable for production devices due to the major area increase required for complex chips (it might be useful for simple chips with two or three blocks). The idea of special test chips properly partitioned for separation is feasible, but it is probably easier to simply put each functional block on a separate chip on a common mask which also contains the complete IC. This is the technique currently being used by most researchers. Rockwell for example places each stage of a three stage amplifier as well as each combination of interconnected stages on a single mask during development. This approach provides an excellent vehicle for troubleshooting circuit problems as well as providing excellent test circuits for reliability studies. Complete parameter characterization of these individual components provides the data needed to study interconnect problems via the computer. Utilization of this approach will probably be reduced once confidence is established in circuit design procedures.

In summary, the presence of multiple functional blocks in complex GaAs integrated circuits will in general preclude allocation of circuit parameter changes to specific blocks during
reliability testing. Phase drift in a switched line phase shifter for example will be indistinguishable from changes in the transmission phase of an amplifier connected in cascade with the phase shifter if only external measurements are considered.

As discussed previously, the use of special microwave probes for internal probing of the chip does not appear practical due to loading effects, inaccessibility of desired probe points, positioning accuracy, real estate required for building in probe buffering circuits, and coupling from close proximity lines.

IV.5 Special Test Chips and Patterns

The most practical means of performing reliability studies on these circuits appears to be the use of special test chips fabricated on the same wafer as the production devices. Each functional block and critical combination would be fabricated on individual chips dispersed across the wafer. These special chips could then be utilized for failure analysis studies if the complete integrated circuit experienced problems during reliability testing. Note that such special chips would likely also be needed during circuit development.

Failure analysis of these circuits may also necessitate the fabrication of special test structures such as ohmic contact test patterns. Such test patterns are routinely used for process control by all firms interviewed. These test patterns, which are fabricated on all wafers, could be extremely useful for detailed failure analysis.

Reliability studies involving these special chips containing
individual functional blocks as well as test patterns should be directly applicable to reliability of the complete integrated circuit provided they are all contained on a common mask and fabricated on the same wafer. These special circuits should utilize the standard design rules. General Electric is planning to use these test patterns as a part of their early reliability testing to help identify problem areas.

A suggestion worthy of serious consideration is to design a standard test pattern useful for reliability studies and have this pattern included on all wafers processed on DoD sponsored programs. Some modifications would be required for each firm's specific process, but the basic test structures would be standard and would allow a comparison of the various processes being used. Specific test structures might include ohmic contacts, gates, discrete FETs, mesa isolation, backgating, etc.

IV.6 Non-contacting Probes

Non-contacting probe techniques such as SEM voltage contrast, EBIC and laser probing should be useful with GaAs integrated circuits just as for Si devices. Relatively little work of this type has been reported with GaAs circuits since reliability studies have been very limited. However, SEM voltage contrast has been used very successfully at Georgia Tech on GaAs IMPATT diodes to study movement of the depletion region during reverse bias. By observing the side of the mesa, the voltage contrast mode of the SEM reveals movement of the depletion region for low-high-low double-drift structures. Prior to utilization of
the SEM, the impact of the electron beam should be evaluated. No effects have been observed at Georgia Tech with GaAs discrete devices such as FETs, millimeter wave mixer diodes, and IMPATT diodes. SEM is used by Hughes to examine the final assembly of space qualified millimeter wave mixer diodes and no effects of the electron beam have been detected.

The use of laser probing should prove extremely useful in failure analysis of GaAs ICs. Introduction of carriers optically with the laser provides a high resolution scanning process for examining the circuit for defects. Research is required however to fully develop this technique and show applicability to GaAs ICs.

IV.7 Radiation Effects

GaAs discrete devices and integrated circuits have been suggested to have improved radiation resistance over Si. Reported measurements indicate that this is indeed the case and suggest interest for military applications. However, most of the data are rather preliminary, and continued research is required to quantify the improvement and identify optimum device configurations. Firms such as McDonnell Douglas and Raytheon are currently performing some such studies, but DoD funding is needed in the near future for thorough evaluation of specific GaAs ICs.

Reported data on GaAs ICs indicate a superiority over Si in terms of total dose susceptibility. Table 4, extracted from a report by NRL, summarizes reported radiation hardness levels of GaAs devices.\(^{(14)}\) An area of concern for GaAs is the radiation
<table>
<thead>
<tr>
<th>TYPE OF RADIATION</th>
<th>D MODE FET</th>
<th>E MODE FET</th>
<th>E MODE JFET</th>
<th>SB DIODE</th>
<th>PIN DIODE</th>
<th>ANALOG IC</th>
<th>DIGITAL IC</th>
<th>GUNN DIODE</th>
<th>CCD</th>
<th>IMPATT</th>
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</thead>
<tbody>
<tr>
<td>ELECTRONS, TD X-RAYS</td>
<td>$10^6$</td>
<td>$10^6$</td>
<td>$10^7$</td>
<td>$10^7$</td>
<td>$2 \times 10^7$</td>
<td>$10^7$</td>
<td>$2 \times 10^7$</td>
<td>$10^8$</td>
<td>$10^8$</td>
<td>$5 \times 10^9$</td>
</tr>
<tr>
<td>Y-RAYS</td>
<td>$2 \times 10^{10}$</td>
<td>$2 \times 10^{10}$</td>
<td>$5 \times 10^{10}$</td>
<td>$2 \times 10^{10}$</td>
<td>$10^8$</td>
<td>$5 \times 10^9$</td>
<td>$10^8$</td>
<td>$10^8$</td>
<td>$5 \times 10^9$</td>
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<tr>
<td>PROTONS TD</td>
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<tr>
<td>NEUTRONS TF</td>
<td>$5 \times 10^{13}$</td>
<td>$1 \times 10^{15}$</td>
<td>$2 \times 10^{15}$</td>
<td>$2 \times 10^{14}, 10^{15}$</td>
<td>$10^{12}$</td>
<td>$10^{12}$</td>
<td>$2 \times 10^{12}$</td>
<td></td>
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<td></td>
</tr>
<tr>
<td>BURST</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$10^{18}/cm^2$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\alpha$, HEAVY IONS, COSMIC RAYS (SINGLE EVENT)</td>
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</table>

TD - TOTAL DOSE (rad)
$\dot{i}$ - DOSE RATE (rad/s)
TF - TOTAL FLUENCE (cm$^{-2}$)

Table 4. Radiation Hardness Levels of GaAs Devices. (14)
transient effect which appears to be the major radiation problem with GaAs devices. The use of undoped substrates and a buried p-layer are helpful in reducing the transient response. Research is required to thoroughly evaluate this problem and determine the optimum solution.

Researchers at Raytheon expressed concern about the effects of radiation on passive devices, including transmission lines. Substrate conversion and effects on dielectrics are also potential problem areas that should be investigated.

IV.8 Survey of Industrial Firms

In order to determine the status of GaAs IC reliability and to obtain guidance as to the direction of such efforts, visits were made to eight industrial firms and several others were interviewed by phone. Trip Reports for these visits are attached as an Appendix. All firms were very open with respect to their present activities and future plans in this area. In some instances they disagreed as to recommendations for future study.

Generally, the firms interviewed had done little or nothing in the area of reliability testing of GaAs ICs. However, almost all had plans for initiating or increasing their involvement in such testing in the coming year. Several, such as General Electric and Raytheon, are planning major reliability efforts in 1984. All firms are involved in some form of reliability testing of GaAs FETs and are using this experience as a base for their GaAs IC studies.

All firms were questioned as to whether or not the timing is
appropriate for GaAs IC reliability studies and if so what type of investigations are needed. There was unanimous agreement that the pace of the technology development, the impending introduction of several MMICs on the commercial market, and the lack of reliability data dictate that DoD begin funding such studies in the near future. There was however some disagreement as to what type of studies should be funded. Avantek felt that full-scale reliability studies involving several hundred integrated circuits are appropriate based on the fact that their process is established and ready for production. The other firms disagreed and felt that rather limited studies involving 10-30 integrated circuits are needed to identify problem areas requiring additional study and to give guidance to IC technology development. Their argument was that the processing technology remains in a very transient period, and full-scale reliability tests would yield technology data which would be quickly outdated. The relatively low level of testing they proposed would search for fundamental mechanisms and give guidance to technology development.

Considering the present status of this technology, the small-scale tests appear more appropriate and should be initiated as quickly as possible. The test vehicles chosen should be relatively simple circuits so as to allow failure analysis. However, the circuits should include most of the components of interest: resistors, capacitors, inductors, FETs, and diodes. If possible, all important nodes should be accessible for fault
isolation. Inclusion of wafer test patterns in these tests could also be extremely helpful. The tests should include dc, RF and thermal stress. An obvious choice for test vehicles are medium power, two or three stage, GaAs FET, monolithic amplifiers. Several firms are developing such amplifiers and it should be possible to procure circuits fabricated with several different processes.

Establishing test facilities for these amplifiers represents a major problem due to the requirement for RF stress, the relatively high temperatures involved, and the precision required for the RF measurements. Since these test facilities don't exist within DoD or an independent laboratory, an effort should be made to have the tests conducted by an industrial firm such as Hughes Space and Communications Division or Bell Laboratories which already has test facilities for hybrid FET amplifiers. Failure analysis of the devices could be performed by the firm conducting the tests, by the vendor supplying the circuits or by an independent laboratory. Determination of the failure mechanisms is critical since these tests will give guidance to the technology development.

Determination of screening procedures and failure criteria for these life tests is also essential and is an area recommended for study by several of the firms. Current screening techniques for FETs consist of applying voltages and currents in excess of the normal operating point. Failure criteria for FET reliability tests have been primarily based on changes in gain of 0.5 - 1.0
dB for devices operated as amplifiers. These procedures must be carefully reviewed and criteria established for the amplifiers to be tested. Careful thought must be given to which of the numerous dc and RF parameters to monitor during reliability testing. Maintaining proper bias at elevated temperatures poses a difficulty which must be considered since bias to the FETs are not controllable independently.

There was considerable disagreement regarding the need for farther study of gates, ohmic contacts and passive elements. Several firms maintained that these areas had been studied extensively in the past and that there were no major problems. They maintained that problems such as capacitor failures reported by some firms were simply due to their inability to properly deposit the oxide or nitride dielectric. Others felt that programs were needed to concentrate on these facets. The small-scale reliability studies recommended above should provide answers to these questions, and consequently, it is recommended that these specific studies be delayed until the reliability tests reveal the failure mechanisms.

There was also disagreement with respect to utilization of RF probes for internal chip probing for nondestructive fault isolation. Most of the firms stated that this technique was probably not practical, and the nodes of interest were likely to be inaccessible unless special designs were implemented. There was, however, agreement that on-wafer RF probing of bond pads was needed, and several firms are working on this problem.
Funding by DoD in the area of RF probe development does not therefore seem necessary at this time.

The need for built in diagnostics was suggested, but the increased chip area required is a major deterrent for production circuits. No one indicated plans to use this technique for either circuit development or fault isolation. The use of wafer test patterns was however much more enthusiastically received. All firms make rather extensive use of such patterns. The generation of standard wafer test patterns to be utilized by all vendors was well received. If properly designed, these test patterns could be very useful in reliability studies and might be included as deliverables on DoD sponsored programs.

Other suggestions for study included the following:

- **Isolation implants** - when epitaxial films are employed for GaAs ICs, implants of boron or oxygen are used to provide isolation between devices. The thermal stability of these implants was questioned. Very few firms are using epitaxial films for such circuits and this does not appear to be a high priority item for funding.

- **Passivation coatings** - Several firms are searching for a good passivation coating for GaAs ICs. Nitrides, oxides and polyimides are all being used. This is an area that appears worthy of investigations, but limited data should be available from the small-scale reliability studies recommended above.
Substrates - Studies were recommended by Hughes to relate RF performance to material properties such as defects, traps, photoconductivity, photoluminescence, residual impurities, mobility, etc. A possible failure mechanism for GaAs FETs, discussed in Section III.1, involves out-diffusion of impurities from the substrate into the channel region. This study is worthy of serious consideration for funding, but it can be performed with discrete FETs rather than MMICs.

Thermal Expansion - General Electric observed that thermal expansion could be a problem with large GaAs IC chips. GaAs is rather brittle and might indeed be subject to such problems. X-ray techniques could be used to characterize various size samples of GaAs subject to thermal cycling. This is a rather straightforward study which could be useful.

Radiation Effects - Additional studies of radiation effects on MMICs were suggested. Such studies are obviously needed for some military applications and should be funded in the near future to give guidance to technology development.

Packages - As GaAs ICs go into production, new packages will be required, especially for the larger, more complex chips. This need was mentioned by several firms. Some packages are available and others are being developed by the firms beginning production of GaAs.
ICs. At the present time, this need appears to be receiving adequate attention and does not justify funding by DoD.
V. CONCLUSIONS AND RECOMMENDATIONS

A thorough review of the literature and interviews with many of the firms involved in GaAs IC technology has supported the view that virtually no reliability data are available for GaAs ICs. Furthermore, no such studies have been identified in progress even though several firms are planning relatively small in-house studies in 1984. Based on reliability studies of power and low noise GaAs discrete FETs which have demonstrated acceptable performance, there appear to be no fundamental reasons why GaAs ICs should not have adequate reliability for military applications. However, this technology remains primarily in the research and development laboratory with several commercial firms only recently beginning to announce commercial products. Consequently, the processing technology remains in a transient state, creating difficulties in evaluating the reliability of various facets of the technology such as ohmic contacts, gates, capacitors, etc. Furthermore, yields are low and major efforts are necessary to develop processes with adequate yields for production.

Based on the state-of-the-art, the rapid growth anticipated, and recommendations from industrial firms, the timing is appropriate to initiate small lot qualification studies involving step stress testing of 10-30 devices. The objective of these studies is to identify problem areas and to give guidance to IC technology development. These studies should be initiated as
rapidly as possible and involve relatively simple circuits as discussed in Section IV.8. RF bias should be included.

A major question posed by the Statement-of-work is the methodology for studying reliability of MMICs and in particular procedures for fault isolation. These areas are discussed in Section IV. The basic conclusions are:

- Microwave probes are available for probing the bond pads but are not useful for internal chip probing due to the loading effects and probe pads required. The special chip designs required for internal probes negate their usefulness. (Section IV.4).

- The use of standardized wafer test patterns to be used by all DoD vendors is recommended. These patterns could be used to supplement reliability/failure analysis studies and would provide a common denominator for comparison of vendors. (Section IV.5).

- Characterization of functional blocks in ICs is best accomplished by either chip layouts which allow for sawing or scribing to isolate blocks or by placing blocks on individual chips as is often done during development stages. (Section IV.5).

- Noncontacting probes such as laser or electron beams should be useful for fault isolation but will not
provide quantitative information. (Section IV.6).

Reliability studies involving RF bias will be much more complex with high frequency GaAs ICs than with conventional Si devices. Both the generation of appropriate driving signals and the accurate phase and amplitude measurements will involve considerable investment in equipment. The use of an automated network analyzer will be extremely desirable to achieve the repeatability and accuracy required. As a result of the complexity of these measurements, very careful planning will be necessary, particularly when hundreds of devices are involved. (Sections IV.1 and III.2)

Other facets of this technology recommended for study are as follows:

- **Polyimides** - This material is being used for interlayer dielectric as well as passivation layers with little or no reliability data (Section IV.3)

- **Channel Temperature Measurements** - Accurate measurement of channel temperatures with 0.5 - 2 μm resolution are necessary for reliability studies on power MMICs. Liquid crystals are the only available technique with this resolution but little is known of their effect on the circuit. Infrared microscopy should be capable of resolution somewhat better than the available 10-20 μm and research in this area could be useful (Section
Radiation effects - Relatively limited data are available on radiation effects on GaAs ICs. Transient effects and effects on passive elements are particularly of interest. (Section IV.7).

Screening Procedures - Current screening procedures consist primarily of applying voltages and currents in excess of the normal operating point. Better procedures are needed before entering full-scale reliability testing. (Section IV.8).

Failure Criteria - The failure criteria used with most FET reliability studies involve changes in RF gain of 0.5 - 10 dB. With complex GaAs ICs, definition of parameters to be monitored during testing is critical due to the complexity of the measurements. (Section IV.8)

Gates and ohmic contacts - Several firms continue to experience problems with FET gates and ohmic contacts. The recommended small-scale reliability studies should provide an indication of the severity of this problem. The development of a replacement for the Au-Ge-Ni ohmic contact should be considered. (Section IV.8)
REFERENCES


APPENDIX
1. RF probes for on-wafer bond pad probing are being developed by Ken Facet. They utilize double clad dielectric and are matched to 50 ohms as close as possible to the wire tip used for contacting. They have no plans for internal chip RF probing and are not optimistic. E-beam probes have been used up to 1 MHz, but these are not useful at microwave frequencies. They have tried resistive dividers for sampling but commented there are problems due to the small signal level and the fact that impedance levels may be high at the desired probe points. The probes they are designing will have 20 pairs of probes in the probe card pattern and are somewhat similar to those reported by Tektronix. George feels that coupling probes from above would have severe mechanical problems.

2. He feels the technology is now adequately advanced to begin reliability testing on a small scale. TRW has not yet tested any of their MMICs for reliability, but they are reorganizing and are considering a new group to look at such reliability problems. They have not had any funding to investigate reliability of these circuits and feel that such programs should be funded. In particular, George recommended a small lot qualification study involving step stress testing of 10-30 devices to derive preliminary data. A large reliability effort is inappropriate at this time since no one is fabricating large numbers of devices for such a study. These preliminary studies should emphasize tests at various temperatures, RF levels, and dc biases to demonstrate problem areas. The use of a high resolution IR
scanner for temperature probing is essential in these studies.

3. The TRW modeling capability is close to allowing full chip design with multiple components without having to build the individual components initially. Their computer designs are working well. However, George is very negative about inferring what is happening within the circuit from the terminal characteristics.

4. In response to a question regarding how useful discrete FET testing is to MMIC reliability studies, he pointed out that the MMIC may require major changes in the processing and may introduce new problems. He feels that gates, ohmic contacts, and capacitor dielectrics all require additional study. He noted that monolithic circuits have an advantage in that there is better control of the environment since the devices and components are close together and thus more uniform with less parasitics between.

5. The difficult reliability problems will obviously lie in the area of power circuits such as phased array modules.
1. TRW is involved in reliability testing of both low noise and power discrete GaAs FETs as well as in failure analysis of these devices. The devices are purchased from outside vendors. Most of the effort has centered on 1 watt, 1 micron, MSC, flip chip mounted FETs. They have performed extensive accelerated life testing with RF using four temperatures and have determined activation energies. They don't have data to prove that RF is required for realistic testing, but they feel strongly that it is, except perhaps for small signal devices. They have built test racks and established test capability for life testing approximately 24-30 devices simultaneous at elevated temperatures under dc and RF bias. They also have developed screening techniques and test procedures.

2. They tested 22 one watt hybrid amplifiers at 200-275°C channel hot spot temperature. An IR high resolution (10 micron) scan was taken to determine the maximum temperature. This IR scan was then used with thermal modeling to determine the hot spot temperature. The criteria for failure was 1 dB drop in gain.

The procedure involves initial dc characterization followed by a stabilization burn-in at 200°C channel hot spot temperature for 168 hours. This is followed by 250°C channel hot spot temperature for over 1000 hours under dc and RF bias. Instant failures are eliminated with a high voltage dc screen at twice the operating temperature.
3. They feel it is appropriate to begin to qualify the IC process using test vehicles for reliability studies. Quantities of 10-20 devices should give useful data and help to identify problems. The forward Schottky characteristics and reverse leakage are important to study as functions of temperature. The importance of the IR scan to determine the spatial temperature profile should be emphasized. They emphasized that the reliability testing should not advance too rapidly since the technology remains in the R&D stage. Relatively simple initial testing is now appropriate, and such tests may only be appropriate for the vendor to perform.

4. MMICs have unique characteristics in comparison with discrete devices due to multiple metal paths, air bridges, vias, thermal coupling, and passive components as well as in some instances different processing. Fault isolation is a major problem and dc probing may be the only procedure available. Even if RF probes are available, desired test points may not be accessible due to overlay metals and dielectrics. Therefore, failure analysis may be limited to the vendor.

5. Passive components are much more reliable than the active devices, but dielectrics do get leaky and resistor values change. These components should not be neglected.
1. Rahul thinks that RF probes for internal chip characterization are feasible. Resistive voltage dividers could be a problem for analog circuits, but they feel external probes may be superior. They have a strong interest in on-wafer RF probing due to the cost of packaging and testing chips. Other firms such as Tektronix and Rucker and Kollas are developing RF probes. A suggestion was made that "process diagnostics" be considered where test patterns are placed on the wafer in key processing steps, evaluated to characterize the processing to that point, and then removed prior to additional processing.

2. TRW has not been involved in high power circuits but they are beginning to look at reliability of low power circuits. They emphasized the importance of process related modeling to help in understanding physics of failure. If failure analysis is to be performed, the circuit should be broken into submodules. The failure analysis is most easily performed by the manufacturer. Rahul suggested a "dynamic burn in system" for MMICs; for example, ring oscillators could be built on the same chips with amplifiers and used to drive these amplifiers for reliability testing.

3. They feel that ohmic contacts are in need of additional study.
SUMMARY

The consensus of opinion at TRW is that the timing is appropriate to begin preliminary reliability testing of MMICs. Full scale testing is inappropriate at this time since there are not yet appropriate circuits in production which are available in sufficient quantities to be utilized in such tests. However, preliminary tests on quantities of circuits ranging from 10 to 30 would provide excellent guidance.
Hughes Malibu Research Center
Bob Lee, Dave Matthews and Chuck Krumm
8/2/83

1. In response to the question of whether or not discrete FET reliability efforts will have a major impact on MMIC reliability studies, they pointed out that the processing for MMICs will likely be somewhat different. For example, most discrete devices are utilizing epitaxial material with high resistivity buffer layers, while MMICs generally are employing ion implantation in semi-insulating substrates. In addition, the air bridges, vias and passive components can have a significant impact on reliability even though they should be much more reliable than the active devices. Problems such as oxide or nitride pinholes in MIM capacitors or poor metalization processes can rapidly degrade reliability for the passive devices. Unstable metalizations can be a major problem. Proton, boron or oxygen implants are used by some firms for isolation between devices when epitaxial layers are employed for MMICs. The reliability of this process does not appear to have been adequately evaluated. Boron and oxygen implants are thought to be stable up to 700-900°C while the proton implant is questionable at 400°C.

2. Their feeling is that full scale reliability tests of MMICs are premature, and they strongly advise against such tests due to the fact that the technology remains in an R&D mode for the most part. However, they strongly recommend that moderate reliability tests are needed now to "shake out the technology problems." They pointed out that reliability efforts must involve testing with both RF and dc at full power and consequently such efforts are extremely expensive,
particularly when multiple RF inputs and outputs are involved. The idea of using chip samples in quantities of 10 to 30 from other module development programs was appealing for these preliminary reliability testing efforts. There is a strong need to perform studies of this type in the near future.

3. Establishing appropriate test procedures for these chips is not a trivial problem. Many of these devices will have very subtle changes in dc and RF characteristics when under test. Furthermore, relating dc characteristics to RF performance is typically extremely difficult. RF characterization will normally require sophisticated test equipment such as automatic network analyzers in order to obtain the desired phase and amplitude accuracy and repeatability. The suggestion was made that programs should be funded to establish criteria for determining failures and to determine what parameters must be measured. For example, they pointed out that generally it is not possible to adequately define component specifications to ensure that they will function in systems. Determining what is actually a fault can be a major problem.

4. Fault isolation is extremely difficult in MMICs in both development and reliability testing. The only approach they utilize for fault isolation is dc probing which is not very satisfactory since they can't necessarily relate dc characteristics to RF performance. When a problem occurs in a component such as a multistage amplifier, their only approaches to identifying the problem are modeling using Compact and dc probing. They rely heavily on test patterns which are dispersed around the wafer. For example, a free running oscillator is an excellent test vehicle since the frequency is very sensitive to parasitics, and the frequency
is easily measured with probe coupling, thus avoiding the requirement for RF contacts. Each chip might have a few test structures included as is sometimes done on silicon ICs.

Functional blocks are developed separately prior to integration and thus are well characterized before designing the complete module. Modeling is emphasized and sensitivity analyses are performed using the Compact program.

Hughes Malibu is not presently using internal chip RF probing, but they are developing probes for bond pads to allow on-wafer RF probing. They point out that microwave RF probes are extremely difficult, particularly at X-band and above. Note that internal RF probing may not be feasible in many instances due to the multiple interconnect levels and the fact that many circuit nodes may not be accessible due to overlays.

The idea of resistive voltage dividers to allow coupling from various circuit nodes is certainly feasible and has been used in digital GaAs circuits. However, real estate is sacrificed and the chip design must account for the parasitics resulting from these structures. The test structures could be eliminated with a laser. Also might consider the use of FET switches to isolate the probes from the actual circuit. These built-in diagnostic techniques could be very useful, but their reliability must also be considered.

5. They suggested that the time is appropriate to fund study programs related to reliability of these MMICs. In particular, they suggested study programs to look at RF probe development, test procedures, and built-in diagnostics. Such studies are far more important at this
time than major reliability evaluations on chips which have not yet gone into production. Studies on specific technology aspects such as ohmic contacts or Schottky barriers are not needed since they are being worked on discrete device studies.

6. Malibu is not working on power devices which are likely to have the major reliability problems. This work is being performed by Hughes Torrance.

7. Based on the very limited reliability testing being performed, they feel the GaAs MMIC process to be reliable with no inherent problems which can't be overcome.
1. Rockwell is developing for NASA a 20 GHz MMIC which includes a phase shifter, driver amplifier and power amplifier. The components have been developed and total integration is in progress. The program requires delivery of 200 modules. There are no reliability tasks on any of their MMIC programs. This is their first MMIC module with multiple components. The circuit being developed for NASA might provide a test vehicle for a reliability study, thus avoiding the development costs and perhaps the fabrication costs if an adequate quantity could be provided by NASA. Since Rockwell does not have reliability test setups, other firms could be used for the testing. Collins (owned by Rockwell) might have this test capability.

2. They feel that 50-100 devices are needed with dc and RF bias for a reliability study to think the timing is appropriate. Their feeling is that gates, ohmic contacts, etc. have been studied for discrete devices and don't need additional study. Passive devices are not a major problem. These preliminary reliability studies are needed to identify problem areas needing further study.

3. Their standard process is ion implantation into undoped substrates with Ti-Pt-Au Schottky gates. Polyimides are used for dielectric isolation and for protection on top of FETs. They do not know what the long term effects of the polyimides might be. This coating does not effect any of the S-parameters except $S_{12}$, as expected, and it does not appear to decrease the power or gain. The polyimide is cured at
250°C and is reported to have no additional outgassing. Note that it does shrink somewhat which could cause stress, but it is rather flexible. If required, silicon nitride could be used in place of the polyimide.

4. Rockwell presently does no RF probing, but they are beginning to develop such a probe for digital GaAs ICs. The RF probe is low priority for analog applications. In many instances it is impossible to isolate devices for probing. They sometimes cut circuit paths or scribe chip to isolate parts of the circuit for test. Their usual approach is to fabricate test structures on the wafer as well as including individual parts of the circuit as separate chips. For example, on a three stage amplifier they would include discrete devices and individual stages as well as all combinations of the stages on separate chips to allow full characterization using an automatic network analyzer. Each component in their circuit has 50 ohm inputs and outputs and each stage is biased separately to aid in characterization. If the circuit doesn't function as desired, computer models are used to conjunction with the measured data to determine the problem and redesign the circuit. They point out that this approach has been very successful.

The accuracy of their model is reported to be good. This model is based on empirical FET data. These models are not absolute, but they indicate well the trends. They would like to have a process related model but pointed out that such a model does not exist for the FET. This is an area that requires much work.

5. No work is being done with packages or thermal analysis of circuits.
6. Experience with ultrasonic wire bonders indicates the damage can occur to FETs with their use. At low powers, successful bonds have been made without obvious damage, but the more subtle effects are not known.
1. Bernie has performed the most extensive FET reliability testing that I have seen. He is buying in quantities the best low noise FETs available from NEC, Fujitsu and Avantek and performing life tests to identify the most reliable devices available for satellite applications. This effort also involves failure analysis and interfacing with the vendors to attempt to correct failure modes. He has spent considerable time in Japan with these vendors and is aware of major efforts in Japan for production of MMICs. Harris, NEC and Avantek will have MMICs on the market in the near future, and these could be purchased for reliability testing. These circuits will be rather simple and thus appropriate test vehicles for preliminary reliability testing.

2. Avantek and NEC are using silicon nitride coatings on FETs to make the devices more stable. Bell Labs says that this nitride must be deposited in a hydrogen environment. This could be an area for investigation.

3. He thinks that the lack of RF probes may not be a major drawback. Extensive dc probing, coupled with capacitance measurements at 1 MHz, should provide a good indication of Rf performance. He is presently assembling such a system using a Hewlett Packard semiconductor parameter analyzer, a capacitance meter and a computer interfaced with a wafer prober which has probes useful up to 10 MHz for the capacitance meter. Andy Anderson at Avantek is also working on an automated dc wafer prober.
4. Isolation of faults and failure analysis are major problems and may be very limited for MMICs. He has not been very successful in this area. Dissection of the circuits will likely introduce more problems than it solves. Extensive wafer test patterns are being used to assist in the analysis.

5. He has done preliminary reliability tests on flip flops, NOR gates and NAND gates fabricated by two vendors. Early circuits with Cr-Au metalization deteriorated rapidly, while Ti-W-Au gates showed no deterioration at 175°C. They are redesigning the test fixtures for 250°C so as to allow a more significant test. The devices are exercised at MHz rates during these thermal soak test. One vendor used SiO₂ layers for isolation, and some cracks were observed after the tests. Other devices with air bridges experienced no failures.

He has seen electromigration on FETs from two vendors when subjected to thermal soak at 250°C. Also, he has observed cracks in some chips which occur after 1000 hours and do not follow the crystal planes. Developing screening tests for such devices is difficult but needs to be considered for MMICs.

6. He has not investigated reliability of passive components, but he feels they are not a major problem. He has observed problems with MIM capacitors.

The use of 16 mil thick substrates is being investigated to reduce microstrip line losses (i.e. line widths are increased). These thick substrates will require laser drilled holes for vias since normal chemical or reactive ion
etching (RIE) procedures do not work for this depth. This laser drilling technique is worthy of investigation.

7. Liquid crystal have been used with some FETs to provide indications of the temperatures. The crystals are dissolved in acetone, dropped on the devices and allowed to dry. They change color rapidly when their critical temperature is exceeded. This technique could be useful for determination of peak temperatures of MMICs. Excellent spatial resolution has been observed.
1. They are conducting numerous programs for DOD and NASA dealing with the development of GaAs MMICs in the 5-110 GHz frequency range. Among these programs are the following:

- 64 element subarray for the Army - 10 W T/R module including power and low noise GaAs monolithic x-band amplifiers
- 30 GHz MMIC receiver for NASA Lewis - includes a front end low noise amplifier
- 70-110 GHz GaAs MMIC receiver for NRL - uses a mixer front end with a fundamental frequency FET LO
- 8-26 GHz traveling wave, monolithic GaAs amplifier
- 2-30 GHz traveling wave, 1 watt, GaAs, MMIC amplifier

2. The major firms involved in analog GaAs MMIC development are Raytheon, TI, Hughes, and Westinghouse in this order.

3. None of their programs involve reliability efforts except for the NASA program which encourages attention to reliability but requires no specific technical tasks. These are all R&D tasks and as such are not yet concerned with reliability testing. Hughes Torrance has been life testing discrete FETs, both power and low noise. They have assembled test sets for simultaneous thermal soaking of over 100 devices with applied dc bias. Some of these test fixtures have been modified for RF bias as well.

4. They have been investigating protection of both the discrete devices and MMICs using silicon dioxide, silicon nitride and
Humiseal. The oxide and nitride are applied with a light enhanced low temperature CVD process. These coatings have been subjected to rather vigorous testing involving thermal cycling between -55 and 125°C, thermal soaks and high humidity. The Hummiseal is applied on top of either the oxide or nitride. They have seen no failures which could be attributed to the humidity or temperature cycling. The hummiseal does not appear to introduce RF loss. There is as expected a slight frequency shift, but the power handling capability appears for some odd reason to increase. The time periods in these tests are short and the temperatures are low; the results are therefore preliminary. These circuits have also been subjected to radiation testing at NRL. Doug agreed to provide summaries of all these tests when they are documented in their contract annual report. I asked about the use of the polyimides for either processing or circuit coating, but they have not used these materials. They pointed out that Plessey is using polyimides extensively in MMICs which are in production in England for military applications. The passive elements are placed on top of polyimides. Obviously, this suggests that the polyimides have been subjected to rather extensive reliability testing.

5. Doug and Melton had differing opinions on what type of reliability studies are appropriate. Doug suggested that MMICs might be purchased from several vendors, all subjected to reliability testing by one firm, and then returned to the appropriate firms for fault isolation and failure analysis. Melton felt that each firm should test its own devices.

They felt that 100 chips are needed to derive useful reliability information; they don't think 25 chips are adequate. This implies that such a test would require major funding to fabricate chips in this quantity and require a
major failure analysis effort. Their suggestion is that these life tests should be conducted initially to define areas for additional study. Also, the MMICs should be rather simple in order to enable the fault isolation to be performed.

6. Their development approach is to begin with a small portion of the circuit and to gradually increase its complexity with succeeding mask sets. They make use of rather simple wafer test patterns. The circuits are designed, to the extent possible, so as to allow scribing for isolation of parts. Their processing is in their opinion extremely reproducible, especially for small signal devices.

7. With respect to the size of chips, they feel that the large chips being explored by some firms are not feasible due to yield. In the next five years they believe practical MMICs will be rather small with one or two functions such as low noise amplifiers, power amplifiers, mixers, etc. These chips will be combined using hybrid MICs. However, in some applications, size constants may force higher levels of monolithic integration.

8. Hughes Torrance appears very wary of RF probes, particularly at X-band and above, and feels that it is naive to spend so much effort on them. Probing with RF is complicated, particularly with microstrip transmission lines where a via must be used to bring a ground connection to the top side of the substrate. Also, for power circuits the wafer is not well heat sunk while probing. With respect to dc probing, they are developing a computer controlled dc wafer prober. Exhaustive dc testing appears more appropriate to them even though they continue to have problems with correlating dc and RF performance.
9. Melton suggested the need for additional GaAs materials work to relate RF performance to defects, traps, photoconductivity, photoluminescence response, residual impurities, etc.

10. The Hughes Torrance MMIC process is predominately ion implantation in buffer layers. Based on the 60 GHz FET devices they have fabricated, this process is obviously working well.
1. General Electric is involved in only analog circuits at this time. They are in the final stages of completion of a very impressive MMIC facility which is being directed by Jim Hwang. A separate reliability group, of which Don Lacombe is the key technical leader, has begun to look at reliability problems with MMICs in the past year. GE management has apparently been convinced by this group that it is appropriate to begin MMIC reliability studies and they are planning to expand this effort next year using IR & D funds. Most of their module work appears to be internal funding. Don feels that even though the MMIC technology is still in the R & D stage and thus very transient, reliability studies are needed to give guidance to technology development. He has conducted an extensive literature search and the references are primarily for discrete devices.

2. Their present approach is to use "Test Element Groups" (TEGs) which are simply wafer test pattern for looking at discrete parts of the process such as ohmic contacts, schottky barriers, device isolation, electromigration, etc. This effort is internally funded and it relates to discretes as well as ICs. The major effort is using thermal soak in a nitrogen environment, but they are also doing some dc tests. They feel that the primary effect of the RF is thermal, based on their experience with silicon, but don't know with any confidence how important it will be for GaAs ICs. They stated that the literature does indicate differences in dc and RF tests for discrete FETs. The importance of these test patterns should not be overlooked in their opinion; they may
be the best approach for failure analysis. The methodology for failure analysis is a problem they plan to "feel their was through."

3. Their plan for next year is to put more than 100 MMICs on dc life test using whatever chips are available. They pointed out that they don't care whether or not the chips meet RF specs, but obviously they must be uniform. They also want to put approximately 25 devices on RF test and are planning to put together a facility for dc and RF testing of MMICs. The tests they are planning will be devised to obtain general information and not specific process technology data; the latter would likely be quickly outdated.

4. A number of specific problem areas have been identified in their reliability testing. Degradation of Ti-Pt-Au schottky barriers has been observed at 300°C. Ti-Wi-Au schottky barriers have demonstrated adhesion problems. Capacitors are often of large areas and are a major contributor to failure of their circuits. Thermal expansion of large GaAs chips could be a problem as chip sizes approach 0.5 inches; this should be assessed. They noted that BTL has reported active layer degradation possibly due to traps diffusing from the substrate or buffer layer.

5. G.E. has not been concerned with packages for MMICs but are now submitting a proposal that could involve package development. Their IC chips are not being packaged at this time.

6. The G.E. MMIC process does not involved polyimides. Don noted that polyimides are porous and conduct water. Oxides or nitrides on top could be used to protect the polyimide. Note that G.E. manufacturers polyimides and therefore has
capability to control impurities, reproducibility, specific characteristics, etc. for these materials as does IBM for polyimides used in their silicon ICs.

7. Radiation hardness is an issue that requires investigation due to DoD's strong involvement in this technology development.

8. Thermal problems also deserve attention. There is a need to fatigue cycle GaAs chips as well as chip-bond interfaces. Thermal modeling is important for MMICs and GE has a 3-D thermal model (ANSYS) which is very useful for this purpose.

9. Don suggested that specially designed TEGs (wafer test patterns) be standardized for DoD sponsored MMIC programs and that these test patterns be required deliverables from the same wafers from which MMICs were processed and delivered. Such test patterns could be used for reliability testing.

10. When searching for fundamental mechanisms, quantities of ten chips should be adequate for reliability testing. We should be looking at screening and not full scale qualification testing. Much larger samples will be required eventually for MTBF determination.

11. Jim pointed out that GaAs power FETs are currently passivated with silicon nitride. He was not aware of what difficulties were encountered when these devices contained airbridges.

12. Don had prepared an outline of his ideas for MMIC reliability studies. There are attached.
1. **Discrete FET Failure Mechanisms**
   - Electromigration
   - Ohmic Contact Degradation (Interdiffusion)
   - Drain Burn-Out (Surface Degradation/High Field)
   - Schottky Barrier Degradation (Interdiffusion)
   - Active Layer Degradation (Traps)
   - Gate Burn-Out.

2. **Possible Additional Failure Mechanisms for MMICs**
   - Isolation Degradation (Ion Implant Anneal)
   - Thermal Fatigue (Chip or Die Bond, Large Chips, Vias)
   - Strain Gradient Induced Defect Migration (Traps)
   - Capacitor Dielectric Failure
   - Other Passive Device Failures
   - Interconnection Failures (Step Coverage, etc.)
   - Unknown (Murphy Mechanisms)

3. **Differences From Si MICs**
   - GaAs Does Not Invert (Surface Instabilities Not as Critical)
   - No Gate Oxide Breakdowns (MESFETS)
   - Au Based Metal is Electromigration Resistant
   - GaAs is Brittle and Weaker than Si
   - GaAs is 3X Less Heat Conductive
   - GaAs Has Higher Band Gap - Less Thermal Leakage
4. Approach to Reliability Assurance

- Evaluate Materials and Processes to Look For Instabilities
  - Ohmic Contact Stability vs. t at T
  - Schottky Barrier Stability vs. t at T
  - Isolation Stability vs. t at T
  - Electromigration Resistance of Metal Systems

- Evaluate FET Stability
  - Life Tests Under Operation at Elevated T

- Project Expected Life of FETs vs. T

- Feedback Information from Above to Process and Design

- Use Process TEG/Hot Probe Approach and Temperature Anneal for Above

- DC Life Test Large Sample at Elevated Temperatures

- RF Life Test Modest Sample at Elevated Temperatures to Verify DC Results

- T-cycle Testing of Packaged MMICs to Evaluate Fatigue Susceptibility

- Thermal Modeling and Measurement

- Detailed Failure Analysis and Feedback

5. Elements of Proposed Program

- Obtain process TEGs from MMIC manufacturers and test for all of the mechanisms listed above. These would be hot probing tests as well as packaged TEGs, where desirable.

- Define standard set of TEGs and tests to be passed before process and MMICs are qualified.

- Temperature-cycle test GaAs chips 4-5 mil thick, .250" square, with vias. Use either actual MMICs or special TEGs for these tests.

- Life test of MMICs at elevated temperature with T-cycling. Bulk of units subjected to DC life test with smaller sample tested under RF operation to verify DC results.

- Thermally characterize MMICs before life test using modeling and measurements

- Evaluate need for hermeticity.
Avantek
Finn Wilhelmsen and Charles Huang
9/8/83

1. Avantek is involved in the development of GaAs MMICs which they intend to market commercially in the near future. Their module work is currently limited to medium power, wideband amplifiers up to 20 GHz where they feel a strong market exists. They currently have a 6-18 GHz MMIC amplifier program from ONR. They expect to market a MMIC GaAs amplifier within a year.

2. They have a strong interest in reliability of discrete GaAs devices as well as MMICs. Finn is Director of Product Assurance and is coordinating this effort. Their approach has been to perform reliability tests on discrete devices (FETs, resistors, capacitors, inductors, etc.) and then integrate and project reliability of the MMICs from the discrete device data. They want to know if this is acceptable to DoD - the answer would appear to be no. What does DoD want next?

3. They are participating in a FET reliability program with Hughes, Aerospace and SAMSQO which is directed towards space qualification of FETs. They are considering a facility for space qualification of GaAs devices and circuits which would be separate from the present Avantek facility. The facility would service government needs and would require in excess of $3M to establish.
4. Avantek has performed testing of GaAs discrete devices used in MMICs and sees no major problem areas. They have no difficulties with respect to reliability of Schottky barriers, ohmic contacts, electromigration, resistors, inductors or capacitors. Their process is firmly established in their opinion, and they believe the time is appropriate for fullscale reliability testing of GaAs MMICs. They recommend 50 chips at each of three different temperatures - 275°C, 250°C and 225°C. These temperatures are currently being used with their FET reliability tests. A major problem related to high temperature testing of these chips under dc and RF bias is obtaining proper dc bias. The resistor values for the built-in bias are functions of temperature and will likely drastically change the bias point as the circuits are tested at high temperatures. It may be possible to modify the external bias supply to compensate so as to maintain an acceptable bias level. However, this bias problem must be carefully considered prior to testing.

5. Avantek has very limited RF stress test capability, but they are planning to add such facilities in the near future. Since they are a commercial supplier, this test capability is important.

6. Silicon nitride is used as a cap for their devices, both discrete and monolithic. This 1000Å nitride layer is deposited over the airbridges. Finn is considering the use of polyimide on top of the nitride for insurance.
7. They expressed strong support for the suggestion of standardizing wafer test patterns so that vendors could provide common test patterns to sponsors to assist in reliability testing. They already use an abundance of test patterns, particularly during circuit development stages.

8. Charlie, who is responsible for the design processing, wanted to know what types of reliability tests DoD would require.
1. Raytheon has initiated a reliability effort on MMICs. Next year's plans are to identify problem areas and will not involve MTTF determination. They feel that the timing is appropriate for such small studies but that it is too early for full scale testing, at least for their devices. Some firms such as Avantek might however be ready for full scale testing of their MMICs since they are more advanced than most firms. All such studies should involve simple modules such as one or two stage amplifiers. Raytheon plans to utilize a 2-stage medium power amplifier which they are developing for in-house system programs; this unit will be produced in relatively large quantities.

2. Their planned program will involve three areas of investigation: Substrate material qualification, thermal soak under DC bias, and study of radiation effects. Anticipated level of these efforts is $500K per year with three senior staff members full time. Equipment is presently being assembled with plans for simultaneous dc test of 20 devices and 10 devices on RF test. They feel that these quantities are statistically adequate for these preliminary tests. In the future they are planning for Raytheon SMDO, their manufacturing operation, to bear the cost of large scale tests.

3. In the area of substrate material qualification, they are planning to study substrate criteria that lead to good performance and long life. Measurements have shown that the substrates contain impurities such as copper which out-
diffuse into the active layer and degrade mobility. They plan to use FETs for test structures. Extensive use will be made of test patterns such as contact structures, fat FETs, etc. on processed wafers. Analysis of the substrate will be performed with SIMS and pulsed transient spectroscopy (PTS) which have been used previously by others for examining copper in the substrates. These studies will have a major impact on discrete FETs as well as MMICs. Raytheon contends that work is needed on the "bottom side" (i.e. substrate) of the devices since most of the studies have concentrated on the "top side" (i.e. ohmics and Schottky barriers). Their standard process will involve ion implantation directly into the substrate and will not utilize a buffer layer.

4. Facilities are presently available for burn-in of discrete devices under dc bias at elevated temperatures with an argon or dry nitrogen environment. They will expand these facilities to handle MMICs. The objective of these studies is to identify the cause of problems and will thus involve detailed failure analysis. For example, they have observed drain metal migration but do not know whether this is actually causing deterioration of performance. RF test systems for MMICs will be assembled next year and will utilize IMPATT diodes as RF drivers. The MMICs intended for these tests are two stage amplifiers which have separate bias leads such that proper bias adjustments can be made at elevated temperatures. The temperatures to be used in these tests are in question. Hot spots on the MMICs are a problem and must be considered. They are working with liquid crystals for mapping the temperature across the chips. They don't know whether or not they can put RF on the chips with the liquid crystal film or whether it can be stripped without damage. DC tests with the liquid crystals have shown
a wide distribution of temperatures across the chips. These liquid crystals give high resolution, and 1 μm gates can be seen to light up. Temperature differentials down to several degrees can be identified, but the temperature range is rather narrow. Liquid Crystal Applications is working with them and are making cholesteric type crystals up to 100°C which will give less extrapolation to the operating temperature. This technique should be a good procedure for checking hot spots, but they will use the forward voltage drop of the gate to determine the average channel temperature. A test setup for making this measurement is being assembled; the measurement will involve pulsing the gate to forward bias and measuring its current. Note that the reverse bias voltage, which is normally used with IMPATT diodes to measure the temperature, is not useful since the reverse breakdown characteristic is not sharp.

5. Raytheon will be working with Sandia to evaluate radiation effects on GaAs MMICs and define baseline numbers. Raytheon will supply the devices and Sandia will perform the testing. The Japanese have performed gamma ray tests on x-band preamps and have found no change up to 10⁷ rads; some effects were observed at 10⁸ rads, but the devices were still operative at 10⁹ rads. Sandia has tested discrete GaAs devices, but the effects on passive devices, including transmission lines, are unknown. They are worried about substrate conversion and effects on dielectrics. Sandia will perform flash gamma, integrated neutron and average gamma tests. With the flash gamma, the dc characteristics can be monitored during the tests.

6. Fault isolation is performed with dc probing, but they are investigating RF probes. Their experience is that faults can
not be isolated in many circuits due to inaccessibility of components due to overlays. They will attempt, particularly with MMICs to be used in reliability studies, to design chips with all terminals accessible from the top side. Their feeling is that in many instances detailed failure analysis will be possible only by the manufacturer.

7. Their normal procedure is to develop the individual components separately and then combine on a single chip. Generally, they cannot cleave the chip to isolate components. Special chips could be designed for reliability investigations if required.

8. Raytheon is under heavy pressure by their system people to get MMICs into systems; presently they have no field equipment with MMICs. They plan a pilot production in 1984 for a medium scale, medium power, FET amplifier with a 2-3K level of production. No one seems to have MMICs in hardware at this time, but Avantek is probably the closest.

9. Continued studies on reliability of gates, ohmic contacts, etc. are required in Raytheon’s opinion. They believe that the built-in one year delay in funding from RADC is desirable since preliminary testing is on-going in several firms and should provide data in the near future. The development of industrial standards for semi-insulating GaAs substrates is an appropriate area for study. Also, standardization of failure criteria is an excellent area for investigation.

10. Raytheon uses polyimides in their circuits, and this material is in direct contact with the GaAs. Also, an adhesion promoter (Pyralin) is used prior to application of
the polyimide. They have performed limited testing on discrete GaAs FETs with polyimides and have observed no difficulties, but more extensive tests are required. The curing schedule on the polyimide is important. Dupont specifies a 450°C cure using a hot plate rather than an oven so as to cure from the bottom surface, thus driving moisture to the top. Raytheon received extensive literature from Dupont related to polyimides. Raytheon cures at 250°C, but the wafer is subsequently exposed to 300°C during nitride deposition. Their feeling is that polyimides are obviously not limiting reliability at this time—other problems are more critical. Raytheon uses plasma to etch the polyimide; others have reported that chemical etches introduce a problem but there is no confirmation of this.

11. The present Au-Ge-Ni ohmic contact technology has many problems and the development of a new approach is extremely desirable. The use of single crystal germanium for ohmic contacts justifies further development.

12. Raytheon SMDO uses aluminum gates while the Research Division uses Ti/Pt/Au. They are not sure about the best choice, but neither appears to be limiting reliability at this point. They use E-beam evaporation for the Ti/Pt/Au gates and do experience problems with deposition of the pure titanium. Ti/W/Au may be a better choice but sputtering is required along with a thermal anneal.

13. Rf probing is desirable but may not need to go to 18 GHz. Probing at 2 GHz can be used in many instances to check the RF health of the circuit.
1. Eric and Reed have developed RF probes for analog and digital GaAs ICs which work very well. They continue to work on these probes and feel that RF probing is not only feasible but mandatory to development of these circuits. They are currently developing a work station which will have four lines of probes with five probes per line yielding a total of 20 probes, each with 50 ohm impedance. These probes are moved mechanically from chip to chip for on-wafer probing. Probe cards are also under development.

2. According to Reed, they have also developed an active probe with 20 fF input capacitance and 200 Psec rise time for digital applications. This probe does not need ground return paths. Unfortunately, it is too slow for the x-band analog circuits.

3. These probes are built similar to those described in the article published by Eric and Reed. Typically, 2 mil pads are required to make contact. There is no reason that internal chip probing cannot be performed providing probe pads are available and the probes don't adversely load the circuit. Unfortunately, for most MMIC's the probe loading is unacceptable and some type of isolation must be available. Eric suggested the use of an integrated resistor to isolate the probe pad from the point in the circuit where probing is desired. If the resistor is less than 1 mm in size, it appears to be a lumped element resistive divider when probed and is an open circuit otherwise. Eric said that he has built circuits using this technique and it works well.
Obviously, careful modeling of this resistive coupling network is required. Capacitive coupling is also a possible approach.

4. The approach used by Tektronix is to place probe pads as desired in the circuit and then break the line with laser scribing. This is apparently a standard procedure with Tektronix.

5. Limited experiments have been performed on taking noise data with these probes, but more work is required in this area. Considerable calibration is required to deembed the probe effects, but this appears feasible.

6. Reed and Eric have recently formed a company, Cascade Microwave, to produce these probes since Tektronix has no desire to pursue this market. The patents have been assigned to Reed and Eric. They predict that they will have probes ready to market in the early fall 1983. A great deal of interest has been expressed by other companies in these probes and several organizations are attempting to duplicate the probes. Perhaps RADC might be interested in supporting this probe development with a small business set aside.

7. I asked Eric about the development approach used at Tektronix for MMICS. His response was that they typically do a very thorough design and have been very successful in going directly from the design to total integration. I pointed out that other firms are not so successful in this procedure. He feels the primary reason for their success is the detailed characterization of discrete devices and the use of these characteristics in their design procedure which involves detailed sensitivity analysis of the circuits using
"spice" circuit modeling. Tektronix is apparently spending considerable effort characterizing on-wafer devices using their probes interfaced with an automatic network analyzer for data acquisition. This approach allows them to quickly and cheaply determine variations in device or circuit parameters across the wafer. These data are then used to determine average parameters with statistical limits for use in the computer aided design and analysis of MMICs. The ability to perform a meaningful sensitivity analysis using real data from a large number of devices is extremely important and is made economically feasible by the ability to perform on-wafer characterization using these RF probes. Obviously, this approach assumes that the MMIC process is reproducible. Many other firms are apparently not willing or able to invest in packaging and characterizing large numbers of devices from numerous wafers to establish good empirical device models.

8. DC probing is used to a great extent in failure analysis of GaAs monolithic circuits at Tektronix. Reed felt that dc probing will reveal many of the potential failures. Some screening will be performed with dc, but RF is still important.

9. The current level of integration at Tektronix is the system level where they are beginning to integrate functional blocks. Their reliability testing to date involves wiring ring oscillators and subjecting them to thermal soak under dc and RF.