GEORGIA INSTITUTE OF TECHNOLOGY
OFFICE OF CONTRACT ADMINISTRATION

PROJECT ADMINISTRATION DATA SHEET

Project No. A-2690

Project Director: Mr. G. N. Hill

Sponsor: Hughes Aircraft Company; Space and Communications Group;
El Segundo, CA 90245

Type Agreement: Purchase Order No. S8-738203-LV3

Award Period: From 4/16/81 To 4/30/82

Sponsor Amount: $66,116

Cost Sharing: None

Title: Millimeter Wave Mixer Diode - Phase II

ADMINISTRATIVE DATA

1) Sponsor Technical Contact:
   Mr. Bernie Walsh
   Hughes Aircraft Company
   1950 East Imperial Highway
   El Segundo, CA 90245
   213/648-1675

   Defense Priority Rating: None

2) Sponsor Admin/Contractual Matters:
   Mr. R. W. Nastri
   Bldg. S12, Mail Station W323
   Hughes Aircraft Company
   P. O. Box 92919 - Airport Station
   Los Angeles, CA 90009
   213/648-8693

   Security Classification: None

REstrictions

See Attached N/A Supplemental Information Sheet for Additional Requirements.

Travel: Foreign travel must have prior approval — Contact OCA in each case. Domestic travel requires sponsor approval where total will exceed greater of $500 or 125% of approved proposal budget category.

Equipment: Title vests with Sponsor; however, none authorized/proposed.

COMMENTS:

COPIES TO:

Administrative Coordinator
research Property Management
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Legal Services (OCA)
Library
EES Public Relations (2)
Computer Input
Project File
Other
GEORGIA INSTITUTE OF TECHNOLOGY
OFFICE OF CONTRACT ADMINISTRATION

SPONSORED PROJECT TERMINATION SHEET

Date 6/2/83

Project Title: Millimeter Wave Mixer Diode — Phase II

Project No: A-2960

Project Director: G. N. Hill

Sponsor: Hughes Aircraft Company

Effective Termination Date: 3/31/83

Clearance of Accounting Charges: 3/31/83

Grant/Contract Closeout Actions Remaining:

- Final Invoice
- Final Fiscal Report
- Final Report of Inventions
- Govt. Property Inventory & Related Certificate
- Classified Material Certificate
- Other

Assigned to: EML/PSD

COPIES TO:

Administrative Coordinator
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Accounting
Procurement/EES Supply Services
Research Security Services
- Reports Coordinator (OCA)
- Legal Services (OCA)
- Library
EES Public Relations (2)
Computer Input
Project File
Other G.N.Hill
MILLIMETER WAVE MIXER DIODE - PHASE II

Contract period covered
16 April 1981 through 31 October 1981
P. O. No. S8-738203-LV3

A-2960

Submitted to
Hughes Aircraft Company
El Segundo, California 90245

by
Physical Sciences Division
Electromagnetics Laboratory
Engineering Experiment Station
Georgia Institute of Technology
Atlanta, Georgia 30332

Contracting through
Georgia Tech Research Institute
Georgia Institute of Technology
Atlanta, Georgia 30332
FOREWORD

This report is submitted in lieu of scheduled monthly status letter for the period of April 16, 1981 to October 31, 1981. The contract negotiations and the specific deliverable schedule have only recently been completed and distributed.

INTRODUCTION

Before proceeding to fabrication of the final deliverable diodes, several equipment modification and process evaluation steps were performed. The modifications included equipment used for SiO$_2$ deposition and vacuum evaporation; the goal being to improve process control in the areas of insulating layers and metal film thickness.

Evaluation of the three Gallium Arsenide wafers purchased at the end of phase one has begun. Samples diodes are available; however, the quality is not presently up to the level of the best diodes produced in phase one.

Modifications to the life test fixture have been completed and initial evaluation of the fixture has been completed. A constant current test setup has also been completed and is at present being tested. This setup will facilitate testing of the deliverable diodes.

The new photomask design has been purchased as well as nickel-gold wire for the whisker contacts. A stock of whisker contacts is being readied.

EQUIPMENT MODIFICATION

SiO$_2$ Deposition System

The SiO$_2$ deposition system was modified to insure a uniform deposit
over at least 0.6 in$^2$. This modification is complete and excellent uniformity has been obtained over 1.22 in$^2$. The modification required complete rebuilding of the heated stage and deposition chamber. The old system used a stationary temperature controlled heated platen enclosed by a glass chamber having a volume of 350cc. The new system consists of rotating temperature controlled heated platen enclosed by a similar but larger (600cc) chamber. A positive pressure vent system has also been incorporated.

The growth rate has been calibrated and is 702 Å per minute; 7.12 minutes being required for 5000 Å.

E-Beam Evaporator

The E beam system shutter actuator assembly has been changed to a bellows type having a travel of 0.63 inches. The previous actuator traveled only 0.090 inches and would occasionally hang up during operation. The new assembly was especially designed to provide positive shutter movement. Its performance has been flawless.

The E-gun crucibles have been recharged with metals and the titanium sublimator filaments have been replaced. A base pressure of $1 \times 10^{-10}$ Torr is being maintained in the main chamber.

Life Test Fixture and Test Results

Following the conclusion of phase one and after discussing the problem of reliably testing the diodes under thermal stress, it was decided to attempt to utilize the orientation-cross present on each chip as a test diode rather than one of the more difficult to contact 3 µm diodes. It was felt that a thermocompression wire bond to a larger diode would be much more stable than the whisker-type of contact. Previous tests of
3 μm diodes during phase one required contacting the anode dot with an etched whisker. These whisker contacts were unstable at the high temperatures. The reasons for the instability has not been thoroughly understood. One line of thought is that softening or annealing of the whisker causes a pressure change on the contact or diode Schottky barrier.

Recently diode chips from three phase one runs have been mounted into conventional diode packages. Thermocompression wire bonds were made to the cross geometry. Five diodes were bonded this way and placed into the life test fixture. Room temperature dc measurements were performed to determine $n$ and $R_s$ prior to exposure to thermal soak. The fixture temperature was then set to 325°C, and the diode bias current was set to 30 mA. The diode voltages were then measured on a daily basis. The test results are shown in table one and in figure 1. The test of diodes

\[
\begin{array}{cccccc}
\text{Diode} & \text{T = 0} & \text{T+191 Hrs @ 325°C} & \text{T+235.5 Hrs @ 325°C} \\
(1) 8A14-4-1 & 1.04 & 0.81Ω & 1.12 & 0.75Ω \\
(2) 8A16-17-1 & 1.06 & 0.57Ω & 1.38 & 1.35Ω \\
(3) 8A16-17-2 & 1.06 & 0.67Ω & 2.84 & 5.62Ω \\
(4) 83012-18-1 & 1.09 & 5.45Ω & 1.38 & 0.10Ω \\
(5) 83012-18-2 & 1.09 & 1.25Ω & 1.10 & 0.78Ω \\
\end{array}
\]

Table 1. Cross Geometry Test Results

2 & 4 was interrupted at 191 hours room in order to perform a room temperature measurement. Note that diode 4 was a very poor device left in test under the assumption that rapid degradation would occur. This did not
occur and actually an improvement was noted. However, the interruption did cause a step deflection in the time voltage plots of figure 1b and 1d. These results demonstrate that the cross can be a suitable test area once the maximum acceptable voltage change is established.

These tests further demonstrate that the degradation noted in tests performed during phase one are again evident. In particular, the final run 83012-18 was metallurgically more stable at high temperature.

**Constant Current Test Circuit**

Parametric data required on mixer diodes includes diode voltage \(V_d\) at eight different diode current levels ranging from 10 nanoamperes to 10 milliamperes. Diode voltage measurements made during phase I were obtained by setting the various current levels utilizing a bias adjust box. This method worked well; however, it was somewhat time consuming due to the variable resistance technique and the wide range of current settings required. In order to efficiently test a large number of diodes, a constant current source capable of providing the eight current levels by simple switch selection was desired.

Several design approaches were considered including op amp circuits; however, the seven decade range involved eliminated many approaches. Monolithic circuits are well suited for constant current applications in the millampere range but are not as effective at lower current levels. The schematic shown in figure 2 is a circuit designed to provide the constant current levels. The design is based on a current mirror technique which is popular in analog integrated circuit design. At the high current levels an emitter resistor at transistor \(Q_2\) is not used and the collector current of \(Q_2\) is determined by the equation
\[ I_2 = \frac{V_1 - V_{BE}}{R_1} \]

where \( V_1 \) - output voltage of the \( V_{BE} \) = base - emitter voltages of \( Q_1 \) and \( Q_2 \)

\( R_1 \) = value of the resistance in the base collector circuit of \( Q_1 \)

\( A_{E1} \) = emitter area of \( Q_1 \)

\( A_{E2} \) = emitter area of \( Q_2 \)

For matched transistors with the same emitter area, the constant current value is determined by

\[ I_2 = \frac{V_1 - V_{BE}}{R_1} \]

and is stable provided \( V_1 \), \( V_{BE} \) and \( R_1 \) (which are all independent of the load) do not change.

A LM 394 supermatch transistor pair is used for \( Q_1 \) and \( Q_2 \) transistors. Current levels are selected with a dual wafer rotary switch which connects one of eight \( R_1 \) resistors and one of four \( R_2 \) emitter resistors or a direct circuit from the emitter of \( Q_2 \) to ground.

\( R_2 \) emitter resistors are used for the low current settings. When connected, the potential across \( R_2 \) is the difference between the base emitter voltages of \( Q_1 \) and \( Q_2 \) given by

\[ R_2 I_{E2} = V_{BE1} - V_{BE2} \]

Since \( I_{E3} = I_2 \), the value of \( R_2 \) needed to set a current level of \( I_0 \) can be found by

\[ R_2 = \frac{I}{I_2} (V_{BE1} - V_{BE2}), \]
but \[ V_{BE} = \frac{KT}{q} \ln \frac{I_E}{J_{SA_E}} \]

and for matched transistors

\[ J_{SA}E_1 = J_{SA}E_2, \text{ so} \]

\[ R_2 = \frac{KT}{q} \ln \frac{I_{E1}}{I_{E2}} \quad \text{or} \]

\[ R_2 = \frac{26mV}{I_0} \ln \frac{I_1}{I_2} \text{ at room temperature.} \]

Multiturn trim pots allow precise adjustment of the constant current which is sensed by measuring the voltage across a 1000 ohm (0.1%) resistor.

Dual binding posts are used to connect the diode test fixture to the current source. Curve tracer and DVM connections are also made with dual binding posts. The diode under test may be switched from the current source to the curve tracer in order to facilitate making initial diode contact and measuring breakdown voltage.

_Gallium Arsenide Materials Evaluation_

The three wafers purchased from Raytheon are presently being evaluated. A portion of wafer 8A501 has been processed. The dc test results show these diodes to be slightly inferior to the best diodes delivered during phase one. Table 2 shows this comparison. This substandard performance should not at this point be interpreted to represent the expected quality of diodes produced from all three of the wafers, or even additional runs from this same 8A501 wafer. Further runs must be made to effectively evaluate this material. The gallium arsenide specifications and impurity profile are included in figures 3, 4 and 5.
### Phase one

<table>
<thead>
<tr>
<th>Diode Run</th>
<th>n</th>
<th>$R_S$</th>
</tr>
</thead>
<tbody>
<tr>
<td>8A16-17</td>
<td>1.12</td>
<td>3.62</td>
</tr>
<tr>
<td>8A16-16</td>
<td>1.14</td>
<td>5.00</td>
</tr>
<tr>
<td>8A14-4</td>
<td>1.11</td>
<td>4.05</td>
</tr>
<tr>
<td>8A12-18</td>
<td>1.14</td>
<td>5.17</td>
</tr>
<tr>
<td>83012-18</td>
<td>1.13</td>
<td>7.88</td>
</tr>
</tbody>
</table>

### Phase two

<table>
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<th>Diode Run</th>
<th>n</th>
<th>$R_S$</th>
</tr>
</thead>
<tbody>
<tr>
<td>8A501-1</td>
<td>1.23</td>
<td>7.16</td>
</tr>
<tr>
<td>8A501-2</td>
<td>1.18</td>
<td>7.73</td>
</tr>
<tr>
<td>8A501-3</td>
<td>1.33</td>
<td>8.32</td>
</tr>
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</table>

Table 2. Comparison of Phase I and Phase II Diodes.

**Photomask**

The new mask was received during the first week of October. A long delay resulted due to problems encountered at Qualitron. The changes in the mask design, although simple, apparently caused them a great deal of trouble. Secondly it is felt that due to the small request, the priority was downgraded. Furthermore, only one mask out of the two ordered has been received. The profile dots although correct in polarity, are of the incorrect size. Four 2 mil dots are printed instead of the one 10 mil dot which was specified. These dots may in fact be suitable and in the interest of continuing work without further delay, one mask will be accepted. Meanwhile, Qualitron has promised to correct this problem.

**PLANS FOR NEXT MONTH**

- Continue processing wafers.
- Deliver test diodes for rf evaluation.
CROSS LIFE TEST

DIODE (1)

8 A 4-4-1

T = 325°C

I_{DIODE} = 30 mA

VOLTAGE (VOLTS)

10 mA

50

1 mA

100

.5 mA

150

.1 mA

200

0.5

250

0.1

300

0.05

350

50

100

150

200

250

300

350

400

TIME

Fig. 1a
CROSS LIFE TEST

DIODE (2)
8A-16-17-1
T = 325°C
I_Diode = 30 mA

VOLTAGE (VOLTS)

10 mA

1 mA

0.1 mA

TIME (mS)

50 100 150 200 250 300 350 400
CROSS LIFE TEST

DIODE (3)
8A-16-17-2
T = 325°C
I_Diode = 30 mA

VOLTAGE (Volts)

TIME (Hours After Load)

50 100 150 200 250 300 350 400

10 mA
1 mA
0.1 mA
CROSS LIFE TEST

DIODE (4)
83012-18-1
T = 325°C
I_Diode = 30 mA

VOLTAGE (VOLTS)

0 mA

1 mA

50 100 150 200 250 300 350 400

TIME
Figure 2. Schematic Diagram - Constant Current Source.
QUALITY ASSURANCE
GaAs Epitaxial Wafer
Number EA497

For FET Type Devices
□ Low Noise
□ Power
□ Other

For IMPATT Type Devices
□ Flat Profile
□ Read Profile
□ Other

For Single Drift
□ Double Drift
□ Thick Buffer
□ Standard Buffer
□ p' contact

Customer
Georgia Tech

Date: 1/9-31

For FET Type Devices
Low Noise
Power
Other

Customer Order No.: 020-401-A2561

For IMPATT Type Devices
Flat Profile
Read Profile
Other

Spec. No.

Attention

Contract No.


SUBSTRATE
Supplier SE
Crystal Boule No.: 0180
Slice No. 93

Orientation 2° off <100> toward <110>

Pregrowth Thickness 40.0 μm

Carrier Concentration: 1.8 x 10¹¹ cm⁻³

Dopant: Te

 Resistivity** 1.5 x 10⁻³ Ω·cm

ELECTRICAL CHARACTERISTICS

<table>
<thead>
<tr>
<th>No.</th>
<th>Layer Type</th>
<th>Carrier Concentration</th>
<th>Dopant</th>
<th>Thickness</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Buffer</td>
<td>&gt; 2 x 10¹⁵ cm⁻³</td>
<td>S1</td>
<td>5.0 μm</td>
</tr>
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<td>2</td>
<td>Active</td>
<td>1.0 x 10¹⁵ cm⁻³</td>
<td>S1</td>
<td>0.26 μm</td>
</tr>
<tr>
<td></td>
<td>Active</td>
<td>x 10¹⁴ cm⁻³</td>
<td></td>
<td>μm</td>
</tr>
<tr>
<td></td>
<td>Spike</td>
<td>x 10¹⁷ cm⁻³</td>
<td></td>
<td>μm</td>
</tr>
<tr>
<td></td>
<td>Contact</td>
<td>x 10 cm⁻³</td>
<td></td>
<td>( ) nm</td>
</tr>
</tbody>
</table>

Wafer Size 2.2 x 3.5 cm
Area 6.16 cm²
Surface Morphology 2

Q⁺: 1 x 10¹² e⁻·cm⁻³
Vₖnee volts (from C vs V curve)

C₀⁺: 11.63 x 10⁴ pF·cm⁻²
Interface 0.05 μm/decade

DELIVERY AUTHORIZATION

Delivery authorized
□ to fill order
□ to fulfill contractual obligations
□ For Device Research
□ For Process Research
□ For Calibration
□ Other

Amount Ordered 3
Amount Delivered 1

William H. LaBodier
<table>
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<tr>
<th>Etch</th>
<th>C</th>
<th>Time</th>
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<tr>
<td>1st</td>
<td>151.6</td>
<td>0</td>
</tr>
<tr>
<td>2nd</td>
<td>151.2</td>
<td></td>
</tr>
<tr>
<td>3rd</td>
<td>151.7</td>
<td></td>
</tr>
<tr>
<td>4th</td>
<td>151.1</td>
<td></td>
</tr>
<tr>
<td>5th</td>
<td>150.9</td>
<td>30</td>
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<tr>
<td>6th</td>
<td>163.0</td>
<td>60</td>
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<tr>
<td>7th</td>
<td>483.0</td>
<td>90</td>
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<tr>
<td>8th</td>
<td>528.3</td>
<td>180</td>
</tr>
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**Figure 3a**
QUALITY ASSURANCE
GaAs Expitaxial Wafer
Number 8A99

For FET Type Devices
Low Noise [ ] Power [ ] Other [ ]
Buffer [ ] Contact Layer [ ]

For IMPATT Type Devices
Flat Profile [ ] Read Profile [ ] Other [ ]
Single Drift [ ] Double Drift [ ] Thick Buffer [ ] Standard Buffer [ ] p⁺ contact [ ]

Customer: Georgia Tech
Customer Order No.: 020-601-A2566-000

Attention: __________________________ Memo No.: __________________________

SUBSTRATE
Supplier: SE
Orientation: 2° off <100> toward <110>
Carrier Concentration: 1.8 x 10¹⁸ cm⁻³
Resistivity**: 1.5 x 10⁻³ Ω·cm

ELECTRICAL CHARACTERISTICS

<table>
<thead>
<tr>
<th>No.</th>
<th>Layer Type</th>
<th>Carrier Concentration</th>
<th>Dopant</th>
<th>Thickness</th>
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</thead>
<tbody>
<tr>
<td>1</td>
<td>Buffer</td>
<td>&gt;2 x 10¹⁸ cm⁻³</td>
<td>S¹</td>
<td>3.0 μm</td>
</tr>
<tr>
<td></td>
<td>Buffer</td>
<td>10 cm⁻³</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Active</td>
<td>1.0 x 10¹⁶ cm⁻³</td>
<td>S¹</td>
<td>0.22 μm</td>
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<td>Active</td>
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<td></td>
<td>Spike</td>
<td>x10¹³ cm⁻³</td>
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<td></td>
</tr>
<tr>
<td></td>
<td>Contact</td>
<td>x10 cm⁻³</td>
<td></td>
<td></td>
</tr>
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</table>

Wafer Size: 2.2 x 2.5 cm
Area: 6.16 cm²
Surface Morphology: 2

C⁺: 1 x 10¹² e⁻·cm⁻³
C₀: 1.2 x 10¹⁰ pF·cm⁻²
V_knee volts (from C vs V curve)
Φ_interface 0.05 μm/decade

DELIVERY AUTHORIZATION

Delivery authorized to fill order to fulfill contractual obligations
For Device Research [ ] For Process Research [ ] For Calibration [ ] Other [ ]
Amount Ordered: 3 Amount Delivered: 2

William H. Labosier
Date: 4-9-81

Figure 4
**Figure 4a**
QUALITY ASSURANCE
GaAs Expitaxial Wafer

For FET Type Devices
☐ Low Noise
☐ Power
☐ Other

with
☐ Buffer
☐ Contact Layer

For IMPATT Type Devices
☒ Flat Profile
☐ Read Profile
☐ Other

☐ Single Drift
☐ Double Drift
with
☐ Thick Buffer
☒ Standard Buffer
☐ p" contact

Customer
George I Tech

Customer Order No.
02-01-A2566-000

Spec. No.
11-01-S4140

93-749-99

SUBSTRATE
Supplier
S6

Crystal Boule No.
0180
Slice No.
105

Orientation
off <100> toward <110>

Pregrowth Thickness
420 μm

Carrier Concentration:
1.8 x 10^{16} cm^{-3}

Dopant:
Te

Resistivity**
1.5 x 10^{-3} Ω cm

ELECTRICAL CHARACTERISTICS

<table>
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<tr>
<th>No.</th>
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<th>Dopant</th>
<th>Thickness</th>
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<td>&gt;2 x 10^{18} cm^{-3}</td>
<td>S1</td>
<td>5.0 μm</td>
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<tr>
<td>2</td>
<td>Buffer</td>
<td>x10 cm^{-3}</td>
<td>S1</td>
<td>0.24 μm</td>
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<td></td>
<td>Active</td>
<td>1.5 x 10^{16} cm^{-3}</td>
<td>S1</td>
<td></td>
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<tr>
<td></td>
<td>Active</td>
<td>x10^{16} cm^{-3}</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Spike</td>
<td>x10^{17} cm^{-3}</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Contact</td>
<td>x10 cm^{-3}</td>
<td></td>
<td></td>
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</tbody>
</table>

Wafer Size: 2.3 x 2.8 cm
Area: 6.44 cm^2
Surface Morphology: 2

Q*: ______ x 10^{13} e^- cm^{-2}
V_{knee}: _______ volts (from C vs V curve)
C_o: 12.8 x 10^{3} pF-cm^{-2}
Interface: 0.05 μm/decade

DELIVERY AUTHORIZATION

Delivery authorized
☒ to fill order
☐ to fulfill contractual obligations

☐ For Device Research
☐ For Process Research
☐ For Calibration
☐ Other

Amount Ordered: 3
Amount Delivered: 3

Figure 5

William H. Labossier
Date: 4-9-81
Figure 5a
Status Report No. 8

MILLIMETER WAVE MIXER DIODES - PHASE II

Contract period covered
1 November 1981 through 30 November 1981
P. O. No. S8-738203-LV3

A-2960

Submitted to
Hughes Aircraft Company
El Segundo, California 90245

by
Physical Sciences Division
Electromagnetics Laboratory
Engineering Experiment Station
Georgia Institute of Technology
Atlanta, Georgia 30332

Contracting through
Georgia Tech Research Institute
Georgia Institute of Technology
Atlanta, Georgia 30332

2 December 1981
INTRODUCTION

During the past month, mixer diodes have been fabricated from portions of two Raytheon wafers, 8A497(A) and 8A499(A). The initial life test experiments of 8A497(A) have recently been completed. These test results are contained in this status letter.

The photomask problem, including profile dot size and diode array orientation has been resolved.

DIODE FABRICATION

Sample diodes have been fabricated from the two remaining Raytheon wafers, 8A497 and 8A499. All of the process steps have proceeded without incident. The dc data shown in table one indicate the best diodes in terms of quality factor are from the GT8A497(A) wafer portion.

<table>
<thead>
<tr>
<th>Wafer No.</th>
<th>Diode Dia. μm</th>
<th>η</th>
<th>Rs</th>
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<tr>
<td>GT8A497A</td>
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<td>1.13</td>
<td>11.31</td>
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<tr>
<td></td>
<td>2.0</td>
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<td></td>
<td>5.0</td>
<td>1.16</td>
<td>2.62</td>
</tr>
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</table>

Table 1. DC Test Data, GT8A497A and FT8A499A.

LIFE TEST

Five packaged GT8A497A diodes were subjected to the 325°C temperature stress in order to establish a comparison between these diodes and those considered to be the most stable of the phase one diodes, 83012-18.
Two of the 3 \( \mu \)m dot diodes were contacted using the whisker contact. The remaining three were wire contacts to the cross geometry. The diodes were biased, 0.25 mA for the 3 \( \mu \)m dots and 30 mA for the cross diodes. Diode, number two was to serve a dual purpose. Both biased and non biased tests could be performed by attaching a lead to the cross as in numbers 3, 4 and 5 but not connecting it to the bias source. This arrangement then permitted the whisker to be the bias contact for one of the dot diodes under biased test. The open circuit cross would then serve as a good high temperature storage test.

DC and curve tracer data were taken before and after the high temperature test to determine \( n \) and \( R_s \) and to visually log the forward and reverse characteristics.

The diode bias voltage was measured daily and plotted on the voltage vs time plots shown in figures 1 thru 5.

During the first series of tests performed, (last report) diode failure was assumed if a noticeable change in the bias voltage plot was observed. This effect has not been observed with the latest GT8A497A cross diodes; yet, the \( n \) and \( R_s \) show significant degradation after 336.5 hours. The whisker contacted diodes both failed catastrophically, number one after 95 hours and number two after 261 hours. Both open circuited (lost contact); therefore, no after-temperature stress information could be obtained. Table two shows the before and after heat stress dc data.

<table>
<thead>
<tr>
<th>Diode</th>
<th>Before</th>
<th>After</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>( n )</td>
<td>( R_s )</td>
</tr>
<tr>
<td>1. 3 ( \mu ) dot</td>
<td>1.16</td>
<td>3.34</td>
</tr>
<tr>
<td>2. cross</td>
<td>1.12</td>
<td>1.15</td>
</tr>
<tr>
<td>3. &quot;</td>
<td>1.12</td>
<td>0.81</td>
</tr>
<tr>
<td>4. &quot;</td>
<td>1.11</td>
<td>1.67</td>
</tr>
<tr>
<td>5. &quot;</td>
<td>1.15</td>
<td>4.79</td>
</tr>
</tbody>
</table>

Table 2. GT8A497A Before and After 325°C Heat Stress (336.5 Hours)
Upon termination of the test, the diode bias voltage deviation was plotted on a much expanded scale as shown in figure 6. In this figure, time = zero denotes 15 minutes after the temperature had stabilized at 325°C. The 30 mA bias was applied and the voltage recorded. After 1.5 hours, diodes 3 and 5 show a significant voltage step followed by a gradual change. Diode 4, displayed a small initial step but a rather large total change.

At this time it appears that the bias voltage at temperature must be measured at a much lower current in order to show diode degradation. Experiments will be conducted to determine this current.

Curve tracer data before and after heat stress were also recorded; however, only diodes 3, 4 and 5 could be compared due to the failure of the whisker contacted diodes 1 and 2. Curve tracer data were not taken before heat stressing of the number 2 unbiased cross diode because the bias contact priority was given to the 3 μm dot diode. These data, shown in figure 7a-7g, visually display the changes that have occurred. No curve tracer $V_B$ data before heat stress are available for the specific number 2 cross diode. It is nevertheless assumed that the $V_B$ increase shown in figure 7g is real because the $V_B$ for all GT8A497 diodes is nearly the same before stress. Although by most standards these diodes are quite good, it is apparent that they are not as stable as the most stable phase I 83012-18 diodes. The differences noted must be examined in detail.

DELIVERY OF SAMPLE DIODES

Two lots of chips (10 each) from GT8A497A and GT8A499A have been delivered. A second portion of the 8A501 wafer is in process and should be ready by the end of December.

PLANS FOR NEXT MONTH

- Examine failures of GT8A497A
- Process second piece of 8A501
3\mu\text{ Diam. Life Test}

\text{DIODE (i)}
\begin{align*}
T &= 325^\circ C \\
I_{\text{DIODE}} &= 0.25\text{ mA}
\end{align*}

\text{VOLTAGE (VOLTS)}

\text{TIME (HOURS AFTER LOAD)}

Figure 1.
Figure 2.

3μ DIAM. LIFETEST

DIODE (2)
T = 325°C
I_{diode} = 0.25 mA

VOLTAGE (VOLTS)

TIME
(HOURS AFTER LOAD)

Figure 2.
CROSS LIFE TEST

DIODE (3)

T = 325°C
I_{diode} = 30 mA

VOLTAGE (VOLTS)

.50
.45
.40
.35
.30
.25
.20
.15
.10
.05
.00

50 100 150 200 250 300 350 400

TIME
(HOURS AFTER LOAD)

Figure 3.
CROSS LIFE TEST

DIODE (9)

$T = 325^\circ C$

$I_{D\text{ode}} = 30 \text{ mA}$

Figure 4.
Figure 5.
Figure 6. Diode Bias, Expanded Scale.
Before Heat Stress

Figure 7a.

Figure 7c.

Figure 7e.

Fwd. Bias
Center Trace
Horiz. 0.1V/Div
Vert. 0.01mA/Div

Rev. Bias
Upper Right
Horiz. 2V/Div
Vert. 0.01mA/Div

After Heat Stress

Figure 7b.

Figure 7d.

Figure 7f.

Figure 7g.

Figure 7. Curve Tracer Data GT8A497A.
Status Report No. 9

MILLIMETER WAVE MIXER DIODES - PHASE II

Contract period covered
1 December 1981 through 31 December 1981
P. O. No. SB-738203-LV3

A-2960

Submitted to
Hughes Aircraft Company
El Segundo, California 90245

by

Physical Sciences Division
Electromagnetics Laboratory
Engineering Experiment Station
Georgia Institute of Technology
Atlanta, Georgia 30332

Contracting through
Georgia Tech Research Institute
Georgia Institute of Technology
Atlanta, Georgia 30332

25 January 1982
INTRODUCTION

The past months activity has produced a second run from the Raytheon 8A501 wafer. Also some attention has been given to the GT8A497A diode failures previously reported. The net activity has been limited due to one staff member being on jury duty and the one week closing of Georgia Tech for the holidays.

DIODE FABRICATION

The second portion of wafer 8A501 (B) has yielded good diodes in terms of \( \eta \) and \( R_s \). A comparison of results obtained from the first run GT8A501A and this recent run is as follows.

<table>
<thead>
<tr>
<th>GT8A501A 3( \mu )m diameter</th>
<th>GT8A501B 3( \mu )m diameter</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \eta )</td>
<td>( R_s )</td>
</tr>
<tr>
<td>1.23</td>
<td>7.16( \Omega )</td>
</tr>
<tr>
<td>( \eta )</td>
<td>( R_s )</td>
</tr>
<tr>
<td>1.10</td>
<td>5.04( \Omega )</td>
</tr>
</tbody>
</table>

These data compare favorably with diode data obtained from runs GT8A497A and GT8A499A, which implies that all three of the Raytheon wafers are acceptable providing of course that the rf data also agree with the dc findings. To this date, Hughes has not supplied Georgia Tech with the rf results from the GT8A497A and GT8A499A runs. It is desirable, to have the rf confirmation before processing the remainder of the Gallium Arsenide. In the event that the rf results are negative, additional runs may be required and perhaps new GaAs wafers may be needed.

Photomicrographs of typical diodes from the three process runs are shown in figure one. One will note that the GT8A501B diodes have metal extending above the SiO\(_2\). This is the result of excessive resist etch back during the
plasma etch step. The evaporated metal is thus permitted to deposit on the slope of the etched oxide hole and therefore protrudes above the surface. Acceptable rf characteristics of this run may be negated by the additional parasitic capacitance due to this additional metal. However, diodes from this run will be submitted for rf tests as a matter of interest. Meanwhile, a new wafer section will be processed.

**DIODE FAILURE ANALYSIS**

The GT8A497A diodes subjected to the heat stress test previously reported have been examined for overall contact metal degradation of the type observed during phase I. Previous failures displayed a color change as well as a severely roughened surface. The recent diodes do not show any of these characteristics. The metal surfaces shown in the photomicrographs of figure 2 of both failed heat stressed cross diodes and unstressed diodes appear similar.

A series of short term heat stress tests are being planned to determine more closely when and at what temperature electronic failures occur. The results of these tests will be used to determine the test parameters to qualify the deliverable diodes.

**PLANS FOR NEXT MONTH**

- Conduct heat stress tests of diodes from GT8A499A and GT8A501B.
- Process additional 8A501 wafer.
Figure 1. Typical diodes yielding good dc characteristics. Submitted for rf tests. Mag = 26,000X

Figure 1b. GT8A499A

Send two copies of binding slip with volume.
Original slip must accompany volume returned for correction.

W.B.
SR 106 59

F-7-10 3/14
Figure 2a. GT8A497A Heat stressed metal contact surface 325°C for 336.5 Hrs. 70° angle Mag = 24,000X

Figure 2b. GT8497A unstressed metal contact surface 70° angle Mag = 24,000X

Figure 2. Surface roughness, heat stressed contact vs unstressed.
Status Report No. 12, 13, 16

MILLIMETER WAVE MIXER DIODES - PHASE II

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Physical Sciences Division
Electromagnetics Laboratory
Engineering Experiment Station
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Contracting through
Georgia Tech Research Institute
Georgia Institute of Technology
Atlanta, Georgia 30332

16 April 1982
INTRODUCTION

This status letter describes the program activity for the period 1 January 1982 - 31 March 1982. Apology is also submitted at this time for the tardiness in reporting the program progress. The planned diode life test activity for diode run GT8A501B has been completed. The results of these tests are included in this report appendix. Obtaining meaningful diode failure data has been hampered by catastrophic failure of some diodes during the high temperature stress test. These failures dictated additional tests in order to obtain a better data base. Three sets of five diodes each were required in order to develop a better feel for the test procedure.

In view of the fact that the program schedule was slipping while awaiting the rf test results from the previously delivered sample diodes; Bernie Walsh, was contacted to determine if it was desirable and prudent to proceed with processing the balance of the GaAs diode material. A decision based on past experience indicated that the sample diodes would most likely prove to be rf acceptable, and to proceed with the process would in fact be advisable.

Thus far two of the gallium arsenide wafers have been completed through the DC test map. Although many of the diodes satisfy the DC test specification, they are in general of poorer quality than sample runs produced from these same wafers. With the knowledge that better diodes have been produced from this material and the results showing that both full scale runs have been of inferior quality, it is desirable to proceed more slowly with the remaining 8A501 wafer. In the advent of total failure of this last wafer, some new GaAs material may have to be purchased or alternately some remaining pieces of phase I material may have to be substituted.

In light of the failure of the two wafers, a no cost program extension has been requested in order to complete the processing evaluation and qualification of additional GaAs materials.

HIGH TEMPERATURE STRESS TESTS

Three lots of five diodes each have been tested. Cross type diodes from the GT8A501B sample run were subjected to temperatures of 300°C and 325°C. A bias current of 30 mA was applied to each diode during the
test. The diode bias voltages at 0.10 mA were measured and the voltage drifts were plotted from time zero to termination of the test. All of the diodes were removed periodically from the heat station and the room temperature DC data; $\eta$, $R_s$ and $V_B$; were recorded. The test data are included in this report appendix. Because of the small test sample size (5 diodes), three repeat runs were required to establish some degree of confidence in the test procedure and the ensuing results. During these three runs several premature catastrophic diode failures occurred. It was felt that these failures were not representative of the true character of the diodes and their failure was caused by outside factors. Such catastrophic failures have been previously observed to be caused by static charge and power line glitches. Grounding of the test personnel and equipment appear to keep the static charge problem at a minimum.

The diodes produced thus far during phase II still do not appear as hardy as the phase I best diodes. The 8A501B data shown in this report also support this claim.

Following these tests, the titanium charge was removed from the E-beam evaporator and analyzed for contamination. A very slight trace of gold was found as a constituent. The titanium charge was changed and additional cross contamination shielding was provided around the E-gun crucible. Apparently the gold contamination comes from some spattering that can occur during the gold evaporation if the beam power level is excessive. A lower power level and slower evaporation of the gold were instituted for the first two whole wafer runs, GT8A497C and GT8A499B. High temperature tests of diodes from these latest runs have not commenced; however, some of the better diodes will be tested to note any improvement in high temperature performance.

PROCESSING DELIVERABLE MATERIAL

The diode processing proceeded very well and good diodes were anticipated from both wafers GT8A497C and GT8A499B. All of the process steps proceeded without difficulty; however, the dc test indicated that the diodes produced were of a poorer quality than expected. Poor ideality factor and high series resistance were the reasons for failure. The GT8A497C wafer was the worst of the two. The GT8A499B wafer has potentially a substantial number of diodes that are quite good. The
The diodes nearest the edge of the wafer for about 3-4 millimeters distance appear to be of fair quality. Additional testing of chips from these areas is required. Table one shows the diode ideality factor, series resistance and breakdown voltage obtained during the wafer mapping step for both wafers GT8A497C and GT8A499B.

The most obvious reason for poor diode quality is an improperly formed metal GaAs interface caused by contamination from some source. Investigation into this problem is certainly required before processing the remaining large wafer.

**PLANS FOR NEXT MONTH**

It is proposed to process a small portion of the remaining 8A501 wafer and/or pieces of remaining phase I material. The experiment that appears to be most useful in solving this problem is the following. Expose the wafer to UV light following completion of the photoresist process to reduce the quantity of nitrogen gas given off by the resist during evaporation of the titanium. Nitrogen and water vapor are normally released during exposure of the photoresist and are probably released during evaporation due to heating of the titanium to a white heat. This gas may contaminate the titanium metal before it is deposited in the diode windows. This phenomenon could explain why smaller wafer portions $6 \text{ mm}^2$ versus $20 \text{ mm}^2$ yielded better diodes since less resist implies less gas released. It is difficult to conclude other explanations because the diode process has been so repeatable throughout phase I and phase II prior to the recent large wafer runs.

**EXPERIMENTS**

At least three experiments are planned in an attempt to resolve the diode quality problem. A control sample consisting of only a small portion of a wafer will be metallized as normal. A second identically sized piece will be metallized along with a larger piece of dummy material, both of which have had all of the photoresist exposed to UV. A third piece will be processed as the second, without the additional UV exposure. The DC data will then be compared to determine the effectiveness of the modified procedure.
| Diode No. | Diode Dia = 3 μm | | | Diode Dia = 3 μm |
|---|---|---|---|---|---|---|
| 1 | 2.57 | 30.4 | 6-10V | 1 | 1.16 | 4.5 | 8.0 |
| 2 | 4.18 | 20.6 | Typical | 2 | 1.15 | 5.4 | 7.0 |
| 3 | 1.78 | 34.3 | | 3 | 1.17 | 5.4 | 7.0 |
| 4 | 1.47 | 35.8 | | 4 | 1.19 | 9.4 | 7.2 |
| 5 | 1.22 | 8.7 | | 5 | 1.16 | 5.8 | 7.5 |
| 6 | 2.00 | 35.5 | | 6 | 1.18 | 8.9 | 7.2 |
| 7 | 3.51 | 98.6 | | 7 | 1.20 | 8.8 | 7.2 |
| 8 | 8.15 | X | | 8 | 1.21 | 13.5 | 5.8 |
| 9 | | | | 9 | 1.18 | 7.5 | 7.0 |
| 10 | | | | 10 | 1.17 | 7.2 | 7.2 |
| 11 | | | | 11 | 1.18 | 7.8 | 6.5 |
| 12 | | | | 12 | 1.17 | 5.9 | 7.0 |
| 13 | | | | 13 | 1.16 | 5.3 | 9.0 |
| 14 | | | | 14 | 1.17 | 7.5 | 6.5 |
| 15 | | | | 15 | 1.26 | 9.5 | 7.0 |
| 16 | | | | 16 | 1.18 | 5.7 | 6.8 |

Table 1. DC Test Results - Wafers GT8A497C and GT8A499B.
APPENDIX

The data presented in this appendix is intended to show that the test procedure developed for the cross diodes does demonstrate failure of the GT8A501B diodes at 300°C and 325°C temperatures. Test data were recorded and plotted for the following:

- Diode forward voltage at 0.10 mA bias current at the test temperature.
- Ideality factor at room temperature
- Series resistance at room temperature
- Reverse breakdown at room temperature.

Some of the rather non-smooth plotted data is due in part to the "operator variable" of data collection. The test necessitated removing the diodes from the heat station for each test; therefore, some temperature cycling was involved which may have affected the tests in some manner. For instance, some of the catastrophic failures observed in the $V_B$ measurements shown in figure 10 may be attributed to temperature cycling. However, most of this type of failures has been attributed to static burnout. Following the second test run, the test person was grounded and the test repeated with five new diodes. There were no "premature" catastrophic failures attributed to static discharge in the run. The $V_B$'s degraded with time as one would expect.

CONCLUSIONS

Some of the diodes from the GT8A501B run when subjected to temperatures of 300°C - 325°C begin changing dc characteristics immediately. At 325°C two of the diodes (7,10) are degraded enough to be classified as failures after 4 hours. The remainder survived for approximately 29 hours. Ignoring the second test run (diodes 11-15) because of the many catastrophic failures, one can determine from the data that the third run (diodes 16-20) is most representative of the high temperature character of the GT8A501B diodes, where three of the five diodes survived in excess of 75 hrs. The two failures (diodes 18-19) occurred over a weekend and a power failure was noted during this time. The observed degradation could be attributed to this cause. Also one can conclude that the uniformity of failure that one might expect from most of the diodes is displayed in the data on the last test run (diodes, 16-20). More tests of this type will be performed once the diode process problems are solved.
APPENDIX

Status Letter No. 12, 13, 16
Figure 1. Diode Forward Voltage Drift at $I_F = 0.01 \text{ mA}$.
GT8A501B (6-10), 325°C Test.
Figure 2. Diode Forward Voltage Drift at $I_F = 0.01$ mA.
GT8A501B (11-15), 300°C Test.
Figure 3. Diode Forward Voltage Drift at $I_F = 0.01 \text{ mA}$.
GTBA501B (16-20), 300°C Test.
Figure 4. Ideality Factor vs Time. GT8A501B (6-10) 325°C Test.
Figure 5. Ideality Factor vs. Time.
GT8A501B (11-15), 300°C Test.
Figure 6. Ideality Factor vs. Time.
GT8A501B (16-20), 300°C Test.
Figure 7. Series Resistance vs. Time.
GT8A501B (6-10), 325°C Test.
Figure 8. Series Resistance vs. Time.
GT8A501B (11-15), 300°C Test.
Figure 9. Series Resistance vs. Time.
GT8A501B (16-20), 300°C Test.
**Figure 10a. V_B Data**

- **DIODE NO:** GT8A501B - 6
- **325°C, 30 mA**
- **% GROUNDSTRAP**

- **For All of Figure 10.**
  - Upper Trace Horiz 2V/DIV
  - Vert 0.01 mA/DIV
  - Lower Left Horiz 0.1V/DIV
  - Vert 0.01 mA/DIV
  - Lower Right Horiz 0.1V/DIV
  - Vert 0.10 mA/DIV
Figure 10b. $V_B$ Data
Figure 10c. $V_B$ Data
**Figure 10d. \( V_B \) Data**

**Diode No:** GT8A501B-9

325°C, 30 mA

W/0 GROUNDSTRAP
DIODE NO: GT8A501B-10
325°C, 30 mA
W/0 GROUNDSTRAP

Figure 10e. $V_B$ Data
Figure 10f. $V_B$ Data
Figure 10g. V Data
Figure 10h. $V_B$ Data
Figure 10f. $V_B$ Data
Figure 10j. $V_B$ Data
Diode No: GTBA501B-17
300°C, 30 mA
W/Groundstrap

Figure 10L. $V_B$ Data
Figure 10m. $V_B$ Data
Figure 10n. $V_B$ Data
DIODE NO. GTBA501B-20
300°C, 30mA
W/GROUNDSTRAP

Figure 10a. $V_B$ Data
Status Report No. 19/20

MILLIMETER WAVE MIXER DIODES - PHASE II

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El Segundo, California 90245

by

Physical Sciences Division
Electromagnetics Laboratory
Engineering Experiment Station
Atlanta, Georgia 30332

Contracting through
Georgia Tech Research Institute
Georgia Institute of Technology
Atlanta, Georgia 30332
INTRODUCTION

The past months activity included completion of the high temperature test of diodes from the GT8A499B run and completion of the experiment defined in last month's report relating to the poor quality of diodes obtained from large area wafers.

HIGH TEMPERATURE STRESS TEST

The high temperature test of diodes from the large wafer GT8A499B have been completed with great satisfaction. The high temperature stability characteristics of these diodes are as good or better than the best phase I diodes. These results indicate that the high temperature instability previously reported on the wafer evaluation runs GT8A497, 499A and 5018 were in fact due to the suspected gold contamination in the titanium charge.

Five diodes from the most recent large wafer run GT8A499B were subjected to temperatures of 300°C to 350°C for a total of 473 hours. Following 233 hours the dc data showed little change under both forward and reverse bias conditions. The temperature was then increased to 325°C. After 144 hours at this new temperature (377 hrs total), all but the number two diode (which shorted) showed little further change; in fact, a slight improvement in ideality factor was observed on diodes four and five. The number one diode was lost in a crack in the screen-room subflooring. Number two shorted catastrophically (possibly due to handling). The test temperature was then increased to 350°C. After approximately 30 hours (410 hours total), a decided upward drift in ideality factor was observed which continued for the remaining 63 hours (473 hours total) of the test. The reverse breakdown characteristics changed somewhat from their initial values but remain quite stable throughout the test. Figures one and two show the plotted ideality and $V_B$ data for the high temperature test.

LARGE WAFER EXPERIMENTS

The large wafer "piggyback" experiment has been completed as initially defined in last month's report. To reiterate briefly, one (6.5 x 8.5 mm) piece of wafer 8A12 remaining from phase one was
processed up to the Schottky metallization step. The wafer was divided into 3 equal parts, GT8A12-3X(-1), (-2) & (-3). The first portion (-1) was processed to diode completion using the established process. The remaining two portions, (-2) and (-3), were mounted piggyback, each on a large silicon wafer which had been processed in normal fashion. One of the large wafers (-3) was additionally exposed to the UV light source to drive off gases and water vapor. The end result of the experiment was three identical small wafer portions metallized under three different conditions, where the resist surface area and subsequent UV exposure treatment were variables. The results of the experiment show that the small wafer (-1) metallized independently yielded good diodes; the (-2) portion which was not UV exposed and the (-3) portion which was exposed to UV both yielded diodes of poor quality. These results were not as expected. The UV exposed wafer was expected to yield good diodes similar to the (-1) portion, if the resist outgassing was contributing to the process problem. The data for this series of experiments are shown in table one.

<table>
<thead>
<tr>
<th>Diode Dia.</th>
<th>Standard Small Wafer</th>
<th>Standard Piggyback</th>
<th>UV Exposed Piggyback</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>n</td>
<td>R_s</td>
<td>n</td>
</tr>
<tr>
<td>1.5 µm</td>
<td>1.15</td>
<td>12.54</td>
<td>1.19</td>
</tr>
<tr>
<td>2.0 µm</td>
<td>1.15</td>
<td>6.33</td>
<td>1.20</td>
</tr>
<tr>
<td>3.0 µm</td>
<td>1.13</td>
<td>4.29</td>
<td>1.20</td>
</tr>
<tr>
<td>5.0 µm</td>
<td>1.10</td>
<td>4.12</td>
<td>1.17</td>
</tr>
<tr>
<td>Cross</td>
<td>1.07</td>
<td>2.68</td>
<td>1.10</td>
</tr>
</tbody>
</table>

Table 1. DC Test Data GT8A123X.
This problem is most perplexing and requires more testing where the large wafer is UV exposed for a much longer period, one or two minutes, instead of the 15 seconds exposure that was given. The basis for this reasoning is that during insertion of the wafer sample it was observed that the vacuum system pressure increased approximately one third order of magnitude when the wafer was exposed to the melt. This effect does demonstrate outgassing of the resist (or perhaps the substrate holder) due to heating by the titanium melt. These results also suggest that the wafer preheat or deposition rate may have to be adjusted to the outgassing condition of the large wafer.

PLANS FOR NEXT MONTH

Two experiments are being defined utilizing the piggyback technique, where the wafer preheat and deposition rates are non-standard.

1. Increase the preheat time until the system pressure stabilizes, then evaporate the titanium slowly.
2. Repeat the above but increase the titanium evaporation rate.

All other things being equal, the second experiment should by virtue of the higher temperature burst more gas but permit less time for reaction of the titanium with the contaminating gases.
Figure 1. Ideality Factor vs Time at 300°C, 325°C, and 350°C.
Temp increased to 325°C

Scale
Horiz = 1V/Div.
Vert = 0.01 mA/Div

Figure 2a. Breakdown Data GT8A499B After 233 Hours at 300°C.
Temp increased to 350°C

Scale

Horiz = 1V/Div
Vert = 0.01 mA/Div

Figure 2B. Breakdown Data GT8A499B After 144 Hrs. at 325°C (377 Hours Total).
Figure 2c. Breakdown Data GT8A499B After 96 Hours at 350°C (473 Hours Total).

Scale
Horiz = 1V/Div
Vert. = 0.0lmA/Div
Status Report No. 21/24

MILLIMETER WAVE MIXER DIODES - PHASE II

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Georgia Institute of Technology
Atlanta, Georgia 30332
INTRODUCTION

This report summarizes the program activity from June thru October. The level of effort was reduced due to funding and temporary personnel shifts. A redefined program schedule and request for additional funding has been completed. The technical effort has proceeded cautiously due to the difficulty in resolving the large wafer processing problem.

TECHNICAL EFFORT

GaAs MATERIALS

A purchase order for two GaAs wafers has been submitted to Raytheon. The bid package was rejected by Georgia Tech because the materials offered were inventory that did not meet the specified doping density and epitaxial layer thickness. Also we were informed that the GaAs materials operation had been transferred to their new facility. A new quote has been requested but not received. Unofficially we have been informed that the new price per wafer will be $3,000. Perhaps this purchase can be circumvented provided the remaining large piece of Phase I material provides in time the required diode quality and quantity. A second alternative is to purchase from Raytheon the off the shelf stock wafers and thin the epilayer as was done in Phase I. This second alternative would provide material much sooner.

DIODE PROCESS

Wafer GT8A501 was processed through the SiO₂ etch step. The major portion was placed on hold until further assessment of the large wafer processing problem could be accomplished. Two small portions (2 x 3 mm) of this wafer were processed through the metallization process utilizing the post development UV exposure "piggyback" method described in status letter 19/20. The large remaining portion was completed
following the "piggyback" experiment. The dc characteristics of the "piggyback" diodes are quite dissimilar to those observed on the previous GT8A12-3X experiment. The recent diodes did demonstrate improved ideality factor but higher series resistance. Most important, the UV exposed wafer demonstrated better ideality factor than the non UV exposed wafer. These comparative data are shown in table I.

<table>
<thead>
<tr>
<th>Diode Dia.</th>
<th>Non UV Exp. Piggyback</th>
<th>UV Exp. Piggyback</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$n$</td>
<td>$R_s^*$</td>
</tr>
<tr>
<td>GT8A12-3X</td>
<td>1.5</td>
<td>1.19</td>
</tr>
<tr>
<td></td>
<td>2.0</td>
<td>1.20</td>
</tr>
<tr>
<td></td>
<td>3.0</td>
<td>1.20</td>
</tr>
<tr>
<td></td>
<td>5.0</td>
<td>1.17</td>
</tr>
</tbody>
</table>

| GT8A501C-(1-2) | 1.5 | 1.14 | 20  | 1.13 | 36 |
|                | 2.0 | 1.15 | 14  | 1.10 | 10 |
|                | 3.0 | 1.13 | 6.0 | 1.09 | 6.5 |
|                | 5.0 | 1.10 | 4.0 | 1.08 | 4.0 |

*includes 1 ohm test setup resistance.

The high series resistance associated with these latest GT8A501 C-1 & C2 runs is thought to be associated with insufficient pre-Schottky GaAs etch. This characteristics has been observed in the past. The low ideality factor on the UV exposed wafer was encouraging. In addition, discovery and solving of a ground-shielding problem in the test setup resulted in obtaining better data on the previous GT8A499 wafer. Unfortunately too few diode chips are available from this run.
Following these rather encouraging experiments it was decided to process the large portion of wafer GT8A501C3.

The diodes produced from this run are quite similar to the previous runs GT8A501C1 & 2. The ideality factors are good for the 5, 3 & 2 μm diodes, and quite poor for the 1.5 μm diodes. Also the series resistances are slightly high when compared to previous good runs. The poor 1.5 μm diodes are a rather new observance. Once again the pre Schottky etch is suspect. One explanation is that the etch does not enter the small window as quickly as the large windows due possibly to bubble formation; therefore etching commences later and insufficient material is removed, giving rise to both poor ideality and higher series resistance. The dc data for wafer GT8A501C3 is contained in table II and figures 1 and 2.

### Table II

<table>
<thead>
<tr>
<th>Diode dia. μm</th>
<th>n</th>
<th>Rs Ω*</th>
</tr>
</thead>
<tbody>
<tr>
<td>GT8A501C3</td>
<td>1.5</td>
<td>1.29</td>
</tr>
<tr>
<td>Large wafer</td>
<td>2.0</td>
<td>1.14</td>
</tr>
<tr>
<td>V_B 10-11V</td>
<td>3.0</td>
<td>1.11</td>
</tr>
<tr>
<td></td>
<td>5.0</td>
<td>1.10</td>
</tr>
</tbody>
</table>

*includes 1 ohm test setup resistance.

The reverse breakdown characteristic of the diodes are very good, in fact better than previous runs.

This series resistance problem can likely be avoided by increasing slightly the pre schottky etch time. Selected diodes from wafer GT8A501C3 will be cross-sectioned to attempt to evaluate the depth of the pre schottky etch. The cross sectioned diodes will be examined on the SEM, comparing these diodes with previous runs.
PLANS FOR NEXT MONTHS

- evaluate pre Schottky etch depth
- rf test chips from wafer GT8A501C3 and compare to Phase I diodes
- process one remaining large piece of Phase I material
- select wafer for deliverable diodes.
Figure 1. Forward Characteristics GT8A501C3
Diode Dia. L to R 5.0, 3.0, 2.0, 1.5 μm.

Figure 2. Reverse Breakdown. GT8A501C3.
Del No. 25

Status Report No. 25

MILLIMETER WAVE MIXER DIODES - PHASE II

Contract period covered
31 October 1982 through 30 November 1982
P. O. No. S8-738203-LV3

A-2960

Submitted to
Hughes Aircraft Company
El Segundo, California  90245

by

Physical Sciences Division
Electromagnetics Laboratory
Engineering Experiment Station
Atlanta, Georgia  30332

Contracting through
Georgia Tech Research Institute
Georgia Institute of Technology
Atlanta, Georgia 30332
INTRODUCTION

This past months program activity has included processing of the remaining large wafer, GT83012A, and comparing the diode dc characteristics with GT8A501C3. The purpose of this task was to determine which of the two wafers would provide the deliverable diodes. The comparison shows the GT83012A wafer to be unacceptable due to high $R_s$. Therefore, wafer GT8A501C3 will be used to provide the deliverable diodes.

The dc, rf and heat stress tests of diodes from this wafer are underway.

GENERAL

Diode Processing

Wafer GT83012A has been processed. The diodes are of unacceptable quality due in part to high $R_s$. The ideality factor is also somewhat high for the smaller diodes. This wafer did however have a lower doping concentration ($8 \times 10^{16}$) than specified ($1.1 \times 10^{17}$) which would emphasize the $R_s$. This wafer required a pre-process modification of the epitaxial layer thickness. The layer was thinned from 4.8 $\mu$m to 2.0 $\mu$m utilizing the $6\text{HPO}_4\cdot2\text{H}_2\text{O} : 100\text{DIH}_2\text{O}$ GaAs etch. A previous run processed from this material did also display slightly high $R_s$. Perhaps the actual thickness of the layer is not known well enough to predict the proper etch time; therefore excess epi remained. Table one shows the typical diode dc characteristics obtained from the GT83012A run.
Table I

<table>
<thead>
<tr>
<th>Wafer</th>
<th>Diode Dia µm</th>
<th>n</th>
<th>Rs*</th>
</tr>
</thead>
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<tr>
<td>GT83012A</td>
<td>1.5</td>
<td>1.18</td>
<td>32.84</td>
</tr>
<tr>
<td></td>
<td>2.0</td>
<td>1.14</td>
<td>18.43</td>
</tr>
<tr>
<td></td>
<td>3.0</td>
<td>1.11</td>
<td>8.76</td>
</tr>
<tr>
<td></td>
<td>5.0</td>
<td>1.08</td>
<td>5.84</td>
</tr>
<tr>
<td>cross</td>
<td>1.07</td>
<td>1.70</td>
<td></td>
</tr>
</tbody>
</table>

*Includes 1 ohm setup resistance

Heat Stress Tests GT8A501C3

Five diodes from this run were subjected to the stress test. Three of the diodes were inadvertently burned out partway thru the test due to grounding of the negative diode lead. One of the remaining two diodes (No. 19) may have suffered some transient damage, if one considers the data shown in figure 1. Three new diodes were mounted, replacing the shorted diodes. These three diodes and No. 20 displayed normal degradation as time progressed. The ideality factor versus time was plotted and is shown in figure one. A rapid upward trend in the factor indicates diode degradation. The diodes were heat stressed at two temperatures 330°C and 350°C. Diode degradation occurred near these temperatures during previous runs. Diodes 19 and 20 ran for 344 hours at 330°C. Number 19 was slowly changing with time. The temperature was increased to 350°C. After 9 hours at this temperature a decided change was noted, especially on diode number 20, indicating imminent failure of these two diodes. Diodes 23, 24 and 25 ran for 167 hours at 330°C at which time the temperature was increased to 350°C. Diode 23 ran an
additional 93 hours and remained stable. Number 24 ran 53 hours before degrading. Number 25 changed almost immediately. These results appear quite satisfactory, considering that the diodes have been temperature cycled from room to the test temperature a considerable number of times, 37 cycles for diodes 19 and 20 and 23 cycles for diodes 23, 24 and 25. Further testing of new diodes will be conducted starting at 350°C.

**Etch Depth Experiment**

The etch depth comparison experiment noted in the last report has been completed on the GT8A501C3 run. The result does not reveal anything significant other than confirming that the pre Schottky etch depth is near the desired 500Å value. The SEM data of 3 μm and 1.5 μm diode areas are shown in figure 2. Figure 3 shows the step profile of 5 μm and 2 μm diode areas. The 1.5 μm diode area could not be profiled due to the size of the profiler stylus.

**RF Test**

Four diodes have been mounted and contacted in the Hughes sharpless type package. Diode noise figure measurements will be conducted on two diodes from the best diode run (GT8A16-17) produced during phase one. These noise figure results will be compared to those obtained from the GT8A501C3 run. DC data for each diode will be taken prior to and following the rf test.

**PLANS FOR NEXT MONTH**

- Continue final testing of GT8A501C3 deliverables
- Prepare for shipment of the first diode lot.
Figure 1. GT8A501C3 Heat Stress Results.
Figure 2. SEM Data Showing Etched Diode Areas with Metallization Removed.

Figure 3. Step Profile Showing pre-Schottky Etch Depth.
Status Report No. 26

MILLIMETER WAVE MIXER DIODES - PHASE II

Contract period covered
30 November 1982 through 31 December 1982
P.O. No. S8-738203-LV3

A-2960

Submitted to
Hughes Aircraft Company
El Segundo, California 90245

by

Physical Sciences Division
Electromagnetics Laboratory
Engineering Experiment Station
Atlanta, Georgia 30332

Contracting through
Georgia Tech Research Institute
Georgia Institute of Technology
Atlanta, Georgia 30332
INTRODUCTION

The program activity for the past month has included beginning the final dc testing of the deliverable diode lot GT8A501C3 and completion of the initial rf tests. These tasks are proceeding favorably. The life tests were halted for the holidays but are to continue until the end of January. A no cost one month time extension is also being considered.

DIODE TESTS

The diode dc tests indicate a very good diode yield. Three hundred diodes have been tested. Thus far only four chips were rejected due to poor dc characteristics. Five to ten percent of the total wafer will be rejected for mechanical reasons. These favorable results have prompted a request to Hughes for quality control on site inspection. This initial inspection will help to clear up any unforeseen problems preparatory to shipment of the diodes to Hughes.

RF TESTS

Four of Georgia Tech's mixer diodes were mounted in wafer assemblies and tested for RF characteristics. Two of the diodes were from an earlier batch (GT8A16-17) and two were from the new batch (GT8A501C3). The three micron diameter Schottky diodes were used for all four measurements.

Measurements of the dc characteristics indicated ideality factors of 1.11 and resistances of four to six ohms. A superheterodyne receiver was set up as shown in Figure 1. Several measurements were performed.
using different LO and IF frequencies while the RF frequency was always close to 60 GHz. A summary of the measurements is given in Table I. These measurements indicate that the new diodes are as good or better than the old batch of diodes.

**SCHEDULE**

A request for a one month no cost time extension is being considered. This additional amount of time should allow completion of the program.

**PLANS FOR NEXT MONTH**

- continue final diode tests
- receive inspection, correct any deficiencies and prepare for diode delivery.
Figure 1. Diagram of Noise Figure Test Set-up.
<table>
<thead>
<tr>
<th>Frequency (GHz)</th>
<th>Mixer Noise Figure (dB)</th>
<th>Diode #</th>
<th>Batch #</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>11</td>
<td>GT8A16-17</td>
</tr>
<tr>
<td></td>
<td></td>
<td>12</td>
<td>GT8A16-17</td>
</tr>
<tr>
<td></td>
<td></td>
<td>21</td>
<td>GT8A501C3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>22</td>
<td>GT8A501C3</td>
</tr>
<tr>
<td>LO</td>
<td>IF</td>
<td>RF</td>
<td>(DSB)</td>
</tr>
<tr>
<td>----------------</td>
<td>-------------------------</td>
<td>---------</td>
<td>---------</td>
</tr>
<tr>
<td>56</td>
<td>0.5 - 1.0</td>
<td>55-56</td>
<td>3.8</td>
</tr>
<tr>
<td>56</td>
<td>1.5 - 3.0</td>
<td>53-59</td>
<td>4.8</td>
</tr>
<tr>
<td>45</td>
<td>7.5 -10.0</td>
<td>52.5-55</td>
<td>6.8</td>
</tr>
<tr>
<td>45</td>
<td>14.0 -16.0</td>
<td>59 61</td>
<td>6.8</td>
</tr>
</tbody>
</table>

*Cut off frequency for the waveguide used is 39.863 GHz*

1st two measurements were DSB (56 GHz LO)
2nd two measurements were SSB (45 GHz LO)
FINAL REPORT
PROJECT NO. A-2960

MILLIMETER WAVE MIXER DIODE
Phase II

By
G. N. Hill

Prepared for
HUGHES AIRCRAFT COMPANY
SPACE AND COMMUNICATIONS GROUP
EL SEGUNDO, CALIFORNIA

Under
P. O. No. S8-738203-LV3

Contract Period covered 16 April 1981 through 28 February 1983

28 February 1983

GEORGIA INSTITUTE OF TECHNOLOGY
A Unit of the University System of Georgia
Engineering Experiment Station
Atlanta, Georgia 30332
FINAL REPORT

MILLIMETER WAVE MIXER DIODE PHASE II

P.O. NO. S8-738203-LV3

Contract period covered
16 April 1981 through 28 February 1983

A-2960

Submitted to
Hughes Aircraft Company
Space and Communications Group
El segundo, California

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Physical Sciences Division
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Georgia Institute of Technology
Atlanta, Georgia 30332

Contracting through
Georgia Tech Research Institute
Georgia Institute of Technology
Atlanta, Georgia 30332

Prepared by
G.N. Hill
28 February 1983
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<thead>
<tr>
<th>TABLE OF CONTENTS</th>
<th>PAGE</th>
</tr>
</thead>
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<td>General Summary</td>
<td>1</td>
</tr>
<tr>
<td>Program Goals</td>
<td>2</td>
</tr>
<tr>
<td>Specifications</td>
<td>2</td>
</tr>
<tr>
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<td>2</td>
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<td>3</td>
</tr>
<tr>
<td>E-Beam Evaporator</td>
<td>3</td>
</tr>
<tr>
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<td>9</td>
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<td>11</td>
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<td>18</td>
</tr>
<tr>
<td>RF Test</td>
<td>24</td>
</tr>
<tr>
<td>APPENDIX</td>
<td>35</td>
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</tbody>
</table>
INTRODUCTION

This final report is a summary of the Millimeter Wave Mixer Diode program, Phase II. The purpose and key feature of this project was to produce from one gallium arsenide epitaxial wafer, one large lot of diodes (approximately 2000) displaying extremely similar electronic characteristics. These diodes were to be low noise at or near frequencies of 60 GHz and be resistant to failure under bias conditions following several hours exposure to temperatures approaching 350°C.

The diode fabrication recipe was established during a first phase development program at Georgia Tech. Upon completion of the first phase, necessary process improvements and equipment modifications were revealed. These process refinements were completed during the course of this phase II program.

General Summary

This report is intended to provide an overview of the phase II program. Many of the details are contained in the monthly status reports. Additional information may also be obtained from the phase I program reports under P.O. S8-712165-LV3.

The program was successfully completed in spite of delays and problems requiring substantial additional process experimentation. A high device yield has been obtained and all of the diode specifications have been met by a wide margin. 1339 good diode chips were produced, 1289 were delivered. Fifty chips were used for various tests. In addition, 500 chips from an alternate run were delivered for developmental use.

The process instructions and process run sheet of the deliverable lot GT8A501C3 are included in the Appendix of this
Program Goals

The major goal of this program was to produce gallium arsenide diodes of high quality and reliability. A second and very important goal was to successfully transfer from phase I, the process recipe to produce these diodes in quantity and similarity.

Specifications

Physical

- Chip size, 0.015 inches square, .002 inches thick
- A matrix "honeycomb" diode array insulated with SiO₂, consisting of four quadrants each of different diode diameter, 1.5, 2.0, 3.0 and 5.0 microns. Also included a chip orientation mark (cross).
- Anode contact metal of gold on platinum over titanium on gallium arsenide
- Cathode contact of gold on platinum over titanium, over nickel and gold/germanium on gallium arsenide.

Electrical

- \( n < 1.2 \)
- \( R_s < 7 \) ohms
- \( V_b > 3 \) volts
- \( f_c > 2 \) THz

Equipment Modification

In the interest of improved process control and testing, modifications were made to both the E beam evaporator and the SiO₂ deposition system. Improved dc testing was accomplished
through the use of a 6 decade constant current source.

**SiO\textsubscript{2} Deposition System**

The SiO\textsubscript{2} deposition system was modified to improve the deposition uniformity. The modification was completed and excellent uniformity was obtained over 1.22 in\textsuperscript{2}. The modification required complete rebuilding of the heated stage and deposition chamber. The old system used a stationary temperature controlled heated platen enclosed by a glass chamber having a volume of 350cc. The new system consists of a rotating temperature controlled heated platen enclosed by a similar but larger (600cc) chamber. A positive pressure vent system was also incorporated.

The growth rate was established at 702A per minute; 7.12 minutes being required for 5000 A.

**E-Beam Evaporator**

The E beam system shutter actuator assembly was changed to a bellows type, having a travel of 0.63 inches. The previous actuator traveled only 0.090 inches and would occasionally hang up during operation. The new assembly was especially designed to provide positive shutter movement. Additional cross contamination shielding was also employed. Tantalum shields were placed between the E-gun crucibles, and a funnel shield was positioned above the hearth such that any metal spattering would be contained.

A system pressure of $1 \times 10^{-10}$ Torr was maintained in the main chamber during idle conditions.

**Constant Current Test Circuit**

Parametric data required on mixer diodes includes diode voltage ($V_d$) at eight different diode current levels ranging from 10 nanoamperes to 10 milliamperes. Diode voltage measurements
Figure 1. Schematic Diagram - Constant Current Source.
\[ I_2 = \frac{V_1 - V_{BE}}{R_1} \]

and is stable provided \( V_1, V_{BE} \) and \( R_1 \) (which are all independent of the load) do not change.

A LM 394 supermatch transistor pair is used for \( Q_1 \) and \( Q_2 \) transistors. Current levels are selected with a dual wafer rotary switch which connects one of eight \( R_1 \) resistors and one of four \( R_2 \) emitter resistors or a direct circuit from the emitter of \( Q_2 \) to ground.

\( R_2 \) emitter resistors are used for the low current settings. When connected, the potential across \( R_2 \) is the difference between the base emitter voltages of \( Q_1 \) and \( Q_2 \) given by
\[ R_2 I_{E2} = V_{BE1} - V_{BE2}. \]
Since \( I_{E3} = I_2 \), the value of \( R_2 \) needed to set a current level of \( I_0 \) can be found by
\[ R_2 = \frac{I_1}{I_2} (V_{BE1} - V_{BE2}), \]
but
\[ V_{BE} = \frac{KT}{q} \ln \frac{I_E}{J_{SAE}}, \]
and for matched transistors
\[ J_{SAE1} = J_{SAE2}, \]  
so
\[ R_2 = \frac{KT}{q} \ln \frac{I_{E1}}{I_{E2}} \text{ or } R_2 = \frac{26mV}{I_0} \ln \frac{I_1}{I_2} \text{ at room temperature.} \]

Multi-turn trim pots allow precise adjustment of the constant current which is sensed by measuring the voltage across a 1000 ohm (0.1%) resistor.
Dual binding posts were used to connect the diode test fixture to the current source. Curve tracer and DVM connections were also made with dual binding posts. The diode under test was switched from the current source to the curve tracer in order to facilitate making initial diode contact and measuring breakdown voltage.

Photomask

The photomask was modified for the phase two work. These changes were required for two reasons. One, Hughes desired a larger capacitance diode in quadrant three, hence a change from 2.5 μm diameter to 5.0 μm diameter, and two, addition of channels bordering the chip scribe streets to facilitate scribing and prevent damage to the SiO₂ in the diode field. The diode chip geometry is shown in figure 2. This change in mask design delayed the program for several months because the mask vendor failed on several occasions to provide the correct geometry.

Diode Fabrication

Gallium Arsenide Materials

The gallium arsenide materials parameters were established during phase I and upon completion of the program three GaAs wafers were special ordered from Raytheon Research Laboratory, Waltham, Massachusetts. The wafer properties are briefly described in table 1, and more fully in the appendix. All of the GaAs material was found to be of excellent quality and uniformity.
Dimensions in inches except where noted

**Figure 2, Chip Geometry Repeated .015 IN.C.C.**
<table>
<thead>
<tr>
<th>Substrate</th>
<th>8A497</th>
<th>8A499</th>
<th>8A501</th>
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<tbody>
<tr>
<td>Size cm$^2$</td>
<td>6.16</td>
<td>6.16</td>
<td>6.44</td>
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<tr>
<td>carrier concentration</td>
<td>1.8</td>
<td>1.8</td>
<td>1.8</td>
</tr>
<tr>
<td>$\times 10^{18}$ cm$^{-3}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dopant</td>
<td>Te</td>
<td>Te</td>
<td>Te</td>
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**Epitaxial Layers**

<table>
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<tr>
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<tr>
<td>carrier concentration</td>
<td>&gt;2</td>
</tr>
<tr>
<td>$\times 10^{18}$ cm$^{-3}$</td>
<td></td>
</tr>
<tr>
<td>thickness µm</td>
<td>5</td>
</tr>
<tr>
<td>dopant</td>
<td>Si</td>
</tr>
</tbody>
</table>

**Active**

| thickness µm | .26 |
| carrier concentration | 1.0 |
| $\times 10^{16}$ cm$^{-3}$ | |

Table 1. Gallium Arsenide Epitaxial Material Properties.

**Diode Samples**

Sample diodes were fabricated from a small portion of each wafer. Dc and high temperature step stress tests were conducted on each lot in order to determine the best wafer with which to produce the deliverable diode lot. Rf testing of these sample diodes was also desirable; however, due to loss of a key person at Hughes these test did not take place. Tests were conducted at Georgia Tech at a later date on the deliverable lot using a
Hughes supplied mixer and IF amplifier.

Typical dc data for sample diodes from the three wafers are shown in Table 2. These data indicated that all of the wafers were of acceptable quality. Prior test experience obtained during phase I demonstrated that good ideality factors and $R_s$ applied good $R_f$ performance.

<table>
<thead>
<tr>
<th>Wafer Run No.</th>
<th>Diode Dia. μm</th>
<th>$\eta$</th>
<th>$R_s^*$</th>
</tr>
</thead>
<tbody>
<tr>
<td>GT8A497A</td>
<td>1.5</td>
<td>1.13</td>
<td>11.31</td>
</tr>
<tr>
<td></td>
<td>2.0</td>
<td>1.12</td>
<td>7.13</td>
</tr>
<tr>
<td></td>
<td>3.0</td>
<td>1.11</td>
<td>4.51</td>
</tr>
<tr>
<td></td>
<td>5.0</td>
<td>1.11</td>
<td>2.85</td>
</tr>
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<td>GT8A499A</td>
<td>1.5</td>
<td>1.17</td>
<td>10.31</td>
</tr>
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<td></td>
<td>2.0</td>
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<td>7.21</td>
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<td>1.15</td>
<td>4.52</td>
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<td></td>
<td>5.0</td>
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<td>2.62</td>
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<tr>
<td>GT8A501B</td>
<td>1.5</td>
<td>1.15</td>
<td>20.0</td>
</tr>
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<td></td>
<td>2.0</td>
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<td>11.91</td>
</tr>
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<td></td>
<td>3.0</td>
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</tr>
<tr>
<td></td>
<td>5.0</td>
<td>1.10</td>
<td>3.45</td>
</tr>
</tbody>
</table>

Table 2. Sample Diode DC Test Results

*Includes 1 ohm test setup resistance.
Deliverable Wafer Process

Wafer runs GT8A497C and GT8A499B

The remaining portion of each wafer was processed following the sample runs. The diode processing proceeded very well and good diodes were anticipated from both wafers GT8A497C and GT8A499B. All of the process steps proceeded in normal fashion; the dc test indicated that the diodes produced were of a poorer quality than expected. Poor ideality factor and high series resistance were the reasons for rejection. The GT8A497C wafer was the worst of the two. The GT8A499B wafer had potentially a substantial number of good diodes. The diodes nearest the edge of the wafer for about 3-4 millimeters distance appeared to be of fair quality. Tables 3a and 3b show the diode ideality factor, series resistance and breakdown voltage obtained during the wafer mapping step for both wafers GT8A497C and GT8A499B.

Diode Dia = 3 \mu m

<table>
<thead>
<tr>
<th>Diode No.</th>
<th>$\eta$</th>
<th>$R_s$</th>
<th>$V_b$ @ 10 \mu A</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2.57</td>
<td>30.4</td>
<td>6-10V</td>
</tr>
<tr>
<td>2</td>
<td>4.18</td>
<td>20.6</td>
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</tr>
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<td>8.15</td>
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</tbody>
</table>

Table 3a. GT8A497C Large wafer dc Test Results
*includes 1 ohm test setup resistance.
Diode Dia = 3 \mu m

<table>
<thead>
<tr>
<th>Diode No.</th>
<th>( n )</th>
<th>( R_s^* )</th>
<th>( V_B ) @ 10 ( \mu A )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1.16</td>
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<td>7.0</td>
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<td>7.2</td>
<td>7.2</td>
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</table>

Table 3b. GT8A499B Large Wafer dc Test Results.

*includes 1 ohm test setup resistance.

It was felt that the most obvious reason for poor diode quality was improperly formed metal GaAs interfaces caused by contamination from some source. Investigation into this problem was required before processing the remaining large wafer, GT8A501C.

It was discovered later that a test setup grounding problem in the screen room contributed somewhat to the poor ideality factor. Great improvement was obtained by shielding all of the leads and terminating them at a common point. The revised data are shown in table 4.
Diode Dia. = 3 µm

<table>
<thead>
<tr>
<th>Diode No.</th>
<th>η</th>
<th>Rs*</th>
<th>V_B @ 10 µA</th>
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<tr>
<td>104</td>
<td>1.11</td>
<td>3.91</td>
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<td>1.09</td>
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Table 4. GT8A499B Large Wafer After Test Setup Grounding.

*includes 1 ohm test setup resistance.

This change did not answer the question of why the GT8A497C wafer was extremely poor and why a large portion of the GT8A499B wafer was poorer than the test devices.

The answer appeared to lie in the fact that a large (20 mm²) wafer was being metallized instead of small (< 6 mm²) wafer portions which were used during all of the Phase I and Phase II work.

It was proposed to process a small portion of the remaining 8A501 wafer and/or pieces of remaining phase I material for evaluation. The experiment that appeared to be most useful in the solving this problem was the following. Expose the wafer to UV light following completion of the photoresist process to reduce the quantity of nitrogen gas given off by the resist due to light exposure and heating during evaporation of the titanium. Nitrogen
and water vapor are normally released during exposure of the photoresist and are probably released during metallization due to heating of the titanium to a white heat. This gas may contaminate the titanium metal before it is deposited in the diode windows. This phenomenon could explain why smaller wafer portions (6 mm$^2$ versus 20 mm$^2$) yielded better diodes since less resist implies less gas released. It is difficult to conclude other explanations because the diode process had been so repeatable throughout Phase I and II prior to the large wafer runs.

Several experiments were planned in an attempt to resolve the diode quality problem. A control sample consisting of only a small portion of a wafer was metallized as normal. A second identically sized piece was metallized along with a larger piece of dummy material, both of which had all of the photoresist exposed to UV following development of the resist. A third piece was processed as the second, without the additional UV exposure. The DC data were then compared to determine the effectiveness of the modified procedure.

The following large wafer "piggyback" experiment was completed. One (6.5 x 8.5 mm) piece of wafer 8A12 remaining from phase one was processed up to the Schottky metallization step. The wafer was divided into 3 equal parts, GT8A12-3X(-1), (-2) & (-3). The first portion (-1) was processed to diode completion using the established process. The remaining two portions, (-2) and (-3), were mounted piggyback, each on a large silicon wafer which had been resist processed in normal fashion. One of the large wafers (-3) was additionally exposed to the UV light source to drive off gases and water vapor. The end result of the
experiment was three identical small wafer portions metallized under three different conditions, where the resist surface area and subsequent UV exposure treatment were variables. The results of the experiment show that the small wafer (-1) metallized independently yielded good diodes; the (-2) portion which was not UV exposed and the (-3) portion which was exposed to UV both yielded diodes of poor quality. These results were not as expected. The UV exposed wafer was expected to yield good diodes similar to the (-1) portion, if the resist outgasing was contributing to the process problem. The data for this series of experiments are shown in Table 5.

<table>
<thead>
<tr>
<th>Diode Dia.</th>
<th>Standard Small Wafer</th>
<th>Standard Piggyback</th>
<th>UV Exposed Piggyback</th>
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<tr>
<td></td>
<td>η R_s^*</td>
<td>η R_s^*</td>
<td>η R_s^*</td>
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<tr>
<td>1.5 μm</td>
<td>1.15 12.54</td>
<td>1.19 13.54</td>
<td>1.19 10.74</td>
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<tr>
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<td>3.0 μm</td>
<td>1.13 4.29</td>
<td>1.20 4.14</td>
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<tr>
<td>Cross</td>
<td>1.07 2.68</td>
<td>1.10 2.04</td>
<td>1.16 2.73</td>
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</tbody>
</table>

Table 5. DC Test Data GT8A12-3X.

*includes 1 ohm test setup resistance.

This problem was most perplexing and dictated additional experimentation. A new experiment was defined where the large wafer was UV exposed for a much longer period, two minutes, instead of the 15 seconds exposure that was given. The basis for this reasoning was that during insertion of the wafer sample it
was observed that the vacuum system pressure increased approximately one third order of magnitude when the wafer was exposed to the melt. This observation did demonstrate outgassing of the resist (or perhaps the substrate holder) due to heating by the titanium melt. These results also suggested that the wafer preheat or deposition rate would have to be adjusted to the outgassing condition of the large wafer.

To evaluate the effects of a longer UV exposure, wafer GT8A501 was processed through the SiO₂ etch step. The major portion was placed on hold until further assessment of the large wafer processing problem could be accomplished. Two small portions (2 x 3 mm) of this wafer were processed through the metallization process utilizing the post development UV exposure "piggyback" method previously described two UV exposure times were utilized for comparison. The dc characteristics of the "piggyback" diodes were quite dissimilar to those observed on the previous GT8A12-3X experiment. These diodes did demonstrate improved ideality factor but higher series resistance. Most important, the UV exposed wafer demonstrated better ideality factor than the non UV exposed wafer and the longer UV exposure gave better results. These comparative data are shown in table 6.
Table 6. DC data non UV vs UV

*Includes 1 ohm test setup resistance.

The high series resistance associated with the GT8A501 C-1 & C2 runs was reasoned to be associated with insufficient pre-Schottky GaAs etch. This characteristic was observed in the past. The low ideality factor on the long UV exposed wafer was encouraging.

Following these rather encouraging experiments it was decided to process the remaining large portion of wafer GT8A501C3; to provide the deliverables.

The diodes produced from the large wafer run were quite similar to the previous runs, GT8A501C1 & C2. The ideality factors were good for the 5, 3 & 2 μm diodes, but poorer for the 1.5 μm diodes. Also the series resistances were slightly higher when compared to previous "best" small wafer runs. The poor 1.5 μm diodes were a rather new observance. The pre-Schottky etch was
suspect. One explanation was that the etch did not enter the small window as quickly as the large windows due possibly to bubble formation; therefore etching commenced later and insufficient GaAs material was removed, giving rise to both "poorer" ideality factors and "higher" series resistances. Longer etching may have improved this condition. Typical dc data for wafer GT8A501C3 is contained in table 7 and figure 3.

<table>
<thead>
<tr>
<th>Diode dia. µm</th>
<th>V_B 10-11V</th>
<th>R_s*Ω</th>
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<td>1.29</td>
</tr>
<tr>
<td>Large Wafer</td>
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<td>1.14</td>
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<tr>
<td>V_B 10-11V</td>
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<td>1.11</td>
</tr>
<tr>
<td></td>
<td>5.0</td>
<td>1.10</td>
</tr>
</tbody>
</table>

*includes 1 ohm test setup resistance.

The reverse breakdown characteristic of the diodes are very good, in fact better than previous runs. Additionally, the diode uniformity in all parameters was excellent. It was mutually concluded by Georgia Tech and Hughes that processing of new material was not necessary because the diodes did exceed the specifications by quite a wide margin. Furthermore, there did not appear to be an immediate requirement for the very smallest diode, (1.5 µm).

**High Temperature Stress Tests**

Following the conclusion of phase I and after discussing the problem of reliably testing the diodes under thermal stress,
Forward Characteristics GT8A501C3
Diode Dia. L to R 5.0, 3.0, 2.0, 1.5 μm.

Reverse Breakdown. GT8A501C3

Figure 3. Diode Curve Tracer Data.
it was decided to attempt to utilize the orientation cross present on each chip as a test diode rather than one of the more difficult to contact 3 μm diodes. It was felt that a thermocompression wire bond to a larger diode would be much more stable than the whisker-type of contact. Previous tests of 3 μm diodes during phase I required contact to the anode dot with an etched whisker. These whisker contacts were unstable at the high temperatures, 300-350°C. The reason for the instability was not thoroughly understood; however, it appeared that softening or annealing of the whisker at the high temperature caused a pressure change on the diode Schottky barrier.

Several high temperature runs were completed, both on "best" phase I diodes and phase II diodes. These runs were made in order to determine the best procedure for this test.

Diode chips from three phase I runs were mounted in conventional diode packages. Thermocompression wire bonds were made to the cross geometry. Five diodes were bonded this way and placed into the life test fixture. Room temperature dc measurements were performed to determine $n$ and $R_s$ prior to exposure to thermal soak. The fixture temperature was then set to 325°C, and the diode bias current was set to 30 mA. The diode voltages were then measured on a daily basis. This method of testing did not provide the sensitivity required, nor did measuring the voltage at a lower current, 0.1 mA. The diode voltage drops appeared quite stable, but the diode ideality factors and series resistances had long since deteriorated. The most consistent method of determining diode longevity and quality was to characterize the diode at room temperature for $n$, $R_s$, and
The diodes were then heat stressed under bias, and the measurements were repeated at 8 and 16 hour intervals. It is important to note that not only did the diodes receive heat stress while under bias but also received temperature cycling, a most severe test. A drawback to the test procedure was that handling of the packaged diode produced some failures due to static or grounding transients as well as bumping the wire lead with the tweezer causing damage to the wire bond.

Because the test fixture was designed to handle only five diodes, as few as two mishaps could cloud the test results. Therefore, several false starts were encountered before a "feel" for the test procedure was developed. The data obtained from the GT8A501B run, diodes 16-20, shown in figures 4 and 5, is representative of meaningful data. Subsequently, tests were conducted on run GT8A499B utilizing only ideality factor and $V_B$ as the determining factors of diode failure at temperature.

Five diodes from the "large" wafer run GT8A499B were subjected to temperatures of 300°C to 350°C for a total of 473 hours. Following 233 hours, the dc data showed little change under both forward and reverse bias conditions. The temperature was then increased to 325°C. After 144 hours at this new temperature (377 hrs total), all but the number two diode (which shorted) showed little further change; in fact, a slight improvement in ideality factor was observed on diodes four and five. The number one diode was lost in a crack in the screen room subflooring. Number two diode shorted catastrophically (confirmed due to handling). The test temperature was then increased to 350°C. After approximately 30 hours (410 hours total), a decided
Figure 4. Ideality Factor vs. Time

GT8A501B (16-20), 300°C Test
Horiz = 1V/Div  
Vert = 0.01 mA/Div.  

Figure 5. Breakdown vs Time at Temp.  
GTBA501B Heat stress (cross).  
23
upward drift in ideality factor was observed on diodes 3, 4 and 5. This trend continued for the remaining 63 hours (473 hours total) of the test. The reverse breakdown characteristics changed somewhat from their initial values but remain quite stable throughout the test. Figures 6 and 7 show the plotted ideality and $V_B$ data for the GT8A499B high temperature test. This particular run exhibited the best overall performance; unfortunately, too few diodes (500) were obtained from this run. These diodes were supplied to Hughes as engineering models, and at Hughes discretion could be qualified for space flight at a later date if desired. The only apparent additional requirements for qualification are to individually test for $n$ and $R_S$ and to properly box and label.

Thedeliverable wafer run GT8A501C3 was similarly subjected to the temperature stress test. The 300°C temperature was ignored completely because of the long time before any failure. Instead the tests were begun at 330°C where failures would occur in a reasonable time. If no failures were observed, the temperature was increased to 350°C. The diodes performed quite well and met the high temperature requirements. Figures 8a, b, c and 9a, b and c show the result of the high temperature stress test.

RF Test

The rf tests were conducted at Georgia Tech utilizing the Hughes supplied mixer and IF amplifier. Hughes also supplied a number of "Sharpless" type diode mounts and associated piece parts. Diodes from the best phase I run, GT8A16-17, were mounted, tested and compared to the deliverable phase II lot, GT8A501C3.

A superheterodyne receiver was set up as shown in figure 10.
Several measurements were performed using different LO and IF frequencies while maintaining the RF frequency near 60 GHz. A summary of the RF measurements are given in Table 8. These measurements indicate that the GT8A501C3 diodes perform as well or perhaps better than any produced to date.

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<th>Mixer Noise Figure (dB)</th>
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<td>(DSB)</td>
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</tr>
<tr>
<td>22</td>
<td>GT8A501C3</td>
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</table>

*Cut off frequency for the waveguide used is 39.863 GHz
1st two measurements were DSB (56 GHz LO)
2nd two measurements were SSB (45 GHz LO)

Table 8. RF Test Results.
Figure 6. Ideality Factor vs. Time.
GT8A499B-(1-5), 300°C, 325°C, 350°C Test.
Figure 7. Breakdown vs Time at Temp.

GT8A4998 Heat stress (cross).
Figure 8a. GT8A501C3-(19, 20, 23, 24, 25), Ideality Factor vs. Time.  
330°C and 350°C Test.
Figure 8b. GT8A501C3-(27, 27, 31, 32, 33), Ideality Factor vs. Time.
350°C Test
Figure 8c. Ideality Factor vs. Time GT8A501C3-(34-36).  
330°C Test
Figure 9a. Breakdown vs Time at Temp

Diode No.

Start 330°C

128 Hrs. 330°C

200 Hrs. 330°C

264 Hrs. 330°C

352 Hrs. 330°C

+ 72 Hrs. 350°C

Horiz. = 1V/Div
Vert. = 0.01 mA/Div.

GTBA501C3 Heat stress (cross).
Figure 9b. Breakdown vs Time at Temp.
32 GT8A501C3 Heat stress (cross).

Horiz = 1V/Div
Vert = 0.01 mA/Div
Diode No.

Start 330°C

104 Hrs. 330°C

130 Hrs. 330°C

199.5 Hrs. 330°C

272 Hrs. 330°C

Horiz = 1V/Div
Vert = 0.01 mA/Div.

Figure 9c. Breakdown vs. Time at Temp.
GT8A501C3 Heat stress (cross).
Figure 10. Diagram of Noise Figure Test Set-up.
PROCESS CHECKLIST

Millimeter Wave Mixer Diode

Hughes 3414270 Rev. (C)

WAFER PROCESS RUN NUMBER: GT8A501C

DATE: 3-26-82 STAN: HOLD
STAFF: G. N. HILL CONT: 9-7-82 GT8A501C3
PI-1 GaAs MATERIALS SPEC.
Attached Copy  yes ✓  no ✗
Haze ___  Hillock ___  Cracks ___  Other  Dust
Comments: See GaAs material data sheet on file

PI-2 WAFER CLEAN-UP
Process Complete  yes ✓  no ___
Inspect - Pass  yes ✓  no ___
Comments:
Very difficult to remove white specks of unknown contaminant. Much US. Required.
Cleaned up OK.

PI-3 OXIDE GROWTH
Temp  330 °C
Flow  N₂ 12  O₂ 6.5  SiH₄ 46.3
Growth Time  7 min.
SiO₂ Thickness  5100 Å.  Color __________
Step Profile Attached  yes ✓  no ___
Comments:

SiO₂ Thickness sample
Run H GTYA501C
10,000 Å F.S.

5100 Å
PI-4 DIODE GEOMETRY POSITIVE LITHOGRAPHY

Spin Speed \(6\,K\) rpm

Time 25 secs

Pre Expose Bake Temp. 95 °C Time 25 min.

Expose 4 secs

Develop 25 secs

Inspect - Pass yes ✓ no 

Postbake Temp 110 °C Time 10 min.

Comments:

PI-5 OXIDE ETCH AND RESIST STRIP BACK

Etch 1. Time 35 secs Color Tan

Etch 2. Time 5 secs Color Clean

Etch 3. Time — secs Color —

Vacuum Bake Temp 150 °C Time 30 min.

Plasma Etch Time 5 min.

Inspect - SEM Pass yes ✓ no 

Comments:
PI-6 DEPOSIT TRI-METAL

Etch Temp  22 °C  Time  30 secs

E-Beam System pressure <2x10^-9 Torr  18 hrs.

Titanium - power  0.7 KW,  Monitor Res.  4.3 ohms
Platinum - power  1.5 KW,  Monitor Res.  3.2 ohms
Gold - power  1.6 KW,  Monitor Res.  1.3 ohms

Inspect - Metal Thicknesses

Ti 1200 Å  Step Profile  yes  no
PT 500 Å
Au 3000 Å

Comments:  Step Profile only

PI-7 LIFTOFF

SEM Photo Attached  yes  no

Comments:
PI-8  WAFFER THIN DOWN

Wafer Thicknesses Start ________ mm 16.8 mils
After Lap ________ mm 4.5 mils
After Polish ________ mm 2.0 mils
Inspect - Pass yes  no
Comments:

PI-9  METALLIZE CATHODE

Evaporator Pressure 5 x 10^-7 torr
Alloy Contact, Temp °C 375  Time 3 min
Sputter Ti, Pt, Au
  Ti 1000 Å  Step Profile yes  no
  Pt 400 Å
  Au 2400 Å
SEM Photo Attached yes  no
Comments:  CT 9A501C3  SPUTTERED
       STEP PROFILE - CATHODE TRIMETAL OVERCOAT
       1000 Å PS  
       15
       3 Au 2400 Å
       Ti 1000 Å
       Pt 1000 Å
       CuR

5 of 14
PI-10 DC TEST

Wafer Map Attached  yes  /

Comments: Very uniform devices
See capacitance data also attached

PI-11 WAFERSCRIBE AND BREAK

Completed  yes  /

Comments: Some incomplete breakage
Must break individual segments
No problems encountered
UNLESS OTHERWISE SPECIFIED:
TOLERANCES — XX ± .01
XXX ± .005
FRAC ± 1/32

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* Includes 1m of setup resistance

WAFFER MAP 3 in. Dia.
RUN NO. GT8A50K-3
### Capacitance 3m dia Dot CTY4501C3

#### Typical Data This Lot

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<td>10</td>
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<tr>
<td>Avg</td>
<td>12.8</td>
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</table>

#### Cutoff Frequency

\[
f_c = \frac{1}{2\pi R C (0)}
\]

\[
f_c = \frac{1}{(6.28) (4\pi) (12.8 F_{F15})}
\]

\[3.17 \mu Hz\]
QUALITY ASSURANCE
GaAs Epitaxial Wafer

For FET Type Devices
- Low Noise
- Power
- Other

with
- Buffer
- Contact Layer

For IMPATT Type Devices
- Flat Profile
- Read Profile
- Other

- Single Drift
- Double Drift
- Thick Buffer
- Standard Buffer
- μ" contact

Customer: [Signature]

Customer Order No.: 020-091-A2666

Spec. No.

Memo No.


SUBSTRATE

Supplier: SEE

Crystal Boule No.: 0180

Slice No.: 93

Orientation: 2° off <100> toward <110>

Carrier Concentration: 1.8 x 10^18 cm^-3

Pregrowth Thickness: 400 μm

Dopant: Te

Resistivity**: 1.5 x 10^-3 Ω - cm

ELECTRICAL CHARACTERISTICS

<table>
<thead>
<tr>
<th>No.</th>
<th>Layer Type</th>
<th>Carrier Concentration</th>
<th>Dopant</th>
<th>Thickness</th>
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<tbody>
<tr>
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<td>&gt; 2 x 10^18 cm^-3</td>
<td>S1</td>
<td>5.0 μm</td>
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<td></td>
<td>Buffer</td>
<td>x10^18 cm^-3</td>
<td></td>
<td></td>
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<tr>
<td>2</td>
<td>Active</td>
<td>1.0 x 10^16 cm^-3</td>
<td>S1</td>
<td>0.2 μm</td>
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<td></td>
<td>Spike</td>
<td>x10^17 cm^-3</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Contact</td>
<td>x10^18 cm^-3</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Wafer Size: 2.2 x 2.8 cm

Area: 6.16 cm^2

Surface Morphology: 2

Q\(^+\): 1 x 10^19 e\(^-\) cm\(^-3\)

V\(_{knee}\) volts (from C vs V curve)

C\(_0\): 11.63 x 10^6 F cm\(^-2\)

Interface: 0.08 μm/decade

DELIVERY AUTHORIZATION

Delivery authorized
- to fill order
- to fulfill contractual obligations

For Device Research
- For Process Research
- For Calibration
- For Sample Purposes
- Other

Amount Ordered: 3

Amount Delivered: 1

Date: 4-9-87

William H. Labosier
QUALITY ASSURANCE

GaAs Epitaxial Wafer

For FET Type Devices

☐ Low Noise ☐ Power ☐ Other

with ☐ Buffer ☐ Contact Layer

For IMPATT Type Devices

☒ Flat Profile ☐ Read Profile ☐ Other

☐ Single Drift ☐ Double Drift with ☐ Thick Buffer ☐ Standard Buffer ☐ Si contact

Customer: Georgia Tech

Customer Order No.: 41-81-71440

Spec. No.:

Memo No.:

Contract No.:


SUBSTRATE

Supplier:

Crystal Boule No.: 01-0

Slice No.: 90

Orientation: 2° off <110> toward <110>

Pre-growth Thickness: 400 μm

Carrier Concentration: $1.8 \times 10^{18} \text{ cm}^{-3}$

Resistivity*: $15 \times 10^{-3} \text{ Ωcm}$

Dopant: TE

ELECTRICAL CHARACTERISTICS

<table>
<thead>
<tr>
<th>Measured</th>
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<tr>
<td>No.</td>
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<tr>
<td></td>
</tr>
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</table>

Water Size: $2.2 \times 2.6 \text{ cm}$

Area: $6.16 \text{ cm}^2$

Surface Morphology: 2

$O^*: 1.0 \times 10^{19} \text{ cm}^{-2}$

$C_o: 12.4 \times 10^{10} \text{ pF/cm}^2$

$V_{knee}$ volts (from C vs V curve)

$\text{Interface}: 0.05 \mu m/\text{decade}$

GATE → CLEAVE

DELIVERY AUTHORIZATION

Delivery authorized ☒ to fill order ☐ to fulfill contractual obligations

☐ For Device Research ☐ For Process Research ☐ For Calibration

☐ For Sample Purposes ☐ Other

Amount Ordered: 3

Amount Delivered: 2

William H. Labosky

Date: 4-9-81
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<th>Etch</th>
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<td>161.9</td>
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<tr>
<td>2nd</td>
<td>161.5</td>
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</tr>
<tr>
<td>3rd</td>
<td>162.1</td>
<td></td>
</tr>
<tr>
<td>4th</td>
<td>162.5</td>
<td>v</td>
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<td>5th</td>
<td>164.9</td>
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<td>553.0</td>
<td>90</td>
</tr>
<tr>
<td>8th</td>
<td>540.5</td>
<td>180</td>
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</tbody>
</table>
QUALITY ASSURANCE

GaAs Epitaxial Wafer

For FET Type Devices: □ Low Noise □ Power □ Other _______________  
with □ Buffer □ Contact Layer

For IMPATT Type Devices: □ Flat Profile □ Read Profile □ Other _______________  
□ Single Drift □ Double Drift □ Thick Buffer □ Standard Buffer □ Other _______________

Customer: Georgia Tech  
Customer Order No: 11-81-71440  
Spec No: _______________  

SUBSTRATE

Supplier: SE  
Orientation: 2° off <100> toward <110>  
Carrier Concentration: 1.8 x 10¹⁸ cm⁻³
Resistivity: 1.5 x 10⁻³ ohm-cm

ELECTRICAL CHARACTERISTICS

<table>
<thead>
<tr>
<th>No.</th>
<th>Layer Type</th>
<th>Carrier Concentration</th>
<th>Dopant</th>
<th>Thickness</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Buffer</td>
<td>&gt;2 x 10¹⁵ cm⁻³</td>
<td>Si</td>
<td>50 μm</td>
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<tr>
<td>2</td>
<td>Active</td>
<td>1.5 x 10¹⁶ cm⁻³</td>
<td>Si</td>
<td>50 μm</td>
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<tr>
<td></td>
<td>Active</td>
<td>1 x 10¹⁷ cm⁻³</td>
<td></td>
<td>0.4 μm</td>
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<tr>
<td></td>
<td>Spike</td>
<td>1 x 10¹⁴ cm⁻³</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Contact</td>
<td>1 x 10¹⁴ cm⁻³</td>
<td></td>
<td></td>
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</tbody>
</table>

Wafer Size: 2.3 x 2.5 cm  
Area: 6.47 cm²

Surface Morphology: 2

DELIVERY AUTHORIZATION

Delivery authorized:  X  to fill order  □ to fulfill contractual obligations
□ For Device Research  □ For Process Research  □ For Calibration
□ For Sample Purposes  Other _______________

Amount Ordered: 3  
Amount Delivered: 3  
Date: 4-9-81

William H. Labossier

Raytheon
PROCESS INSTRUCTIONS

FOR

MILLIMETER WAVE MIXER DIODES

HUGHES DRAWING

3414270 REV C

Prepared by
G. N. Hill

G. N. Hill 6-5-81

1 of 43
PROCESS FLOW CHART FOR MILLIMETER WAVE MIXER DIODES
Major Activity
Block Diagram

( ) denotes lab area in which process step takes place.
Layout and Major Equipment Location in the Microelectronics/Semiconductor Laboratory.
GEORGIA TECH ENGINEERING EXPERIMENT STATION  
Gallium Arsenide Material  

PROCESS INSTRUCTIONS FOR MILLIMETER WAVE DIODE  
PI-1

SCOPE
To specify epitaxial gallium arsenide wafer material

APPLICABLE DOCUMENTS
Contract No. S8-738203-LV3  
Hughes Drawing 3414270  Rev (C)

REQUIREMENTS
1. Gallium arsenide substrate characteristics to be supplied or as required.
   a. Boule supplier, Boule number and wafer number
   b. Orientation, 2° off < 100 > toward < 110 >
   c. Dopant, Te
   d. Carrier Concentration > 2 x 10^18 cm^3
   e. Resistivity, 1.2 ohm cm^3
   f. Area, as required, typically 6-7 cm^2
   g. Backside, lapped flat

2. Gallium arsenide buffer layer characteristics
   a. Dopant, silicon
   b. Carrier concentration > 2 x 10^18 cm^-3
   c. Thickness > 3 μm

3. Gallium arsenide, active layer characteristics
   a. Dopant, silicon
   b. Carrier concentration, 1.1 x 10^17 cm^-3 ± 0.11 x 10^17 cm^-3
   c. Thickness, 0.25 μm ± .05 μm

QUALITY ASSURANCE PROVISIONS
4. Equipment
   a. Microscope 7-50x.

5. Inspect surface morphology under 7-50 power magnification.  
   Any defect noted in 5a, b, c, will be cause for rejection.
   a. Surface haze
   b. Hillocks
   c. Cracks
6. Data sheets
   a. Impurity profile
   b. Vendor quality assurance document

7. Handling
   a. Do not touch wafer with bare hands.
   b. Do not slide wafer, face down, on any surface.
   c. Receiving will not open package immediately surrounding wafer.
SCOPE

To describe gallium arsenide wafer clean-up prior to depositing SiO₂

APPLICABLE DOCUMENTS

Contract Number S8-738203-LV3
Hughes Drawing 3414270 Rev. (C)

REQUIREMENTS

1. Equipment
   a. Wet chemical fume hood
   b. Hot plate, Model HPA 1915B, Thermolyne
   c. Microscope, 7-30X, Bausch and Lomb
   d. Sonic cleaner, Model 75, Beuhler Ltd.
   e. Sundry supplies: Tweezers, Tri-grip teflon holder, beakers, filter paper, petri dishes, etc.

2. Chemicals and Gases - Electronic grade or equivalent high purity
   a. Dry nitrogen gas, 99.994%.
   b. Hydrochloric acid
   c. Deionized water, filtered, 10 megohm or better.
   d. Methanol
   e. Trichloroethylene

3. Procedure
   a. Carefully remove gallium arsenide wafer from storage container.
   b. Grip wafer with tri-grip teflon tweezer.
   c. Prepare and submerse wafer into a beaker of trichloroethylene. Sonic agitate beaker for 1 minute.
   d. Prepare a second beaker of trichloroethylene. Heat to boiling. Immerse wafer into vapor for 30 seconds.
   e. Rinse wafer in methanol, then rinse in running DI water for 30 seconds.
   f. In a beaker, prepare 50 ml of hydrochloric acid. Also prepare 200 ml of deionized water. Heat HCl until bubble forms, then immerse the wafer into the HCl for 30 seconds. Rinse in the deionized water beaker for 30 seconds. Follow with 2 minutes of running deionized water rinse.
   g. Blow dry using N₂ opposed jet dryer.
   h. Inspect the wafer surface using the 7-30X microscope. Observe the reflected light from the wafer at various angles. Water spots or other visible contaminates is cause for rejection. Reclean if required.
i. Place wafer into clean, covered petri dish.
j. Label dish cover to retain wafer identity.
SCOPE

To describe the procedure for growing an oxide layer.

APPLICABLE DOCUMENTS

Contract No. S8-738203
Hughes Drawing No. 3414270  Rev (C)

SYSTEM DESCRIPTION

The system schematic is shown in Figure 1. As the system is set up, the valves are contained in one of three groups. The control manifold houses the silane (SiH₄), nitrogen (N₂) and oxygen (O₂) control valves as well as acting as a mechanical support for the deposition chamber. The flowmeter panel contains the silane, nitrogen and oxygen flowmeters and flow valves; and the nitrogen and oxygen supply valves. The silane tank assembly includes the silane supply valve, the silane regulator outlet valve, the regulator purge valve, and the silane line purge valve.

REQUIREMENTS

1. Gases
   a. Ultra pure nitrogen 99.999%
   b. Ultra pure oxygen 99.999%
   c. Electronic Grade 3% silane in nitrogen
   d. Dry nitrogen gas 99.994%

2. Equipment
   a. Air conditioned limited access area
   b. Hood, to vent gases
   c. Growth chamber, Setup shown in Figure 1
   d. Calibrated color comparison tablet.
   e. Hot plate, HPA1915B, Thermolyne
   f. Sundry supplies; tweezers, petri dish, filter paper, etc.

3. Start-up
   a. Attach thermocouple bridge to check system operating temperature for 300 °C.
   b. Turn on mass flow meter 30 minutes prior to using system.
4. Set valves to their proper initial positions
   a. Silane control valve - closed - handle vertical
   b. Nitrogen control valve - off - handle vertical
   c. Oxygen control valve - closed - handle vertical
   d. Nitrogen supply valve - closed - clockwise
   e. Oxygen supply valve - closed - clockwise
   f. Silane flow valve - N/A
   g. Nitrogen flow valve - N/A
   h. Oxygen flow valve - N/A
   i. Silane supply valve - closed - clockwise
   j. Silane regulator outlet valve - closed - clockwise
   k. Silane line purge valve - off - handle vertical
   l. Regulator purge valve - off - clockwise

5. Purge system
   a. Open nitrogen and oxygen supply valves (CCW).
   b. Open nitrogen control valve (handle vertical).
   c. Set nitrogen flow valve for a flowmeter reading of 6 (black ball).
   d. Simultaneously set the silane control valve to "SiH₄" and open
      the silane line purge valve (horizontal).
   e. Set silane mass flow meter to read 200%.
   f. Set oxygen control valve to "O₂".
   g. Set oxygen flow to 6.5 (black ball).
   h. Allow system to purge for a total of five minutes.

6. Load wafer
   a. Set oxygen and silane control valves to "Vent".
   b. Lower jack while carefully guiding platform from the chamber.
   c. Using tweezers, carefully place the wafer face up on the
      platform. Avoid scraping the platform which may generate SiO₂
      particulate matter. If such matter is generated it may be
      removed by blowing with nitrogen gas.
   d. Raise platform until the crossbar supporting the chamber
      begins to flex.
   e. Turn on table rotation switch.

7. Establish gas flow
   a. Turn silane line purge valve off (vertical).
   b. Turn silane supply valve on (CCW).
   c. Turn regulator outlet valve on (CCW).
   d. Reset silane flowmeter for a flow of 85%.
   e. Increase nitrogen flow to 12.
   f. Allow two minutes of nitrogen and silane flow.

8. Grow oxide, 5000 ± 500 Å Thickness required.
   a. Turn silane control valve to "SiH₄".
   b. Quickly turn oxygen control valve to "O₂".
   c. Watch oxide growth carefully. Maintain silane flow at 85% as
      required. During the SiO₂ deposition, observe and compare the
wafer surface color under cool white fluorescent light with the calibrated color comparison chart. The deposition rate is approximately 500 Å per minute, therefore; approximately 10 minutes is required to deposit 5000 Å.

d. Turn silane and oxygen control valves to "Vent" when 5000 Å is grown.

9. Turn silane tank assembly off

   a. Close silane supply valve (CW).
   b. Open silane flow valve for rapid flow, 200%.
   c. Watch the high scale regulator carefully. When it beings to approach zero, start closing regulator outlet valve.
   d. When the low scale regulator beings to drop, quickly finish closing the regulator outlet valve (CW).

10. Purge system

   a. Open silane line purge valve (horizontal).
   b. Reduce nitrogen flow to between 5 and 6.
   c. Turn oxygen control valve to "Closed".
   d. Close oxygen supply valve (CW).
   e. Close nitrogen control valve (vertical)
   f. Wait two minutes.
   g. Turn silane control valve to "Closed".
   h. Close silane line purge valve (vertical).
   i. Close nitrogen supply valve (CW).

11. Retrieve wafer using tweezer. Utilize caution noted in PI-3, 6c.

   a. Turn off table rotation switch.
   b. Lower jack.
   c. Remove wafer and return it to the clean, covered container.
   d. Raise jack.

13. Inspect

   a. Proper color, 5,000 ± 500 Å. Determined from the calibrated color comparison tablet.
   b. Uniform color across wafer surface.
   c. Note: If the deposited film is rejected, the oxide may be etched away and a repeat deposit cycle initiated. Consult this process instruction PI-3, 14.

14. Reclaim wafer. Note: Proceed only if the wafer is rejected.

   a. Prepare separately 50 ml of hydrofluoric and hydrochloric acid. Use a plastic beaker for HF. Prepare separate 200 ml beakers of deionized water.
Grasp the wafer in the trigrip teflon tweezer. Immerse the wafer into the HF for 1 minute, then rinse in the di water. Follow with 1 minute of running di water rinse.

c. Heat the hydrochloric acid until bubbles form.

d. Immerse the wafer into the hydrochloric acid for 30 seconds. Rinse in the di water for 30 seconds. Follow with 2 minutes of running deionized water rinse.

e. Blow dry using the $\text{N}_2$ opposed jet drier. Place the wafer into the covered container and repeat, PI-3.
Figure 1. Oxide Growth System Schematic.
Diode Geometry
Positive lithography

PROCESS INSTRUCTIONS FOR MILLIMETER WAVE MIXER
DIODE

SCOPE

To describe the procedure for delineating the diode geometry

APPLICABLE DOCUMENTS

Contract No. S8-738203-LV3
Hughes Drawing 3414270  Rev (C)

REQUIREMENTS

1. Equipment - set up in air conditioned, limited access room.
   a. Wet chemical fume hood
   b. CVD SiO₂ deposition system. Lab built.
   c. Photore sist spinner, model no. AHT2A-T, Headway Research, Inc.
   d. Ovens, 95 °C and 110 °C.
   e. Mask exposure system. model no. 686B, Kulicke & Soffa.
   f. Traveling stage microscope, 100x to 800x power, Unitron, model no. TMS-6560.
   g. Sonic cleaner, model no. 75, Buehler, Ltd.
   h. Hot plate, model no. HP-A1915B, Thermolyne.
   i. Sundry supplies: tweezers, beakers, petri dishes, etc.
   j. Mask A2960, or as determined by process Engineer.

2. Chemicals and gases, electronic grade or equivalent high purity.
   a. Trichlorethelene
   b. Methanol
   c. DI water 10 megohm or better.
   d. Hexamethyldisilazene (HMDS)
   e. AZ 1350 J - photoresist thinned 3:1
   f. AZ 351 developer
   g. AZ thinner

3. Apply Photoresist - Preset speed, 6000 RPM, time: 25 secs.
   a. Remove wafer from transport container. Note: Use tweezer when ever handling wafer.
   b. Place wafer onto spin chuck. Turn on vacuum.
   c. Apply HMDS. Cover entire surface. Let soak for 30 secs.
   d. Press start spin, let stand for 30 secs before applying resist.
   e. Apply thinned AZ1350J resist dropwise to the wafer center until one half of the wafer is covered, start spin immediately.
   f. Release vacuum and remove wafer, placing wafer into a clean covered petri dish.
   g. Place dish into 95 ± 5 °C oven. Remove cover, then bake for 25 minutes.
4. Expose wafer - Turn on mask aligner, preset exposure time for 5 secs. Allow unit to warm up for at least 15 minutes. Load mixer mask no. A 2960. Keep mask in storage container when not in use. DO NOT TOUCH SURFACES.

a. Following bake, allow wafer to cool in covered dish for 5 minutes.
b. Center a new millipore filter HAWP 25 on aligner chuck. Place wafer, centered, on filter.
c. Ensure that mask vacuum is off. Rotate wafer chuck into position under mask. Lower ball chuck to lowest position, manual adjust.
d. Press pantograph button. (Raises ball chuck partially). Turn on mask vacuum, then continue raising ball chuck until the wafer just contacts the mask.
e. Increase separation by one click of separate switch.
f. Press pantograph button again (clamps wafer to mask).
g. Press exposure.
h. When cycle is complete, rotate chuck away from mask. Remove wafer.

5. Develop - Mix developer 1 part AZ351 to 3.5 parts DI H$_2$O (20 ml;70 ml). Also prepare DI H$_2$O rinse in a 250 ml beaker.

a. Place wafer onto vacuum hold-down wand.
b. Immerse into developer for 45 seconds, rinse immediately.
c. Rinse again in running DI H$_2$O for 2 minutes.
d. Blow dry using dry nitrogen gas.

6. Inspect

a. Inspect the images formed by the process by first using low power (100x) to scan the wafer for gross defects; such as cracks or resist lifting, then use 800x to examine the edge acuity of the cross geometries. The diode holes should be clear of resist, however, due to the interference fringes present, it may be difficult to observe. A small corner of the wafer may be broken away and subjected to SEM analysis if necessary.

7. Post bake

a. Bake for 10 minutes at 110 °C.
b. Remove from oven and store in clean, covered glass petri dish.
SCOPEx

Describes the delineation of the deposited oxide, vacuum bake and resist strip back, preparatory to metal deposition.

APPLICABLE DOCUMENTS

Contract No. S8738203-LV3
Hughes Drawing 3414270 Rev (C)

REQUIREMENTS

1. Equipment - setup in an air conditioned, limited access facility.
   a. Wet chemical fume hood
   b. RF sputtering system - to be used for high vacuum bakeout of the photoresist. Perkin Elmer model 2400, with substrate heat and temperature monitoring provisions.
   c. Plasma strip system - LFE Corp, model PDS/PDE 301.
   d. Traveling stage microscope - Unitron model TMS 6560, 100 to 800x.
   e. General purpose microscope - 7-30x, Bausch & Lomb
   f. Sundry supplies: plastic beakers, teflon trigrig tweezers, filter paper, graduated cylinder, safety goggles, plastic gloves, teflon stir rod.
   g. Timer - seconds, minutes.

2. Chemicals and gases - electronic grade or equivalent, high purity.
   a. Hydrofluoric Acid
   b. Ammonium Fluoride
   c. Oxygen gas 99.994%
   d. Deionized water, 10 megohm or better
   e. Nitrogen gas 99.994%
   f. Microclean - used as wetting agent.

3. Procedure - define diode area in deposited oxide.
   Secure wafer processed in PI-4. CAUTION: wear protective goggles and gloves. HF extremely hazardous in contact with skin, eyes and lungs.
   a. In a fume hood, dispense 60 ml ammonium fluoride into 100 ml plastic beaker, then add 10 ml of HF. Stir with teflon rod. Let solution stand for 1 hour.
   b. Prepare 200 ml DI rinse in plastic beaker.
   c. Prepare wetting agent. 1 drop microclean in 200 ml DI water.
d. Grip wafer with teflon tri-grip tweezer.

e. Immerse wafer into wetting agent then immediately immerse wafer in NH₃ HF etch solution. Start timer. Etch for 45 seconds. Stop timer and rinse wafer in DI water beaker, then running DI water.

f. Inspect etch progress by observing color change in orientation crosses. Color should be blue (1200 Å). The etch rate is approximately 85 Å per second.

i. Continue etching for 10 more seconds. Observe again, cross will appear slightly tan to clear. Etch again for 5 more seconds.

h. Rinse thoroughly in running DI water.

i. Blow dry using N₂ gas, then return wafer to petri dish storage container.

4. Procedure - high vacuum resist bakeout.

Obtain wafer from oxide etch step PI-5, 3i. Transport to sputtering system for vacuum bakeout.

a. Push start vent switches to open vacuum chamber.

b. Raise chamber head carefully so as not to stretch wires. Place wafer onto heated stage, face up.

c. Lower chamber head. Push start pump. System will automatically sequence. Turn on vacuum gauge.

d. Charge system with LN₂.

e. When system pressure reaches 7 x 10⁻⁷ Torr, turn on heater supply and temperature monitor.

f. Increase temperature to 150 °C. Let stabilize and bake for 30 minutes.

g. Lower temperature. Allow to cool to 30 °C.

h. Push start vent to open chamber.

i. When vented, remove wafer. Close chamber and start pump. Turn off vacuum gauge.

j. Place wafer into covered petri dish.

5. Procedure - resist etch back.

Obtain wafer from high vacuum bakeout step PI-5, 4j. Transport to plasma strip reactor.

a. Turn on vacuum pump. Turn on main system. Set mode to strip. Press start cycle. Preset RF power to 350 watts. Set O₂ flow to 30 cc/min. Set timer to 4.75 minutes.

b. Start sequence. Push vacuum release; open chamber. Place wafer on carrier face up. Close chamber. Press start cycle. System will auto sequence.

c. Open chamber. Remove wafer. Place into covered petri dish.

6. Inspect

Under microscopic examination, determine that the photoresist has been removed sufficiently in the etched oxide openings. Figure 1 shows the desired etch back.
Figure 1. Plasma Strip. Photoresist Strip Back.
SCOPE

To describe procedure for depositing anode contact metals by E-beam evaporation methods.

APPLICABLE DOCUMENTS

Contract No. S8-738203-LV3
Hughes Drawing 3414270  Rev. (C)

REQUIREMENTS

1. The contact metals Ti, Pt and Au described in the Process Instruction Section PI-6.1 will be deposited sequentially onto a surface delineated wafer processed in PI-4 and PI-5.

2. Equipment - setup in an air conditioned limited access facility.
   a. Wet chemical fume hood.
   b. E-beam evaporator system consisting of models VeB-6 E-gun, VeB-6c control, VeB-6T transformer, and lab modified vacuum system comprised of dual Ultex ion pumps, powered by a model 60-656 supply. System roughing is accomplished by a Welch, turbo-molecular pump model 3102. Included are three crucibles, precharged with metal described in PI-6.1.
   c. Tencor, Alpha Step Profiler
   d. Sundry supplies: tri-grip tweezers, beakers, microscope slide, timer, filter paper, apiezon black wax, petri dishes, safety goggles, plastic gloves, glass dish 8 x 10 x 2", etch rate graph and glass thermometer.

3. Chemicals and gases - electronic grade or equivalent high purity.
   a. Hydrochloric acid
   b. Phosphoric acid
   c. Hydrogen peroxide
   d. Dry nitrogen gas 99.994%
   e. Deionized water - 10 megohm or better.
   f. Hydrofluoric acid
   g. Techni-strip AU.
   h. Trichloroethylene

4. Safety
   a. Dispense chemicals in a safe manner. Do not allow contact with skin. Wear protective goggles and gloves.


   Obtain wafer completed and described in PI-5.
NOTE: Do not prepare wafer unless it can be loaded into the vacuum chamber immediately following surface preparation.

a. Prepare surface etch solution consisting of 1 part hydrogen peroxide, 3 parts phosphoric acid, and 50 parts room temperature DI water. Also prepare a beaker of DI rinse water.

b. Dispense chemicals using Repipet dispensers of the type 13-678v Fisher Scientific Co., 90 ml of etch solution is used. After mixing, the beaker is placed in a flat glass dish, half filled with room temperature water.

c. Let etch stand for 5 minutes. Measure the temperature of the etch solution. Consult the etch rate graph shown in Figure 1 and determine the time necessary to remove approximately 0.05 \( \mu \)m of GaAs in the oxide opening.

d. Grasp the wafer, face up, with the trigrip tweezers. Immerse wafer in the etch solution. Start timer simultaneously and etch for the required time.

e. Rinse immediately in the DI water beaker, then rinse in running DI water for 3 minutes.

f. Blow dry using filtered N\(_2\) gas. Place wafer into clean, covered petri dish.

6. Procedure - load wafer into vacuum evaporator

The vacuum evaporator is described in Figure 2. The system idles in a pumped-down condition having a pressure of 2-5 \( \times 10^{-9} \) Torr. The interlock gate valve is closed. The turbo isolation valve is closed and turbo pump is off. The mechanical pump is running with the foreline valve closed.

a. Ensure that the sample slide rod is pulled into interlock chamber and the interlock gate valve is closed.

b. Vent the interlock chamber. Open all N\(_2\) valves.

c. Loosen all of the bolts holding the sample rod flange. N\(_2\) will constantly purge the interlock chamber. Remove all but the top bolt. Have an assistant remove this bolt while you hold the sample rod flange and support tube.

d. Pull the sample rod flange away from the system. Place flange into the bench vise provided for that purpose.

e. Load resistance monitor. Slip into the clips provided. Check for short circuits.

f. Load wafer, face up, placing it into the wafer clip provided.

g. Install a new copper gasket into the flange.

h. Replace sample rod flange. Ensure that the wafer faces down when installed.

I. Close N\(_2\) purge valves.

7. Pump Down Interlock Chamber; then Main Chamber.

a. Slowly open foreline valve. Watch vacuum gauge on front panel. When the pressure indicates 100 microns or less, turn on turbo pump.
b. When the pressure indicates zero on the pressure gauge, begin cracking open the turbo isolation valve. A gurgling in the mechanical pump and an increase in pressure reading to between 5 and 10 Torr indicates proper pumping. Do not crack valve further until pressure decreases to 0.5 Torr. When pressure indicates zero, open valve about 2 inches further. Allow to pump in this condition for 45-60 minutes.

c. Close the isolation valve.

d. Open the interlock gate valve while observing the ion supply pressure indicator. Pressure will rise to the mid 10⁻⁶ Torr scale.

e. Turn on the titanium sublimation pump. Pressure will rise, then drop to less than 10⁻⁶ Torr. Continue observing the ion gauge. A slight increase in pressure will again be observed. Turn off titanium pump. Pressure should again drop. When drop ceases, again turn on titanium pump. Watch rise, drop, and slow rise again.

Note that with each cycle of turning titanium on and off, the base pressure will be lower. Continue this procedure until system remains stable - well on the 10⁻⁷ Torr scale.

The best results have been obtained when the system is allowed to pump at least 16 hours, attaining a base pressure of 2-5 x 10⁻⁹ Torr.

f. Connect ohmeter to the resistance monitor terminal.

8. Evaporation of the Tri-metal System - Ti, Pt, and Au.

a. Preheat all of the metal charges by sequentially beaming them for 20 seconds to their evaporating temperature. Titanium - 0.7 kW, 11 kV range; Platinum - 1.5 kW, 15 kV range; Gold - 0.6 kW, 11 kV range.

b. Position the titanium crucible in the beam; then again turn up the E-gun beam current to 0.7 kW for 10 seconds.

c. Lower the beam current to idle the titanium at 0.125 kW. This temperature will supply enough radiant heat to increase the wafer temperature to approximately 150 °C which provides a final bakeout.

d. Insert the wafer sample rod into the main chamber. Open the shutter and allow the wafer to heat for 75 seconds. Increase the beam current to 0.7 kW. Monitor the change in resistance on the ohmeter. When 250 ohms is attained (20 seconds), close the shutter and slide the sample rod out of the main chamber. Lower the beam current to idle, 0.125 kW. Allow the sample to cool. Watch the resistance monitor. When stable, again insert the wafer and repeat two more 20 second intervals, allowing to cool each time. When the monitor reads 60 ohms, reduce the time for the next insertion to 15 seconds; then 5 seconds until approximately 45 ohms is attained. Pull sample rod back into the interlock. Turn off the beam power.

e. Position the platinum crucible in the E-beam. Turn the voltage range switch to 15 kV. Turn up the beam power to 1.5 kW. After 30 seconds, insert wafer into main chamber. Open shutter for 2 seconds; then pull sample rod back and allow to cool. The film monitor
resistance should now read 35 ohms. Slightly lower is acceptable (30 ohms). If higher, repeat for 2 seconds more. Turn off the beam power.

f. Position the gold crucible in the E-beam. Turn the voltage range switch back to 11 kV. Turn up the beam power to 0.6 kW. Insert the sample rod and open the shutter for 5 seconds; then retract the sample rod. Allow to cool and repeat 3 cycles. The film monitor should read 1.6 ± .3 ohms when completed. Turn off E-beam supply. Retract sample rod sufficiently to close gate valve.

g. Close the interlock gate valve. Open N₂ purge valves. Disconnect ohm meter. Loosen bolts to remove sample rod flange as performed in 6.c.

h. Remove wafer and resistance monitor. Reload new monitor, if desired. Place wafer into covered petri dish. Label run number, e.g. GTRAY 9A16-(No.)

9. QUALITY ASSURANCE

The resistance monitor for each run will be preserved. One end of the monitor may be cleaved and subjected to selective etching of the cleaned interface. A second method may employ a completed masked cross on the GaAs diode chip.

a. Cleave sample and mount to SEM stub, cleaved edge up.


c. Etch in 10% HF for 10 seconds. Delineates titanium film. Then rinse in di water for 30 seconds.

d. Platinum film remains unaffected.

e. SEM photomicrographs will serve as file data.

OR

a. Mount a chip in black wax onto a glass slide.

b. Mask off a portion of the cross geometry using black wax.

c. Etch in 60°C Techni-strip to remove the exposed gold film. Then rinse in Di water. This creates the gold platinum step.

d. Etch in 10% HF for 1 minute. This etches the titanium under the platinum, creating a platinum titanium step. Then rinse in Di water and N₂ blow dry.

e. Remove wax mask using trichloroethylene.

f. Step profile the resultant etch steps on the Alpha Step Profiler.

g. Attach the profile data to the run sheet.
Figure 2. E-beam system block diagram.
SCOPE

Describes contact metals for anode and cathode contacts

APPLICABLE DOCUMENTS

Contract number S8-738203-LV3
Hughes Drawing 3414270   Rev (C)

REQUIREMENTS

Anode contact

1. Diodes will be produced utilizing a tri-metal system for the anode contact composed of titanium, platinum and gold.
2. The deposited pattern will be in accordance with sketch figures A, B and C.
3. Titanium, 1000-1500 Å thick will be used to form the metal semiconductor contact
4. Platinum, 500 Å thick, will be used as an intermediate metal to prevent the formation of a resistive titanium gold compound.
5. Gold 2000 Å thick will be used as the external contact metal.

Cathode Contact

6. Gold-germanium alloy, consisting of 88% gold and 12% germanium will be used as the back contact metal. A nickel layer will follow which will serve to stabilize the alloy during heat treatment.
7. The alloy will be further coated with a similar tri-metal described in 3, 4 and 5 after heat treating the deposited alloy.

Quality Assurance

8. All metals to be at least as good as, or better than, 99.97% pure.
9. Before depositing metals, they will be heated to their evaporation temperature until such time as the observed charge in each crucible is fully melted and remains stable under the condition; when the beam power is increased 20% for 10 seconds in excess of the established running conditions described in PI-6, 8a.
2 \mu m \phi \text{ CLEAR ON DARK FIELD}

.001 INCHES

4 \mu m

.015 INCHES

10 \mu m

5 \mu m \phi \text{ CLEAR BORDER}

5 \mu m \phi \text{ CLEAR ON DARK FIELD}

4 \mu m

5 \mu m \phi \text{ CLEAR ON DARK FIELD}

8 \mu m

8 \mu m

10 \mu m

1.5 \mu m \phi \text{ CLEAR ON DARK FIELD}

4 \mu m

3 \mu m \phi \text{ CLEAR ON DARK FIELD}

SKETCH A - DIODE UNIT
KETCH B - ORIENTATION & DOT ALIGNMENT MARKS

Dimensions in inches except where noted.
1% PROFILE TEST DOTS
SPACED UNIFORMLY THROUGHOUT MASK

DIMENSIONS IN INCHES

SPACE FILLED WITH DIODE UNIT (SKETCH A)

SKETCH C - PROFILE DOTS
SCOPE

To describe clearing the wafer surface of undesired metal and photoresist.

APPLICABLE DOCUMENTS

Contract No. S8-738203-LV3
Hughes Drawing 3414270 Rev. (C)

REQUIREMENTS

1. Equipment set up in an air conditioned, limited access facility.
   a. Wet chemical fume hood
   b. Hot plate HP 1915B
   c. Microscope 7-30x, Bausch & Lomb
   d. Microscope - 100-800x, Unitron model 6560

2. Chemicals - Electronic grade or equivalent, high purity.
   a. Trichloroethylene
   b. Apiezon hard wax, W
   c. SEM stub
   d. Adhesive mylar tape, 3M
   e. Cotton swabs, 6" long
   f. 50 ml beakers

3. Procedure
   Mount wafer, face up, onto a SEM sample stub.
   a. Heat stub so wax may be melted on the surface.
   b. Place wafer, face up, in wax. Gently apply pressure using swab stick to force out air. Let cool.
   c. Cut a small piece of mylar tape (approximately .2 inches wide x 1 inch long).
   d. Grasp each end of the tape between the thumb and forefinger. Adhesive will stick, each end to a finger. A smooth loop, protruding outward and in plane with the fingers, is the object.
   e. Under the low power microscope, gently and repeatedly contact and pull away the tape from the wafer surface. Some of the undesired metal and resist will pull away with each application and retraction of the tape. Lightly swabbing the surface with a trichloroethylene damped swab will improve the adhesion of the tape. Patience will be required, however, eventually all of the material will be lifted. Use a new piece of tape as required.
f. Remove the wafer from the stub after SEM analysis. Heat the stub to remelt the wax. Slide off, using a tweezer.
g. Hold the wafer in boiling trichloroethylene vapor to complete the wafer cleanup.
h. Place wafer into covered petri dish.

4. Quality Assurance

SEM analysis of the wafer shall be performed during liftoff and before step 3.g. The resist overhang may be examined to ensure that the deposited metal partially coats the sides of the oxide wall. Figure 1 shows the desired coverage.
Figure 1. Metal Coverage.
SCOPE

Describes the process for thinning the wafer by mechanically lapping and polishing of the wafer backside.

APPLICABLE DOCUMENTS

Contract Number S8-738203-LY3
Hughes Drawing 341427C  Rev. (C)

REQUIREMENTS

1. Equipment - setup in an air conditioned, limited access facility.
   a. Wet chemical fume hood
   b. Mazur lapping machine, model 601
   c. Buehler polishing machine, model 48-1553
   d. Lapping, polishing, holding fixture, lab built
   e. Gauge stand, reading in one-ten thousandths
   f. Hot plate, HPA1915B
   g. Pneumatic pressure stand, lab built
   h. Sonic cleaner, Buehler model 75
   i. Microscope General purpose 7-30x Bausch & Lomb

2. Chemicals and Gases and supplies. Electronic or best grade available.
   a. Parafin wax, Gulfwax
   b. Trichloroethelene
   c. Silicon carbide powder, 1000 grit, Buehler
   d. Clorox
   e. Dionized water
   f. Methanol
   g. Nitrogen gas 99.994%
   h. Sundry supplies, - Kimwipes, beakers, filter paper, tweezers, optical paper.

   a. Measure thickness of the wafer utilizing the gauge stand. Record the thickness nearest the wafer center.

4. Mount the wafer face down in parafin wax which is applied to the center post of the lapping fixture.
   a. Lay a sheet of filter paper on the hot plate set at 90 °C. Place the center post of the lapping fixture on the paper. When the side of the post nearest the hot plate is uncomfortably warm, remove it and apply a small speck of wax to the hot surface.
b. Lay the wafer face down in the wax then place a quarter size piece of lens tissue over the wafer.

c. Place the fixture centered under the pressure diaphragm of the pneumatic pressure stand. Lower the post and turn on air supply. This step flattens the wafer to the plane of the lapping fixture.

d. When cool, release the air pressure and remove the lapping fixture. Remove the lens tissue. Swab away excess wax using a cotton swab.

e. Place mounted wafer into the gauge stand. Adjust the dial to read the thickness recorded in step 3a.

5. Lap-grind the wafer to a thickness of 4 mils.

   a. Prepare the lapping machine tray by sprinkling a 1/4 teaspoon amount of grit onto the glass flat. Add deionized water to form a slurry.

   b. Insert the center post of the lapping fixture into the holder. Set the holder into the lapping tray. Move it around by hand to distribute the grit. Then set the speed control to 1/2 speed and turn on the machine. NOTE: Speed of material removal depends on area and distribution of grit. Time required to remove a fixed amount may vary, so check progress often until secure rate is established. Clean the wafer before measuring the thickness. Swab with deionized water. Blow dry using N₂ gas.

6. Polish the wafer to a thickness of 2±0.2 mils

   a. Sonic clean both center post and holder. Make sure no vestige of grit remains.

   b. Prepare the Buehler polishing machine. Ensure that a clean satin polishing cloth is installed on the polishing wheel.

   c. Mix 100 ml of clorox in 400 ml of deionized water. Pour it into a plastic squeeze bottle.

   d. Soak polishing wheel with methanol then deionized water. Turn machine on slow speed and add clorox solution to wheel.

   e. Place polishing fixture onto wheel. Slowly allow the center post to slide into position. Continue adding a small spray of clorox. Allow or cause fixture to turn in your hand as polishing progresses. NOTE: Measure polishing rate periodically. Polishing is purposely slow. 1 mil in 10 minutes is typical for an area of 1 cm². Rinse pad with deionized water before removing fixture. Then rinse and dry wafer before measuring thickness.

   f. When the proper thickness of 2 mils is achieved, remove the wafer from the center post by immersing the post in boiling deionized water. Pour off the water, flood with methanol several times, and flood with trichloroethylene several times. Once again flood with methanol several times. Finish with a 3-minute running hot deionized water rinse. Keep the wafer on the side wall of the beaker during the pour off.

   g. Carefully remove the wafer from the side of the rinse beaker. Lay it flat on a sheet of filter paper and carefully blow the wafer dry using Dry N₂. Place the wafer back into a clean covered petri dish.
7. Quality Assurance

The polished wafer should have a specular appearance, having no surface scratches or roughness.

a. Inspect, microscopically from various angles, utilizing the reflected light from the wafer surface. Magnification from 7-30x is acceptable.
SCOPE

Describes metallization of the cathode contact by vacuum evaporating a gold-germanium-nickel alloy for the contact metal. The alloy coated wafer is heat treated to reduce the contact resistance. Sputtered films of titanium, platinum and gold are then deposited, completing the contact.

APPLICABLE DOCUMENTS

Contract Number 58-738203-LV3
Hughes Drawing 3414270  Rev. (C)

REQUIREMENTS

1. Equipment - setup in an air conditioned, limited access facility.
   a. Wet chemical fume hood
   b. Vacuum evaporator, Veeco model 775
   c. RF sputtering system. Perkin Elmer model 2400
   d. Heat treat furnace, lab built
   e. Hot plate, HPA1915B
   f. Tencor Alpha Step Profiler
   g. Sundry supplies, tri-grip holder, beakers, filter paper, tweezers.
      Microscope slide & coverglass, apiezon blackwax. Thickness sample made from scrap GaAs.

2. Chemicals and gases, electronic grade or equivalent high purity.
   a. Hydrochloric acid
   b. Trichloroethylene
   c. Methanol
   d. Metals refer to PI-6.1
   e. Forming gas mixture, 90% N₂, 10% H₂ purities > 99.99%.
   f. Argon gas, UHP 99.999%
   g. LN₂
   h. Hydrofluoric acid
   i. Techni-strip AU

   a. Prepare vacuum evaporator. Fill cold trap with LN₂. Check pressure < 10⁻⁶ torr.
   b. Weigh out 40 mgs of AuGe alloy and 10 mgs of nickel wire then degrease all in boiling trichloroethylene vapor. Use filter paper cone to contain charges. Transport to vacuum evaporator.
   c. In a hood, pour 50 ml of HCl into a clean 100 ml beaker. Set up a rinse beaker with 200 ml of deionized water.
d. Remove wafer from petri dish; grasp with the tri-grip tweezer. Immerse wafer into HCl for 2 seconds, then rinse in distilled water beaker. Final rinse in running hot deionized water for 3 minutes. Be careful, wafer is fragile.
e. Dry using opposed jet N₂ blow station. Be very careful, wafer is fragile.
f. Place dried wafer into clean petri dish and transport to the vacuum evaporator.

4. Open vacuum chamber
   a. Press stop cycle, system will vent and raise bell-jar automatically.
   b. Remove substrate holder from chamber. Mount wafer under spring clips. Replace substrate holder.
   c. Remove shield.
   d. Place AuGe alloy charge into center tungsten boat. Place nickel charge in farthest boat. Shutter must be closed.
   e. Replace shield.
   f. Press start cycle. System will automatically lower bell-jar and pump down.
   g. Evaporate charges. CAUTION! Use filter glass while observing melt. When system pressure achieves < 10⁻⁶ torr, turn up power in AuGe boat slowly while observing melt. When the tungsten dimple is wetted, open shutter and increase boat power until the charge is evaporated. Close shutter.
   h. Switch boat power to the nickel boat. Increase power while observing melt. When melted, increase power further to 200 amps. while opening shutter. Leave power up for 30 seconds. CAUTION! Use filter glass while observing melt. Close shutter and allow to cool for 5 minutes.
   i. Open system by pressing stop cycle. When system opens, remove substrate holder. Remove wafer from holder and place into clean covered petri dish.

5. Transport wafer to heat treat furnace.
   a. Open forming gas valve and set flow to full scale. Slide furnace tray out of furnace and place the wafer on the tray. Return tray to preheat position.
   b. Reduce forming gas flow to a reading of 5. Allow furnace to purge for 5 minutes.
   c. Push tray into hot zone. Time for 3 minutes, then quickly slide furnace tray to the preheat position.
   d. Remove tray after 15 seconds. Slide wafer onto clean filter paper in petri dish.
   e. Turn off forming gas

6. Transport wafer to RF sputtering system.
   a. Open system by pressing start vent.
   b. Charge cold trap with LN₂ while venting.
c. Open chamber. Place wafer on clean BeO substrate with alloy side up. Also place thickness gauge near wafer.
d. Close chamber. Press start pump. System will automatically pump down.
e. When chamber pressure reads < 10^-6 torr, press start gas and open gas valve. Turn on RF generator. Turn vacuum gauge to position 1. Pressure should stabilize at 20 mtorr in 1 minute or less.
f. Presputter all 3 targets Au, Pt, and Ti at 500 watts RF as follows: Au 2 minutes, Pt 2 minutes and Ti 10 minutes.
g. After 10 minutes of Ti presputter, rotate substrate wafer to coincide with the Ti target. Sputter for 1 minute then rotate table one revolution; sputter again for 1 minute and repeat this for 8 cycles. Film should be % 1000 Å thick.
h. Start PT target, presputter 2 minutes and then rotate substrate to coincide with the PT target. Sputter for 1 minute. Film should be % 500 Å thick.
i. Start Au target, presputter 2 minutes and then rotate substrate to coincide with the Au target. Sputter for 4 1-minute cycles. Film should be % 2000 Å thick.
j. Turn off RF generator. Turn off gas. Press start-stop. When chamber vents, open and remove wafer and place in clean covered petri dish.
k. Close chamber and press start pump.

7. Quality Assurance

A thickness gauge partially masked with a portion of glass cover slip will be placed beside the wafer during the metallization runs. The monitor may be a glass cover slip or a piece of scrap polished GaAs. Selective etching or SEM analysis will be used to determine the thicknesses.

a. Cleave sample and mount on an SEM stub, with cleaved edge up.
b. Etch in 60°C techni-strip Au for 10 seconds. Then rinse in di water for 30 seconds. This delineates Au film. 2000 ± 500 Å
c. Etch in 10% HF for 10 seconds then rinse in di water for 30 seconds. Blow dry using N2 gas. This delineates Ti film. 1000 ± 200 Å
d. Platinum film remains unaffected. 500 ± 100 Å
e. SEM photomicrographs will serve as file data.

OR: If a GaAs Thickness Gauge is used.

a. Mount the piece in blackwax onto a glass slide.
b. Mask off all but a 1 mm strip of metallized area orthogonal to the pre-metallization mask.
c. Etch in 60°C Technistrip to remove the gold metallization. Then rinse in DI water. This creates the gold platinum step.
d. Etch in 10% HF for 1 minute. This etches the titanium under the platinum, creating a platinum titanium step. Then rinse in DI water and N2 blow dry.
e. Remove wax using Trichloroethylene.
f. Step profile the resultant etch steps on the Alpha Step Profiler.
g. Attach the profile data to the run sheet.
SCOPE

To determine the I vs. V characteristic of the diodes and while still in wafer form, determine the diode uniformity across the wafer.

APPLICABLE DOCUMENTS

Contract Number S8-738203-LV3
Hughes Drawing 3414270 Rev (C)

REQUIREMENTS

1. Equipment - set up in air conditioned, RF shielded room.
   a. Curve tracer, Tektronix model 576
   b. Digital voltmeter, Keithley model 191
   c. 22V Battery Supply
   d. Probe station with 1 mil pointed whisker, lab built
   e. Lab built constant current source
   f. Microscope, boom mounted. Rausch and Lomb 7-30x

2. Procedure - Connect equipment la, b, c, and d as shown in Figure 1, constant current source.
   a. Turn Diode switch to curve tracer.
   b. Set max peak volts units to 20 V max
   c. Polarity, NPN
   d. Series resistance, 5 K
   e. Horizontal to .1 V/cm
   f. Vertical to .01 mA/cm
   g. Adjust intensity and focus for clear display
   h. Adjust graticule illumination

3. Place wafer on probe station platform. Perform the measurements on three evenly spaced areas of the wafer, in accordance with the wafer map shown in Figure 2.
   a. Adjust curve tracer sweep to .8 V (8 cm)
   b. Lower whisker probe, adjusting X, Y, Z knobs as needed until whisker contacts one diode, indicated by a vertical jump in the trace.
   c. Further adjust sweep volts until a full scale display is observed.
   d. Switch curve tracer vertical to 1 mA/cm and increase sweep volts to indicate 5 mA of vertical display.
e. Carefully increase or decrease contact pressure while observing curve tracer display. Adjust for steepest slope. CAUTION! Too much downward movement may dislodge the whisker or grossly affect the knee portion of the trace. The knee should remain as sharp as when first contacted in step 3c. Turn sweep volts to zero.

4. Measure and record reverse breakdown.
   a. Switch polarity to PNP
   b. Move sweep start to right side center of screen
   c. Set horizontal to 2 V/cm
   d. Set vertical to 0.1 mV/cm
   e. Turn up sweep volts to display diode breakdown volts when indicating 0.001 mA current.
   f. Position polaroid camera to photograph display, or record voltage displayed on I-V data sheet.
   g. Turn down sweep and turn diode switch to current source.

5. Record forward I-V data
   a. Set current switch to lowest setting ccw, 0.01 microamperes.
   b. Read and record voltage on Keithly model 191 DVM.
   c. Turn current switch to next current, 0.10 microamperes - Repeat step b. for each current setting.
   d. Return current switch to lowest setting and turn diode switch back to curve tracer.
   e. Record the I-V data indicating the man area on 7-cycle semilog graph paper, or enter data into a preprogrammed calculator with printer such as the HP 41C and HP 82143A.
   f. Determine diode quality factor $\eta$, and series resistance $R_s$ from the following equations.

\[
\eta = \left( \frac{\Delta V}{100 \, \mu A} \right) \times \frac{0.0593}{(296/T)}
\]

\[
T = \text{room temperature} \, ^\circ K
\]

\[
R_s = \left( \frac{\Delta V}{1.0 \, mA} - \frac{\Delta V}{100 \, \mu A} \right) \times 1000
\]

If the test results are acceptable, the wafer is now ready for scribing PI-11.
Figure 1. Schematic Diagram - Constant Current Source.
Figure 2. Wafer Map
<table>
<thead>
<tr>
<th>I</th>
<th>V</th>
<th>ΔV</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.1 μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1.0</td>
<td></td>
<td></td>
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<tr>
<td>10.0</td>
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<tr>
<td>100.0</td>
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<tr>
<td>1.0 mA</td>
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</tr>
<tr>
<td>3.16 mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10.0 mA</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Date: ______________________
Wafer No.: _______________
Diode No.: _______________
Temperature: ____________

\[ R_s = \frac{(\Delta V_{1.0 mA} - \Delta V_{100 \mu A}) \times 1000}{n} = \frac{(\Delta V_{100 \mu A}/0.0583) \times (2.96/T)}{T = \text{Ambient temperature, } ^\circ K} \]

\[ V_B = \text{(at 1.0)} \]

[\( V_B \) need not be supplied for all diodes; just for a representative sample]

PI-10

Table 1. Typical I-V Test Data, Hughes 3414271 Rev. (C).
SCOPE

Describes the procedure for dicing the wafer into individual chips

APPLICABLE DOCUMENTS

Contract Number S8-738203-LV3
Hughes Drawing 3144270  Rev (C)

REQUIREMENTS

1. Equipment set up in an air conditioned, limited access facility.
   a. Temperess Automatic wafer scriber model 1713-10C
   b. Hot plate, HPA1915B
   c. Fume hood
   d. Sundry supplies. Parafin wax, glass cover slips, beakers, filter paper, tweezer, plastic storage containers, labels, stainless steel screen, fine mesh.
   e. Microscope, General purpose, 7-30x Baush & Lomb

2. Chemicals and gases electronic grade or equivalent high purity.
   a. Trichloroethylene
   b. Nitrogen gas 99.994%

3. Procedure - Mount wafer to a heated glass cover slip.
   a. Apply parafin wax to cover slip
   b. Place wafer face up in wax
   c. Remove excess wax using trichloroethylene
   d. Remelt wax to form a bead around wafer edge

4. Place mounted wafer on scriber chuck.
   a. Turn on machine power
   b. Turn on vacuum
   c. Set mode to index, and spacing to .015
   d. Align scribe streets with cross hair in eyepiece
   e. Translate the wafer well to the left of the scribe point
   f. Adjust the point height to just touch the cover slip. Manually cycle once to determine planarity. If not in plane, adjust accordingly.
   g. Increase the scribed point height 1 to 1.5 mils
   h. Reposition wafer to align its scribe street with point
i. Begin scribe stroke. Single stroke operation is recommended to avert catastrophe. When one axis is completed, rotate stage 90° and repeat the operation. Blow clean occasionally using N₂ gas.

5. Remove wafer from machine.
   a. Blow dust off surface using N₂ gas
   b. Carefully dissolve wax from wafer by soaking in trichloroethylene. Pour off several times after the wafer comes free of the cover slip.

6. Break into chips.
   NOTE: This procedure is temporary
   a. Place wafer scribed side up between halves of a folded sheet of lens tissue.
   b. Grip tissue, keeping it taut and trapping the wafer
   c. Pass the underside of the tissue over a sharp, smooth edge of an aluminum block. Use just enough pressure to break the wafer. Remember to keep tissue taut. Then rotate the tissue 90° and repeat.
   d. Rinse the chips in methanol over a fine stainless steel screen to remove particulate matter.
   e. Oven dry 85 °C for 10 minutes

7. Quality Assurance
   a. Pour chips into a clean covered box
   b. Inspect chips for poor edges, cracks, flaking of back metallization or other obvious flaws.
   c. Label container