Variable-ratio power splitters using computer-generated planar holograms on multimode interference couplers

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Received November 4, 2008; revised December 11, 2008; accepted January 3, 2009; posted January 15, 2009 (Doc. ID 103662); published February 12, 2009

Variable-ratio power splitters using computer-generated planar holograms on multimode interference couplers are analyzed. The coherent wave at the device input is transformed to the desired output using numerically calculated refractive index perturbations on multimode channel waveguides at half the beat length. Devices are fabricated on the silicon-on-insulator platform and characterized at a wavelength of 1.55 μm. Power-splitting ratios are varied by changing the hologram etch depth and the hologram length.

OCIS codes: 130.3120, 130.2790, 090.1760.

Optical interconnects based on thin computer-generated holograms (CGHs) using free-space optics have been shown to be a highly versatile technology for guiding optical signals [1]. However, these systems suffer from low diffraction efficiency in comparison with optically recorded volume holograms. The recent advances of micro and nanofabrication technologies have allowed the realization of highly complex patterns on planar lightwave circuits. Coupling the new fabrication capability with the rapid advance of computing power, it is now possible to calculate and fabricate a refractive index distribution as a hologram on a waveguide [2]. This class of integrated optical components based on the concept of computer-generated planar holograms (CGPHs) on planar optical platforms has unique refractive index distributions as a CGH to transfer a coherent optical input light pattern to a desired optical output pattern with high efficiency. In contrast to the common single-mode waveguide structures, for wavefront manipulation in guided-wave optics, it is necessary to have more than one guided mode in the guiding structure. Using computer-generated index perturbations in the guiding structure, the modes excited by the input light pattern are mixed and transformed to generate the desired output light pattern. A similar concept has been applied in long-period-fiber gratings in which the light in the guided mode is coupled to the cladding modes of a single-mode fiber through a grating [3]. Recently, it has been proposed that the modes in a waveguide array can be coupled through long-period gratings to perform broadband coupling functionalities [4]. Another approach using index perturbations on planar waveguides to match the input and the output wavefronts has also been demonstrated [5,6].

Multimode planar waveguides have interesting self-imaging properties [7]. These multimode interference (MMI) couplers [7] are particularly attractive for power splitter applications because of their large fabrication tolerance, large bandwidth, and compact size [8]. For MMI-based power splitters, changes in device geometry [9] or configuration [10] are often required to obtain different splitting ratios. In the past [11], we have demonstrated that CGPHs on MMI-type devices can be used to perform unitary optical operations, such as mode-order conversion [12] and Hadamard transformation [13]; we also demonstrated numerically that an arbitrary splitting ratio can be obtained by changing the CGPH pattern on a fixed-dimension MMI coupler [14]. These results illustrate the design versatility and functionality enabled by CGPHs. In this Letter, we present the design and the fabrication of variable splitting ratio 2 $\times$2 MMI couplers based on the principle of CGPHs.

The CGPH devices are fabricated using passive waveguides on commercially available 100 mm silicon-on-insulator (SOI) wafers with a 3 μm Si layer and a 1 μm buried oxide layer. We choose an SOI rib waveguide structure with a large mode cross section for its lower coupling loss to optical fibers. For the MMIs, the width of the multimode section W_{MMI} is 24 μm, the length L of the multimode section is half the beat length at 1080 μm, and the width of the access waveguides is 4 μm as shown in Fig. 1. The MMI supports a single mode in the longitudinal direction and eight modes in the transverse direction. The centers of the access waveguides are placed ±4.3 μm from the center of the multimode section for paired imaging [7]. S bends are incorporated in the design to separate the ports at the edge of the chips. Without a CGPH, the MMI functions as a fixed ratio power splitter with a 50:50 splitting ratio.

The CGPH is designed using the eigenmodes at paired-imaging planes as in [14]. Following the procedures in [14], the output field amplitudes in both output ports are related to input ports by $\mathbf{V}(L)=\mathbf{T}\exp(-i\mathbf{K}L_H)\mathbf{H}\mathbf{V}(0)$. $\mathbf{T}$ is the transfer matrix representing the MMI without the CGPH, L_H is the hologram length, and

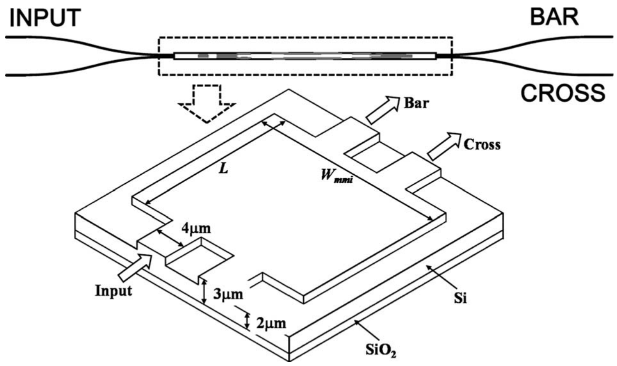

Fig. 1. Top, schematic of the 2×2 CGPH power splitter on SOI. Bottom, dimensions of the power splitter.

$$\mathbf{K} = \begin{bmatrix} 0 & \kappa \\ \kappa & 0 \end{bmatrix}, \quad (1)$$

where κ represents the coupling coefficient; its magnitude is on the order of $(2\pi/\lambda)(\Delta n/n_c)$ [11]. For a single input port, the output power at bar and cross ports can be calculated from $\mathbf{V}(L)$ as

$$\text{bar:}\tfrac{1}{2}(1+\sin 2\kappa L_H), \quad (2)$$

$$\text{cross:}\tfrac{1}{2}(1-\sin 2\kappa L_H). \quad (3)$$

From Eqs. (2) and (3), it is obvious that an arbitrary power-splitting ratio can be obtained by varying κ via index modulation Δn or by varying the hologram length L_H while maintaining the dimensions of the MMI. We calculate the CGPH using a two-dimensional wide-angle beam-propagation method (WA-BPM) [15] with the effective index corresponding to TE polarization of the device. The calculated CGPH is then converted to a binary pattern for fabrication.

The fabrication is a two-step process involving separate patterning and alignment of the CGPH layer and the MMI layer. First, we pattern 1-μm-deep global alignment marks on the chip for both layers using the electron beam (e-beam) lithography and a reactive ion etching (RIE) system with an SF_6/O_2 chemistry. The global marks are necessary because it is difficult to align the MMI patterns to the shallow etched CGPH patterns. The CGPH is aligned to the global marks, patterned using the same e-beam system, and transferred to Si with the same RIE. The etch depth d_{etch} for the CGPH is varied from 130 to 260 nm to change the power-splitting ratio of the devices; d_{etch} is directly related to the magnitude of the effective index modulation Δn and can be estimated by the effective index method [16]. Then, the MMIs are patterned and aligned to the CGPH layer via the global marks using a contact aligner and transferred to Si with the same RIE system. The etch depth for the MMI patterns is 1 μm. The final processing steps of the fabrication involve cleaving the chips to obtain optical quality facets for test and measurement.

Devices with a different etch depth and hologram length are fabricated. Figure 2 shows a section of a fabricated device and scanning electron microscope (SEM) micrographs. These devices are measured with a cw laser at a wavelength of 1.55 μm with TE input polarization. Light is coupled into the input and out of the bar and cross ports shown in Fig. 1 via tapered fibers. The typical insertion loss of the measured devices is between 13.5–14.8 dB, including an estimated fiber-coupling loss of 4.5 dB/facet. The MMI without CGPHs functions as a 50:50 power splitter as designed. As predicted by the theoretical calculations and numerical simulations in [14], the power-splitting ratio of fixed-dimension 2×2 MMI couplers can be varied by changing the CGPH etch depth and the CGPH length, as shown in Fig. 3. There are discrepancies between the measured splitting ratios and the predicted splitting ratios by the analytical calculations in Eqs. (2) and (3). This is due to the difference between the binary pattern used in the fabrication and the smooth refractive index modulation assumed in the analytical calculations. Using the WA-BPM model, we simulated the splitting ratios using the binary CGPH pattern used in the fabrication. The effective index modulation Δn's in the simulation are −0.005, −0.010, −0.015, and −0.002, which correspond to etch depths of approximately 130, 200, 260, and 300 nm in the SOI mate-

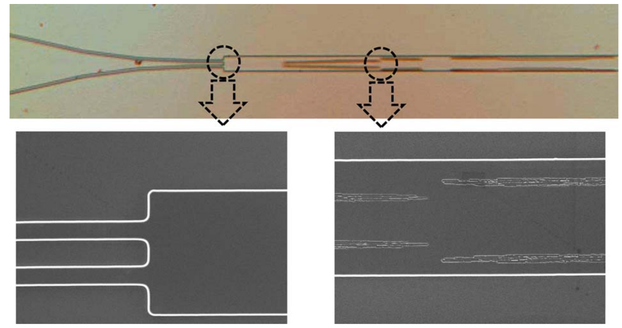

Fig. 2. (Color online) Section of the fabricated 2×2 CGPH power splitter. Insets show SEM micrographs of the device.

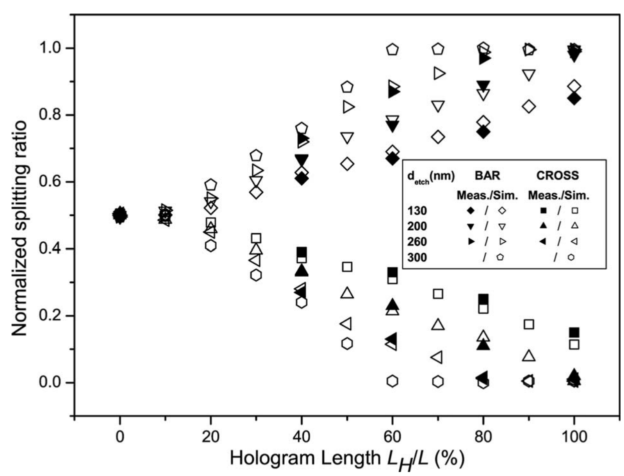

Fig. 3. Normalized splitting ratio (Meas.) of the fabricated devices with different etch depth d_{etch} and hologram length L_H at $\lambda=1.55$ μm with TE polarization. Also shown are simulated splitting ratios (Sim.) of devices with various effective index modulations corresponding to the different etch depths.

rial system used in the fabrication. As shown in Fig. 3, the simulated splitting ratios and the experimental results agree quite well.

In summary, a new class of power splitters using CGPHs on 2×2 MMI couplers has been realized in SOI. Based on the principles of CGPHs, these devices allow a free selection of the splitting ratio while maintaining a fixed device dimension. Many different splitting ratios have been realized. The experimental results are compared with the computer simulation based on the WA-BPM algorithm. There is a fairly good agreement between the experiment and the simulation.

This material is based upon work supported in part by the Science and Technology Center Program of the National Science Foundation (NSF) under agreement DMR-0120967 and by a Defense Advanced Research Projects Agency (DARPA) program. S.-Y. Tseng's work is supported by the National Science Council of Taiwan (NSCT) under contract NSC97-2218-E-006-281-.

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