High-performance InGaZnO thin-film transistors with high-k amorphous Ba0.5Sr0.5TiO3 gate insulator

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High-performance InGaZnO thin-film transistors with high-*k* amorphous $Ba_{0.5}Sr_{0.5}TiO_3$ gate insulator

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We report on high-performance *n*-channel thin-film transistors (TFTs) fabricated using amorphous indium gallium zinc oxide (*a*-IGZO) and amorphous $Ba_{0.5}Sr_{0.5}TiO_3$ (*a*-BST) as the channel and gate dielectric layers, respectively. *a*-BST/*a*-IGZO TFTs achieve low-voltage operation with a high saturation mobility value of 10 ± 1 cm^2/V s, excellent subthreshold slopes of 0.06 ± 0.01 V/decade, a low threshold voltage of 0.5 ± 0.1 V, and a high on-off current ratio up to 8×10^7 ($W/L = 1000\ \mu$m/5 μm) at 3 V. The high capacitance density of *a*-BST (145 ± 2 nF/cm^2) and the small contact resistance, smaller than the channel resistance, are responsible for the high performance of these TFTs. © *2008 American Institute of Physics*. [DOI: 10.1063/1.3054335]

Recently, transparent oxide-based thin-film transistors (TFTs) have attracted much attention because of their high electron mobilities (>10 cm^2/V s) and because they can be processed at low temperatures to produce large-area displays with the potential of low production costs.[1] However, large operating voltages are often required to achieve high mobility and high on-off current ratio in such TFTs. For circuit applications, such as inverters, ring oscillators, and backplane circuits for mobile displays, low-voltage and high-frequency operations are desirable. For low-voltage operation, small threshold voltage (V_T), small subthreshold slope (S), and high on-off current ($I_{\text{on-off}}$) ratios need to be achieved. Consequently, TFTs that exhibit high mobility with a high capacitance density are desirable. Recently, a ZnO-based TFT using Mg-doped $Ba_{0.5}Sr_{0.5}TiO_3$ (BST) gate insulator on a polyethylene terephthalate (PET) substrate was fabricated at low temperatures.[2] This TFT showed a field-effect mobility of 16.3 cm^2/V s, subthreshold slope of 0.4 V/decade, and on-off current ratio of 6.4×10^4 at 6 V. However, ZnO films are polycrystalline even when deposited at room temperature. This leads to channels with grain boundaries that deteriorate the TFT stability, uniformity, and performance of its electrical characteristics.[3] In contrast, indium gallium zinc oxide (IGZO) films deposited by physical vapor deposition or rf-magnetron sputtering show an amorphous nature. Using Y_2O_3 ($\varepsilon_r \sim 14$)[4,5] as gate dielectric, high-performance amorphous-IGZO (*a*-IGZO)-based TFTs have been reported, with electron mobilities over 10 cm^2/V s, $V_T = 1.4$ V, and $S = 0.20$ V/decade. Despite operating below 6 V, the low V_{DS} region on these TFTs shows strong nonlinear effects that are commonly associated with a source-drain contact resistance (R_c) limited behavior. The source-drain contact resistance effectively limits the maximum transconductance, $g_m = \partial I_{DS}/\partial V_{GS}$, attainable at a given mobility and channel length, therefore increasing the subthreshold slope $S = [\partial(\log I_{DS})/\partial V_{GS}]^{-1}$ and decreasing the cutoff frequency $f_T = g_m/2\pi C_{\text{gate}}$. Therefore, R_c is the limiting factor to achieve low-voltage and high-frequency TFT operation.

In this paper, we report on the use of a high-*k*, amorphous $Ba_{0.5}Sr_{0.5}TiO_3$ (*a*-BST), gate dielectric to produce high-performance *n*-channel TFT driven by an *a*-IGZO channel layer. These TFTs combine a high mobility of 10 ± 1 cm^2/V s, low V_T of 0.5 ± 0.1 V, and $I_{\text{on-off}}$ current ratio up to 8×10^7 at low operating voltages (<3 V). We also demonstrate that g_m in these TFTs is not limited by R_c in the linear and saturation regions in devices with channel lengths ranging from 100 μm down to 5 μm. The negligible contribution of R_c allows to achieve extremely small subthreshold slopes $S = 0.06 \pm 0.01$ V/decade, opening the potential for low-voltage and high-frequency TFT operation.

In this work, TFTs were fabricated with a bottom-gate and top-contact source and drain electrodes. First, indium tin oxide (ITO) on a glass substrate was cleaned and used as the common gate electrode. A 170 nm thick *a*-BST gate dielectric layer was deposited onto the ITO on glass substrate by rf sputtering without substrate heating using a power of 150 W, a working pressure of 5 mTorr, and an O_2/Ar (6/4) atmosphere. A 30 nm thick *a*-IGZO (Ga_2O_3:In_2O_3:ZnO = 1:1:2 mol %) active layer was then deposited by rf sputtering at room temperature and using a power of 125 W, a working pressure of 5 mTorr, and an O_2/Ar (1/10) atmosphere. After deposition of the *a*-IGZO layer, the device was annealed at 325 °C for 30 min in air. To define the channel, *a*-IGZO layer was patterned by wet-etching process using hydrochloric acid (HCl:H_2O = 100:1) diluted in de-ionized water. To provide access to the gate electrode, *a*-BST was selectively patterned using hydrofluoric acid (HF:H_2O = 10:1). Then, Ti (6 nm) and Au (120 nm) were sequentially e-beam deposited and patterned by lift-off process to form the source and drain electrodes, creating a total overlap area of 1.462×10^{-3} cm^2 with the gate electrode.

Although BST is a well-known high-*k* dielectric in its polycrystalline phase, the voltage-dependent dielectric constant characteristics that make it attractive for dynamic random access memories and tunable microwave devices[6] are less desirable to achieve low-voltage and high-frequency operating TFTs. In contrast with its polycrystalline phase, which requires high deposition temperatures, *a*-BST films

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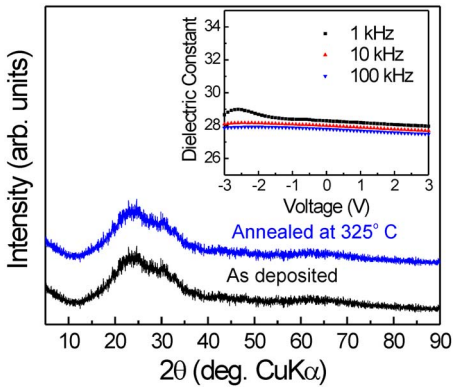

FIG. 1. (Color online) XRD patterns of *a*-BST film on glass substrate as deposited at room temperature and after annealing at 325 °C for 1 h. Inset: Dielectric constant measured on a Au/Ti/*a*-BST/ITO/glass sample as a function of bias voltage and at 1, 10, and 100 kHz.

can be fabricated using rf sputtering at room temperature. Figure 1 shows x-ray diffraction (XRD) patterns confirming the amorphous nature of the BST films right after room temperature deposition and after annealing for 1 h at 325 °C in air. While the dielectric constant of the amorphous phase (ε_r=28) is smaller than that of the polycrystalline phase (ε_r>100),[7] *a*-BST shows no appreciable dielectric tunability. The inset of Fig. 1 shows that the dielectric capacitance measured in Au(120 nm)/Ti(5 nm)/*a*-BST(170 nm)/ITO/glass samples using an Agilent 4284A *LCR* meter decreases only by 3.0% with frequencies ranging from 1 to 100 kHz and bias voltages between −3 and 3 V. This behavior is consistent with BST's amorphous nature and also is indicative of a low defect concentration.[6,7] In these samples, the capacitance density is estimated to be 145 nF/cm^2 with breakdown field values of 1.4 MV/cm or higher. The leakage current densities were highly asymmetric due to the different electrodes (ITO bias electrode and Ti/Au ground electrode) with values of $<10^{-7}$ and 1×10^{-4} A/cm^2 at bias voltages of −3 and +3 V, respectively. Therefore, *a*-BST combines a large voltage and frequency independent dielectric constant which is desirable for the fabrication of *a*-IGZO-based TFTs with a large capacitance density.

Several *a*-BST/*a*-IGZO TFTs were fabricated using a channel width of W=1000 μm and channel lengths ranging from 100 to 5 μm. Figure 2 shows the measured transfer and output characteristics of the *a*-BST/*a*-IGZO TFT with a W/L=1000 μm/5 μm. The output characteristics (drain current I_{DS} versus drain-source voltage V_{DS} at multiple constant gate-source voltages V_{GS}) and transfer characteristics (I_{DS} versus V_{GS} at fixed V_{DS}) of the TFTs were measured using an Agilent E5272A medium-power source/monitor unit connected to a probe station. The saturation mobility (μ) and threshold voltage (V_T) were derived from a linear fitting to a $(I_{DS})^{1/2}$ versus V_{GS} plot (I_{DS} is the source-to-drain current, V_{GS} the gate-to-source voltage) using the equation

$$I_{DS}=(\mu\varepsilon_0\varepsilon_r W/2Ld)(V_{GS}-V_T)^2, \quad (1)$$

where W is the channel width, L is the channel length, ε_0 is the free-space permittivity, ε_r is the relative dielectric constant of the gate insulator (ε_r=28 for *a*-BST), and d is the thickness of the gate insulator. The subthreshold slope (S) was extracted from the linear portion of a $\log(I_{DS})$ versus V_{GS} plot. All *a*-BST/*a*-IGZO TFTs exhibited *n*-channel transistor behavior with saturation mobilities of 10 ± 1 cm^2/V s, operating in the enhancement mode, with excellent subthreshold slopes of 0.06 ± 0.01 V/decade, low threshold voltages (0.5 ± 0.1 V), and a high on-off current ratio up to 8×10^7 at 3 V (W/L=1000 μm/5 μm). The average values and standard deviations were calculated from the measurements of 20 devices with 4 devices per given channel length. The leakage current $|I_G|$ as a function of V_G was also measured at V_{DS}=0 V. As shown in Fig. 2, even in these common gate devices, the leakage current in the off region is around 10^{-10} A and that in the on region does not contribute more than 0.1% to the signal current. Further reduction in the leakage currents can be achieved by pattering the gate electrode.

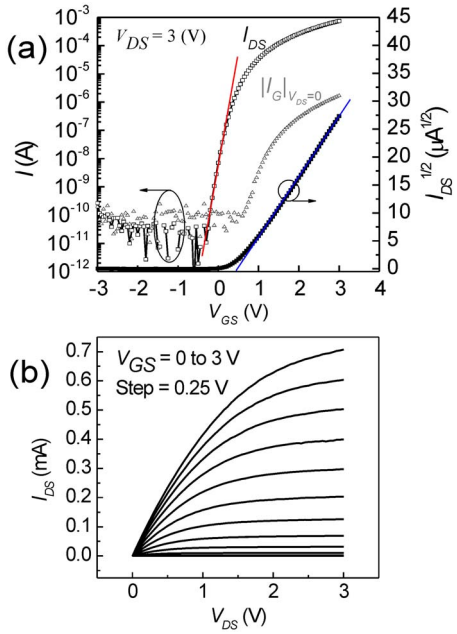

FIG. 2. (Color online) Operation characteristics of sputtered *a*-BST/*a*-IGZO TFT with L=5 μm and W=1000 μm. (a) Transfer characteristics (squares) V_{GS} was swept from −3 to +3 V at V_{DS}=3 V and leakage current (triangles) at V_{DS}=0 V. (b) Output characteristics. V_{DS} was swept from 0 to +3 V at each V_{GS} varied from 0 to 3 V at 0.25 V steps.

Unlike organic or *a*-Si TFTs, very little experimental work has been reported on the source-drain contact resistance, R_c effects on oxide TFTs. In short channel *a*-IGZO TFTs, contact resistance effects can limit the electrical performance by decreasing the field-effect mobility (μ_{FE}).[8–10] Therefore, even in top-contact bottom gate oxide-based TFTs, it is important to quantify the influence of R_c on the overall electrical performance. As previously mentioned, R_c decreases μ_{FE} which in turn limits the maximum g_m attainable in a TFT with a given intrinsic mobility and channel length. In the absence of contact resistance effects, in the linear and saturation regions $g_m \propto \mu C_{gate} WL^{-1}$. Figure 3(a) shows that g_m, calculated as its maximum value as a function of V_{GS}, follows the expected L^{-1} dependence in TFTs down to 5 μm channel lengths. This behavior is only explained if μ remains constant as a function of L, its standard deviation is around 10% in both regions, since as shown in the inset of Fig. 1, C_{gate} is voltage independent. The very small S values can then be explained by a large C_{gate} and by the fact that g_m does not seem to be limited by contact resistance effects. Furthermore, following the transmission line method,[11,12] the

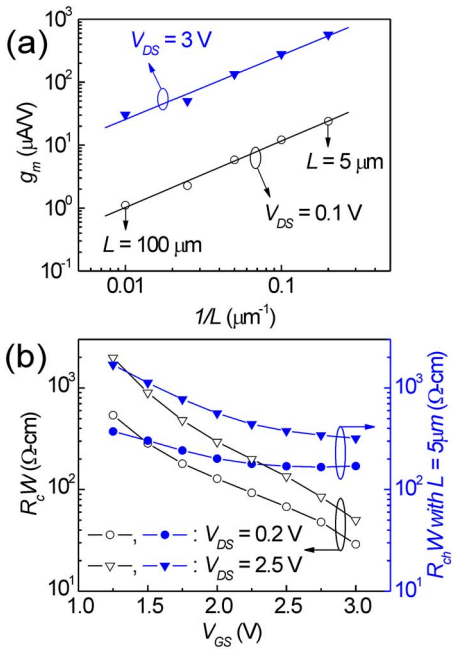

FIG. 3. (Color online) (a) Transconductance (g_m) vs inverse of channel length ($1/L$) in the linear (V_{DS}=0.1 V) and saturation (V_{DS}=3 V) regions for a-BST/a-IGZO TFTs. (b) Width-normalized contact resistance (R_cW) as a function of channel length ranging from 5 to 100 μm and width-normalized channel resistance ($R_{ch}W$) at a channel length of 5 μm in the linear (V_{DS}=0.2 V) and saturation (V_{DS}=2.5 V) regions for a-BST/a-IGZO TFTs.

total device resistance can be expressed as $R_{on}=R_c+R_{ch}$, where R_{ch} is the channel resistance. By plotting R_{on} versus L at different gate voltages, R_c was estimated as the ordinate extrapolated for a zero channel length. The width-normalized contact resistance (R_cW) of a-BST/a-IGZO TFTs is then extracted for a channel width of 1000 μm and channel lengths ranging from 5 to 100 μm. In the linear (V_{DS}=0.2 V) and saturation (V_{DS}=2.5 V) regions, R_cW was compared with the width-normalized channel resistance ($R_{ch}W$) on 5 μm channel length TFT and at different gate voltages. Figure 3(b) shows that even if in the saturation region R_c and R_{ch} are larger than in the linear region due to channel pinchoff at the drain contact,[12] in both regions $R_{ch}W > R_cW$ above V_{GS} =1.5 V and at V_{GS}=3 V, $R_cW < 50$ Ω cm represents <20% of $R_{ch}W$. Studies are underway to determine the origin of the very small contact resistance observed in our devices. However, it is expected that the major contribution to R_c comes from the bulk a-IGZO layer rather than from the a-IGZO/source(drain) interface.[8–10]

In summary, we have demonstrated high-performance top-contact bottom-gate n-channel a-IGZO TFTs that use a 170 nm thick a-BST (ε_r=28) as a gate dielectric material. a-BST films deposited at room temperature by rf sputtering show negligible frequency and voltage dependence. With a high gate dielectric capacitance density of 145 nF/cm^2, a-BST/a-IGZO TFTs show high saturation mobility values of 10 ± 1 cm^2/V s, low threshold voltages of 0.5 ± 0.1 V at 3 V, and on-off current ratios up to 8×10^7. The very low source-drain contact resistance <50 Ω cm at 3 V obtained in these TFTs allows for very small subthreshold slopes of 0.06 ± 0.01 V/decade and a channel length independent mobility which does not limit the transconductance and potentially allows for TFTs capable of low-power and high-frequency operation.

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