Low-voltage flexible organic complementary inverters with high noise margin and high dc gain

Xiao-Hong Zhang, William J. Potscavage, Seungkeun Choi, and Bernard Kippelen

Citation: Appl. Phys. Lett. 94, 043312 (2009); doi: 10.1063/1.3077025
View online: http://dx.doi.org/10.1063/1.3077025
View Table of Contents: http://apl.aip.org/resource/1/APPLAB/v94/i4
Published by the American Institute of Physics.
Low-voltage flexible organic complementary inverters with high noise margin and high dc gain

Xiao-Hong Zhang, William J. Potscavage, Jr., Seungkeun Choi, and Bernard Kippelen

Center for Organic Photonics and Electronics (COPE), School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, Georgia 30332, USA

(Received 11 December 2008; accepted 9 January 2009; published online 29 January 2009)

We report on flexible organic complementary inverters using pentacene and C60 as active semiconductors fabricated on a plastic substrate. Individual transistors as well as inverters show good operational stability with negligible hysteresis. The threshold voltages are comparable for p-channel pentacene and n-channel C60 organic field-effect transistors, and noise margins larger than 80% of the maximum theoretical values were obtained at a supply voltage V_{DD} as low as 3 V. A high dc gain of 180 was achieved at V_{DD}=5 V. The inverters demonstrated good mechanical stability when tested after bending under both tensile and compressive stress. © 2009 American Institute of Physics. [DOI: 10.1063/1.3077025]

Driven by the demands for low-cost, large-area, and flexible devices, complementary organic-based circuits are attracting more attention due to their high power efficiency and operation robustness. Previous demonstrations of organic complementary circuits often showed high operating voltage,8 low noise margins,9 low dc gain, and electrical instability such as hysteresis and threshold voltage shifts.8,9 To date, two major obstacles have been hindering the development of organic complementary circuits, which are as follows: the lack of high-performance n-channel organic field-effect transistors (OFETs) and the challenge of integrating both n- and p-channel OFETs on the same substrate while maintaining high performance.10

In this paper, we report on flexible low-voltage organic complementary inverters with both high noise margins and high dc gains using pentacene and C60 as active semiconductors. In our recent work, we have demonstrated low-voltage C60 n-channel OFETs with good electrical stability and low contact resistance.11 To maintain operational stability for inverters, the interface of the gate insulator Al2O3 needs to be passivated with a smooth, trap-free dielectric layer that is stable for both n-channel and p-channel transistors. In recent studies, we have found that a thin passivation layer of polyvinyl alcohol (PVA) provides high performance and good electrical stability not only for C60 OFETs (Ref. 12) but also for pentacene OFETs.

The complementary inverters were built on a 75 μm thick polyethylene naphthalate (PEN) substrate. Before use, the PEN film was shrunk by thermal annealing at 130 °C for several hours in a vacuum oven. The inverters were fabricated in a top-contact configuration, as shown in Fig. 1(a), with connections between transistors leading to the corresponding circuit schematics shown in Fig. 1(b). Source/drain electrodes of Au for p-channel and Ca for n-channel transistors were selected to minimize the contact resistance. A 50 nm thick layer of Au with a 10 nm thick layer of Ti was deposited using an e-beam deposition system and served as a common gate (G_{n,p}) for both n- and p-channel OFETs. This common gate also serves as the input (V_{IN}) node of the inverter. A 200 nm thick Al2O3 gate insulator was formed by atomic layer deposition at 100 °C as described elsewhere.13 To better control the interfacial properties at the dielectric and C60/pentacene, the Al2O3 dielectric surface was coated with a thin layer of PS to passivate the polar groups and impurities at the interface. PS films were spin coated from a 4 mg/ml solution in toluene and annealed at 120 °C on a hot plate for 1 h. After coating with PS, the dielectric surface turned hydrophobic with a water contact angle of 88°. The capacitance density C_{OX} was 26.5 nF/cm², measured from parallel-plate capacitors with 12 varying contact areas.

C60 (Alfa Aesar) and pentacene (Sigma-Aldrich) were purified by thermal gradient zone sublimation prior to deposition. The C60 (50 nm) and pentacene (50 nm) layers were deposited at rates of 0.3 and 1 Å/s, respectively. The top-contact source/drain electrodes with Au (60 nm) for p-channel and Ca (150 nm) for n-channel OFETs were deposited at a rate of 1 Å/s. The substrates were held unheated during all the deposition processes with a chamber pressure below 5 × 10⁻⁶ Torr. The semiconductor layers and source/drain contacts were patterned by a set of shadow masks. A photograph of the flexible inverters is shown in Fig. 1(c). As shown in the circuit diagram in Fig. 1(b), the drain terminals of the two OFETs (D_{n,p}) were connected to form the output

FIG. 1. (Color online) (a) Schematics of the complementary inverter built on a PEN substrate with pentacene and C60, as active semiconductors. (b) Corresponding inverter circuit diagram. (c) Photograph of the inverters under tensile stress (transistors on the outer bent surface).

---

Author to whom correspondence should be addressed. Electronic mail: kippelen@ece.gatech.edu. Tel.: 404-385-5163. FAX: 404-385-5162.

10.1063/1.3077025

© 2009 American Institute of Physics

94, 043312-1

0003-6951/2009/94(4)/043312/3/$25.00
node ($V_{OUT}$) of the inverter. A supply voltage ($V_{DD}$) was applied to the source of $p$-channel OFETs ($S_p$), while a low power supply ($V_{SS}=0$ V in this case) was applied to the source of $n$-channel OFETs ($S_n$). The electrical measurements were performed in a nitrogen glovebox ($O_2, H_2O <0.1$ ppm) at normal pressure (1 atm) in the dark using an Agilent E5272A source/monitor unit and an Agilent E3647A dc output power supply.

The current-voltage characteristics of both $p$- and $n$-channel OFETs are shown in Figs. 2(a)–2(d). The output characteristics exhibit good ohmic-contact behavior for both $p$-channel [Fig. 2(a)] and $n$-channel OFETs (Fig. 2(c)] with $I_{DS}$ increasing linearly with $V_{DS}$ in the linear regime. The transfer curves were measured for both forward and reverse gate biases as shown in Fig. 2(b) ($p$-channel) and Fig. 2(d) ($n$-channel). No threshold voltage shift or hysteresis was observed in either type of transistors, demonstrating good electrical stability with PS at the gate dielectric interface for both hole and electron transports. Field-effect mobilities $\mu$ and threshold voltages $V_T$ were calculated in the saturation regime defined by standard metal-oxide-semiconductor FET models by fitting the $\sqrt{I_{DS}}$ versus $V_{GS}$ data to a square law model. Also extracted from the transfer characteristics are subthreshold slope ($S$) and maximum channel on-current [$I_{DS(max)}$]. The extracted electrical parameters [$\mu$, $V_T$, $S$, and $I_{DS(max)}$] (calculated from forward bias scans) are summarized and compared in Table I. $C_{eo}$ $n$-channel transistors show similar performance as the devices fabricated on rigid substrates$^1$ with a high mobility of 2.17 cm$^2$/V s, a low threshold voltage $V_T$ of 2.1 V, and a sharp subthreshold slope $S$ of 0.3 V/decade. The pentacene $p$-channel transistors show threshold voltage of $-2.7$ V and a subthreshold slope of 0.2 V/decade, which are comparable to those of C$_{60}$ transistors. However, the hole mobility is about six times lower than the electron mobility (2.17 cm$^2$/V s). The lower mobility of pentacene (0.33 cm$^2$/V s) compared to $C_{60}$ was partially compensated by having a channel width of the $p$-channel OFET ($W=4030$ $\mu$m) four times larger than that of the $n$-channel transistor ($W=1030$ $\mu$m). A channel length $L=70$ $\mu$m was used for both devices.

With low threshold voltages for both transistors, the inverters could be operated at a supply voltage as low as 3 V. The voltage transfer characteristics (VTCs) with a supply voltage of $V_{DD}=3$, 4, and 5 V are shown in Fig. 3(a). The switching voltage $V_M$ were obtained graphically from the intersection of the VTC with the line $V_{OUT}=V_{IN}$ ($V_{OUT}$ denotes output voltage and $V_{IN}$ denotes input voltage). $V_M$ values are 2.4, 2, and 1.6 V corresponding to $V_{DD}=5$, 4, and 3 V. These numbers are very close or equal to the maximum theoretical values of 0.5 $V_{DD}$, showing a good symmetry of VTC due to the comparable threshold voltages in individual $n$- and $p$-channel transistors. The noise margin was characterized by the negative slope criteria.$^{14}$ The noise margin low (NM$_L$) and noise margin high (NM$_H$) are 2.0 and 2.3 V for $V_{DD}=5$, 1.7, and 1.8 V for $V_{DD}=4$ V, and 1.2 and 1.2 V for $V_{DD}=3$ V. Those values are higher than 80% of the maximum theoretical values of the noise margins (NM$_{L}=$NM$_{H} = 0.5V_{DD}$). These results are believed to be among the highest noise margin values obtained in organic complementary inverters. The maximum dc voltage gain, defined as $dV_{OUT}/dV_{IN}$, is dependent on $V_{DD}$, as shown in Fig. 3(b). A high dc gain of 180 was achieved with $V_{DD}=5$ V. The $V_{IN}$ values at the highest dc gains correspond to $V_M$ values obtained in Fig. 3(a).

The inverters were subjected to bending experiments to test their stability under flexing. They were tested before bending (test 1), tested again after bending under a tensile stress (test 2, devices on the outer bent surface), and then tested after bending under a subsequent compressive stress (test 3, devices on the inner bent surface). During each bending test, the samples were bent at a radius $R=5$ $\text{mm}$, held in that position for 5 s, and released. This cycle was repeated five times. Since the thickness of the gate dielectric is negligible compared with the thickness $D$ of the substrate film ($D=75$ $\mu$m), a strain $\varepsilon=0.75\%$ for a bending radius of $R=5$ $\text{mm}$ can be approximated from the value of $D/2R$. The changes to the transfer characteristics of individual OFETs induced by the bending are shown in Fig. 4(a).

![FIG. 2. (a) Representative output and (b) hysteretic transfer curves for pentacene $p$-channel OFETs. (c) Representative output and (d) hysteretic transfer curves for $C_{eo}$ $n$-channel OFETs.](image1)

![FIG. 3. (Color online) (a) VTCs of a static organic complementary inverter. (b) Corresponding calculated dc gain values.](image2)
saturation current for the pentacene p-channel OFET decreased by only 0.6% after the tensile strain but increased by 4% after the compressive strain. This observation agrees well with the report of Yang et al.\textsuperscript{14} report on bending-stress-driven transitions in pentacene thin films. On the other hand, the n-channel saturation current increased both with the tensile and compressive strains by 8% and 13%, respectively. With these changes in the individual transistors, the VTC of the inverter shifted by a negligible value of 0.6% under the tensile strain and by a small fraction of 3% under the compressive strain [Fig. 4(b)]. Accordingly, the maximum dc gain increased by 11% and 20%, respectively.

In summary, we have demonstrated organic flexible inverters with both high noise margin and high dc gain at low supply voltage. With the surface of gate dielectrics passivated using a thin layer of PS, both n-channel and p-channel OFETs show negligible hysteresis and comparable threshold voltages. The inverters can be operated at a supply voltage as low as 3 V with noise margin values higher than 80% of their maximum theoretical values. A high dc gain of 180 was obtained at a supply voltage of 5 V. The performance of flexible inverters did not degrade after bending; instead a small increase in dc gains was observed. Due to the sensitivity of both C_{60} semiconductor and the Ca electrode to ambient conditions, these devices will require encapsulation to protect them from oxygen and moisture.

This material is based on the work supported in part by the STC Program of the National Science Foundation under Agreement No. DMR-0120967 and by the Office of Naval Research and was performed in part at the Microelectronics Research Center at Georgia Institute of Technology, a member of the National Nanotechnology Infrastructure Network, which is supported by NSF (Grant No. ECS-03-35765).

\footnotesize
\begin{itemize}
\end{itemize}