Low-voltage solution-processed n-channel organic field-effect transistors with high-k HfO2 gate dielectrics grown by atomic layer deposition

Shree Prakash Tiwari, Xiao-Hong Zhang, William J. Potscavage, and Bernard Kippelen

Citation: Appl. Phys. Lett. 95, 223303 (2009); doi: 10.1063/1.3269579
View online: http://dx.doi.org/10.1063/1.3269579
View Table of Contents: http://apl.aip.org/resource/1/APPLAB/v95/i22
Published by the American Institute of Physics.
Low-voltage solution-processed n-channel organic field-effect transistors with high-κ HfO₂ gate dielectrics grown by atomic layer deposition

Shree Prakash Tiwari, Xiao-Hong Zhang, William J. Potscavage, Jr., and Bernard Kippelen

Center for Organic Photonics and Electronics (COPE), School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, Georgia 30332, USA

(Received 23 August 2009; accepted 8 November 2009; published online 2 December 2009)

High performance solution-processed n-channel organic field-effect transistors based on [6,6]-phenyl C61 butyric acid methyl ester with low operating voltages (3 V) are demonstrated using a high-κ hafnium dioxide gate dielectric grown by atomic layer deposition. Devices exhibit excellent n-channel performance with electron mobility values up to 0.14 cm²/V s, threshold voltages of ~0.3 V, current on/off ratios >10⁵, and very low values of subthreshold slope (~140 mV/decade). © 2009 American Institute of Physics. [doi:10.1063/1.3269579]

Organic field-effect transistors (OFETs) are receiving significant interest due to their potential applications for large-area, low-cost flexible electronics, like displays, smart

[Image]

FIG. 1. (Color online) (a) Device structure of a top contact OFET along with the chemical structure of [60]PCBM. (b) Output and (c) transfer characteristics of [60]PCBM OFETs with device dimensions of W/L = 2000 μm/25 μm.
TABLE I. Summary of the electrical parameters for 8 [60]PCBM transistors with $L=25$ to 200 $\mu$m and $W=2000$ $\mu$m. All devices were fabricated on the same substrate.

<table>
<thead>
<tr>
<th>Device (W/L)</th>
<th>$\mu$ (cm$^2$/V s)</th>
<th>$V_{TH}$ (V)</th>
<th>$I_{on}/I_{off}$</th>
<th>SS (V/dec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>200 $\mu$m/25 $\mu$m, Dev. 1</td>
<td>0.11</td>
<td>0.27</td>
<td>$1 \times 10^4$</td>
<td>0.13</td>
</tr>
<tr>
<td>2</td>
<td>0.10</td>
<td>0.38</td>
<td>$2 \times 10^6$</td>
<td>0.15</td>
</tr>
<tr>
<td>200 $\mu$m/50 $\mu$m, Dev. 1</td>
<td>0.12</td>
<td>0.33</td>
<td>$4 \times 10^4$</td>
<td>0.17</td>
</tr>
<tr>
<td>2</td>
<td>0.11</td>
<td>0.27</td>
<td>$2 \times 10^4$</td>
<td>0.16</td>
</tr>
<tr>
<td>200 $\mu$m/100 $\mu$m, Dev. 1</td>
<td>0.13</td>
<td>0.32</td>
<td>$2 \times 10^4$</td>
<td>0.14</td>
</tr>
<tr>
<td>2</td>
<td>0.13</td>
<td>0.28</td>
<td>$2 \times 10^4$</td>
<td>0.14</td>
</tr>
<tr>
<td>200 $\mu$m/200 $\mu$m, Dev. 1</td>
<td>0.14</td>
<td>0.32</td>
<td>$3 \times 10^4$</td>
<td>0.14</td>
</tr>
<tr>
<td>2</td>
<td>0.13</td>
<td>0.28</td>
<td>$2 \times 10^4$</td>
<td>0.20</td>
</tr>
</tbody>
</table>

tene™, Dow Chemicals) diluted in trimethylbenzene in a 1:20 ratio and spin coated at 3,000 rpm for 60 s to provide a very thin uniform layer. The samples were then annealed at 250 °C for 1 h inside a N$_2$ glove box for cross linking. The total capacitance density ($C_t$) measured from 12 parallel-plate capacitors was 71 nF/cm$^2$ for HfO$_2$/BCB (reduced due to the BCB layer). A bare 50 nm thick HfO$_2$ layer has a $C_t$ value as high as $\sim 245$ nF/cm$^2$ with leakage current density below $10^{-8}$ A/cm$^2$ under an applied field of 2 MV/cm. A thin layer of [60]PCBM (Solenne B.V., 99.5%) was deposited on the substrates by spin-coating from a solution in chlorobenzene ($10$ mg/mL) at 1000 rpm for 60 s. A 150 nm thick Ca layer (work function 2.9 eV) was deposited through a shadow mask to act as the top S/D electrodes.

The samples were transferred in a vacuum-tight vessel without being exposed to atmospheric conditions into another N$_2$-filled glove box ($O_2$, $H_2O$<0.1 ppm) for electrical testing. The electrical measurements were performed using an Agilent E5272A source/monitor unit. Output ($I_{DS}$ versus $V_{DS}$) and transfer ($I_{DS}$ versus $V_{GS}$) characteristics were measured (dwell time=20 to 50 s, integration time=$6 \times 80$ s) for the devices, and field-effect mobility ($\mu$) values and threshold voltages ($V_{TH}$) were measured in the saturation regime from the highest slope of $|I_{DS}|^{1/2}$ versus $V_{GS}$ plots using the saturation region current equation for standard transistors. For the study of stability under a constant bias, the time-dependent decay of $I_{DS}$ was tested under the following two different dc biasing conditions: (a) in linear operating regime ($V_{GS}=3$ V, $V_{DS}=0.5$ V) and (b) in saturation regime ($V_{GS}=V_{DS}=3$ V) for 1 h. To study the operational stability, the devices were repeatedly stressed by measuring transfer characteristics in the saturation regime 50 times with a 1 s waiting time between cycles.

Figures 1(b) and 1(c) show the output and transfer characteristics of a representative OFET (W/L =2000 $\mu$m/25 $\mu$m). Two identical devices with the same dimensions of W/L=2000 $\mu$m/25 $\mu$m yielded electron mobility values of 0.10 and 0.11 cm$^2$/V s with $V_{TH}$ of 0.38 and 0.27 V, respectively. The current on/off ratios ($I_{on}/I_{off}$) were greater than $10^5$. The devices showed excellent n-channel behavior having no hysteresis in the transfer characteristics and subthreshold slopes (SS) up to 130 mV/decade. Table I summarizes the performance parameters for devices with a channel width $W=2000$ $\mu$m and different channel lengths $L=25$, 50, 100, and 200 $\mu$m fabricated on the same substrate. For each device geometry, we report the performance parameters measured for two identi-cal devices. $I_{on}/I_{off}$ from representative devices is also shown. The SS values reported here are almost five times lower than the values of 0.7 V/decade for [60]PCBM devices on SiO$_2$/BCB dielectric layer recently reported by our group.17 Devices with larger $L$ (200 $\mu$m) provide higher saturation mobility (0.14 cm$^2$/V s) in comparison to the shorter $L$. Interestingly, the electron mobility values are similar to our previously reported values (varying from 0.11 to 0.13 cm$^2$/V s), with the operating voltages reduced by ten times (30 to 3 V) in this case.17

To explore the effect of channel length scaling on $V_{TH}$ and $\mu$, both parameters are statistically plotted over the inverse of channel length ($L^{-1}$) with $W=2000$ $\mu$m. Figure 2(a) shows the plot of $V_{TH}$ with $L^{-1}$, which shows that the devices show almost unchanged $V_{TH}$ on the scaling of $L$ in the used range. However, $\mu$ decreases upon scaling $L$ [see Fig. 2(b)] from 200 down to 25 $\mu$m due to the contact resistance at the metal/organic interface. For a better understanding of the effect of the contact resistance ($R_C$) on the $\mu$, the $R_C$ in each type of device was extracted using a transmission line method based on the dependence of the current-voltage characteristics on $L$. A set of devices $L$ ranging from $L=25$ to 200 $\mu$m and a fixed $W=2000$ $\mu$m was used to calculate the $R_C$ values at a low $V_{DS}$ of 0.5 V for $V_{GS}$ values ranging from 1 to 3 V. In the linear regime, the overall device resistance $R_{on}$ can be considered to be the sum of the channel resistance ($R_{ch}$) and the $R_C$, as already explained in the literature.18,19 The $R_{on}$ here is calculated by dividing the $V_{DS}$ by $I_{DS}$ at $V_{GS}$ values of 1, 1.5, 2, 2.5, and 3 V in the linear regime ($V_{DS}=0.5$ V). Figure 2(c) shows the plot of $R_{on}/W$ versus $L$. The width-normalized contact resistance ($R_C/W$) was calculated by extrapolating $R_{on}/W$ to $L=0$ $\mu$m using the $y$ intercept of plots of $R_{on}/W$ versus $L$, and $R_C/W$ for different $V_{GS}$ are plotted in Fig. 2(d). The $R_C/W$ drops to 18 k$\Omega$ cm, at a gate voltage of $V_{GS}=3$ V.

Figure 3(a) shows the time-dependent decay of $I_{DS}$ under a constant dc bias stress in the linear operating regime.
(\(V_{GS}=3\) V, \(V_{DS}=0.5\) V) as well as saturation regime (\(V_{GS}=V_{TH}=3\) V) over 1 h for these devices. The current decay in both cases exhibited typical features of bias stress instability showing an exponential decay function with extremely low decay in \(\Delta I_{DS}\) of 6% and 7% after one hour in the linear and saturation regimes, respectively. The transfer characteristics were measured right before and after the constant bias stress. (b) Superimposed transfer characteristics of the first ten scans and the last ten scans during a 50-time scan test with 1 s rest time between cycles.

This material is based upon work supported in part by Solvay S.A., by the STC Program of the National Science Foundation under Agreement No. DMR-0120967, and by the Office of Naval Research (Grant No. N00014-04-1-0120).


