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Low-voltage solution-processed n-channel organic field-effect transistors with high-*k* HfO_2 gate dielectrics grown by atomic layer deposition

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High performance solution-processed n-channel organic field-effect transistors based on [6,6]-phenyl C61 butyric acid methyl ester with low operating voltages (3 V) are demonstrated using a high-*k* hafnium dioxide gate dielectric grown by atomic layer deposition. Devices exhibit excellent n-channel performance with electron mobility values up to 0.14 $cm^2/V\,s$, threshold voltages of ~0.3 V, current on/off ratios $>10^5$, and very low values of subthreshold slope (~140 mV/decade). © *2009 American Institute of Physics*. [doi:10.1063/1.3269579]

Organic field-effect transistors (OFETs) are receiving significant interest due to their potential applications for large-area, low-cost flexible electronics, like displays, smart pixels, and radio frequency identification tags.[1–3] For large-area and low-cost processing, solution-processed OFETs are preferred. Solution-processed p-channel OFETs (Refs. 4 and 5) with saturation mobility values up to 0.7 $cm^2/V\,s$ and solution processed n-channel OFETs (Ref. 6) with electron mobility values up to 0.85 $cm^2/V\,s$ have been reported recently; however, the operating voltage of these transistors are still very high (|20| to |60| V). Integration of suitable gate dielectric materials with high capacitance density is very important to achieve low voltage operation in these OFETs for practical electronic circuit applications. Various methods have been reported to get a high capacitance density by developing high-*k* gate dielectric materials,[7–9] and low-voltage transistors have been demonstrated with pentacene. However, reports on low-voltage solution-processed OFETs with high-*k* gate dielectrics are scarce. Atomic layer deposition (ALD) is a simple technique that provides highly conformal, defect-free dielectric layers at relatively low temperature and low cost[10] and provides high quality dielectric layers (such as Al_2O_3) for low-voltage OFETs.[11]

In this letter, we report on high performance, low-voltage, solution-processed n-channel OFETs with high-*k* HfO_2 gate dielectrics (HfO_2, $k\sim15$) grown by ALD. [6,6]-phenyl C61 butyric acid methyl ester ([60]PCBM) is used as the organic semiconductor with top Ca metal source/drain (S/D) electrodes. Fullerene-based compounds are known to be promising candidates for solution-processed n-channel OFETs,[12–15] and [60]PCBM is a widely studied fullerene derivative.[12,14,15] A 50 nm HfO_2 layer deposited by ALD with a thin buffer layer of divinyltetramethyldisiloxanebis(benzocyclobutene) (BCB) on top acts as the gate dielectric. BCB was chosen to minimize electron trapping at the dielectric/semiconductor interface, which is a primary limiting factor for n-channel conduction.[16] We demonstrate overall high performance in these OFETs with [60]PCBM while also achieving low voltage operation (3 V). Channel length scaling is studied with varying channel lengths (L) (25–200 μm), and contact resistance is extracted. We also investigate the stability of these devices under multiple transfer characteristics scans and under continuous electrical bias stress.

OFETs were fabricated on a heavily doped n-type silicon substrate (resistivity $<0.005\ \Omega$ cm, also serves as gate electrodes). A schematic of the device and the chemical structure of [60]PCBM are given in Fig. 1(a). First, the SiO_2 layer from both sides of the wafer was etched away by wet chemical etching with 6:1 buffered oxide etchant. Ti/Au (10 nm/100 nm) metallization on the backside of the substrate was done to improve the gate electrical contact. HfO_2 (50 nm) was deposited using ALD by alternating exposures of tetrakis(dimethylamido)hafnium(IV) (from Aldrich) and H_2O vapor with a substrate temperature of 200 °C using a Savannah100 ALD system (Cambridge Nanotech Inc.). The substrates were cleaned with O_2 plasma for three minutes before and after HfO_2 deposition. The HfO_2 dielectric surface was passivated with a thin buffer layer of BCB (Cyclo-

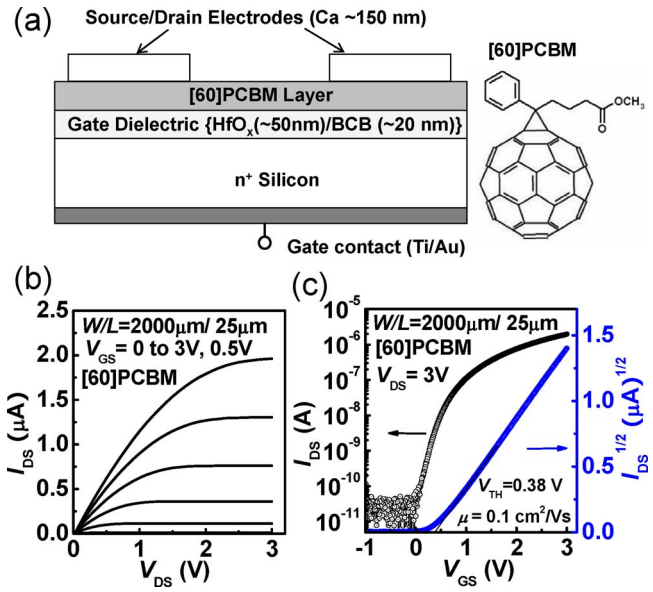

FIG. 1. (Color online) (a) Device structure of a top contact OFET along with the chemical structure of [60]PCBM. (b) Output and (c) transfer characteristics of [60]PCBM OFETs with device dimensions of $W/L=2000\ \mu m/25\ \mu m$.

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TABLE I. Summary of the electrical parameters for 8 [60]PCBM transistors with L=25 to 200 μm and W=2000 μm. All devices were fabricated on the same substrate.

Device (W/L)	μ (cm^2/V s)	V_{TH} (V)	$I_{on/off}$	SS (V/dec)
2000 μm/25 μm, Dev. 1	0.11	0.27	1×10^5	0.13
2	0.10	0.38	2×10^5	0.15
2000 μm/50 μm, Dev. 1	0.12	0.33	4×10^4	0.17
2	0.11	0.27	2×10^4	0.16
2000 μm/100 μm, Dev. 1	0.13	0.32	1×10^4	0.15
2	0.13	0.28	2×10^4	0.14
2000 μm/200 μm, Dev. 1	0.14	0.32	3×10^4	0.14
2	0.13	0.28	2×10^4	0.20

tene™, Dow Chemicals) diluted in trimethylbenzene in a 1:20 ratio and spin coated at 3,000 rpm for 60 s to provide a very thin uniform layer. The samples were then annealed at 250 °C for 1 h inside a N_2 glove box for cross linking. The total capacitance density (C_i) measured from 12 parallel-plate capacitors was 71 nF/cm^2 for HfO_2/BCB (reduced due to the BCB layer). A bare 50 nm thick HfO_2 layer has a C_i value as high as ~245 nF/cm^2 with leakage current density below 10^{-8} A/cm^2 under an applied field of 2 MV/cm. A thin layer of [60]PCBM (Solenne B.V., 99.5%) was deposited on the substrates by spin-coating from a solution in chlorobenzene (10 mg/mL) at 1000 rpm for 60 s. A 150 nm thick Ca layer (work function 2.9 eV) was deposited through a shadow mask to act as the top S/D electrodes.

The samples were transferred in a vacuum-tight vessel without being exposed to atmospheric conditions into another N_2-filled glove box (O_2, $H_2O<0.1$ ppm) for electrical testing. The electrical measurements were performed using an Agilent E5272A source/monitor unit. Output (I_{DS} versus V_{DS}) and transfer (I_{DS} versus V_{GS}) characteristics were measured (dwell time=20 to 50 s, integration time=6×80 μs) for the devices, and field-effect mobility (μ) values and threshold voltages (V_{TH}) were measured in the saturation regime from the highest slope of $|I_{DS}|^{1/2}$ versus V_{GS} plots using the saturation region current equation for standard transistors. For the study of stability under a constant bias, the time-dependent decay of I_{DS} was tested under the following two different dc biasing conditions: (a) in linear operating regime (V_{GS}=3 V, V_{DS}=0.5 V) and (b) in saturation regime ($V_{GS}=V_{DS}$=3 V) for 1 h. To study the operational stability, the devices were repeatedly stressed by measuring transfer characteristics in the saturation regime 50 times with a 1 s waiting time between cycles.

Figures 1(b) and 1(c) show the output and transfer characteristics of a representative OFET (W/L =2000 μm/25 μm). Two identical devices with the same dimensions of W/L=2000 μm/25 μm yielded electron mobility values of 0.10 and 0.11 cm^2/V s with V_{TH} of 0.38 and 0.27 V, respectively. The current on/off ratios (I_{on}/I_{off}) were greater than 10^5. The devices showed excellent n-channel behavior having no hysteresis in the transfer characteristics and subthreshold slopes (SS) up to 130 mV/decade. Table I summarizes the performance parameters for devices with a channel width W=2000 μm and different values of channel length L=25, 50, 100, and 200 μm fabricated on the same substrate. For each device geometry, we report the performance parameters measured for two identical devices. I_{on}/I_{off} from representative devices is also shown. The SS values reported here are almost five times lower than the values of 0.7 V/decade for [60]PCBM devices on SiO_2/BCB dielectric layer recently reported by our group.[17] Devices with larger L (200 μm) provide higher saturation mobility (0.14 cm^2/V s) in comparison to the shorter L. Interestingly, the electron mobility values are similar to our previously reported values (varying from 0.11 to 0.13 cm^2/V s), with the operating voltages reduced by ten times (30 to 3 V) in this case.[17]

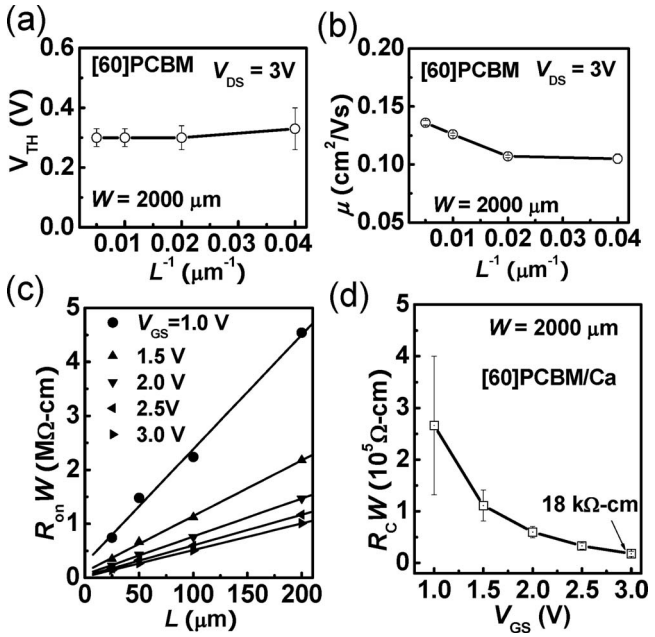

FIG. 2. The dependence of (a) V_{TH} and (b) μ on L^{-1}. (c) Values of $R_{on}W$ obtained at various V_{GS} for different channel lengths. (d) Plot of R_CW as a function of V_{GS}.

To explore the effect of channel length scaling on V_{TH} and μ, both parameters are statistically plotted over the inverse of channel length (L^{-1}) with a W=2000 μm. Figure 2(a) shows the plot of V_{TH} with L^{-1}, which shows that the devices show almost unchanged V_{TH} on the scaling of L in the studied range However, μ decreases upon scaling L [see Fig. 2(b)] from 200 down to 25 μm due to the contact resistance at the metal/organic interface. For a better understanding of the effect of the contact resistance (R_C) on the μ, the R_C in each type of device was extracted using a transmission line method based on the dependence of the current-voltage characteristics on L. A set of devices L ranging from L=25 to 200 μm and a fixed W=2000 μm was used to calculate the R_C values at a low V_{DS} of 0.5 V for V_{GS} values ranging from 1 to 3 V. In the linear regime, the overall device resistance R_{on} can be considered to be the sum of the channel resistance (R_{ch}) and the R_C, as already explained in the literature.[18,19] The R_{on} here is calculated by dividing the V_{DS} by I_{DS} at V_{GS} values of 1, 1.5, 2, 2.5, and 3 V in the linear regime (V_{DS}=0.5 V). Figure 2(c) shows the plot of $R_{on}W$ versus L. The width-normalized contact resistance (R_CW) was calculated by extrapolating $R_{on}W$ to L=0 μm using the y intercept of plots of $R_{on}W$ versus L, and R_CW for different V_{GS} are plotted in Fig. 2(d). The R_CW drops to 18 kΩ cm, at a gate voltage of V_{GS}=3 V.

Figure 3(a) shows the time-dependent decay of I_{DS} under a constant dc bias stress in the linear operating regime

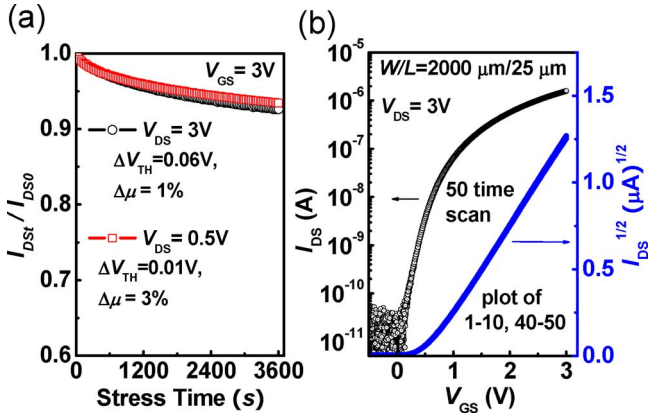

FIG. 3. (Color online) (a) Decay of I_{DS} measured during bias stress experiments in the linear (V_{GS}=3 V, V_{DS}=0.5 V) and saturation regions (V_{GS} = V_{DS}=3 V). ΔV_{TH} and $\Delta\mu$ were determined from the transfer characteristics measured right before and after the constant bias stress. (b) Superimposed transfer characteristics of the first ten scans and the last ten scans during a 50-time scan test with 1 s rest time between cycles.

(V_{GS}=3 V, V_{DS}=0.5 V) as well as saturation regime (V_{GS}=V_{DS}=3 V) over 1 h for these devices. The current decay in both cases exhibited typical features of bias stress instability showing an exponential decay function with extremely low decay in I_{DS} of 6% and 7% after one hour in the linear and saturation regimes, respectively. The transfer characteristics were measured right before and after the constant bias stress to determine the threshold voltage shift (ΔV_{TH}) and change in μ. After 1 h of stressing at V_{GS}=3 V, V_{DS} =0.5 V, a nominal decrease of 3% in μ was observed, with a very small ΔV_{TH} of 0.01 V. In the saturation regime (1 h stressing at V_{GS}=V_{DS}=3 V) the decrease in μ was 1%, with a low change in ΔV_{TH} of 0.06 V. To check the reproducibility of the electrical characteristics, the transfer characteristics of the devices were scanned 50 times with a time interval of 1 s between scans in N_2. The superimposed measured transfer curves from the first ten cycles and the last ten cycles are shown in Fig. 3(b). The shape of the successive transfer curves remained almost unchanged during multiple scans, indicating a good electrical stability and reproducibility for devices under normal operation, resulting in the reliable extraction of device parameters. Both of these studies show that these OFETs have extremely good electrical bias and operational stability, which is very important for the reliable operation of organic devices and circuits.

In summary, solution-processed n-channel OFETs based on [60]PCBM with very low operating voltages (3 V) were demonstrated by integration of high-k hafnium dioxide gate dielectric grown by ALD with a thin buffer layer of BCB on the top as the gate dielectric layer. Ca was used as S/D electrodes to achieve overall high performance. The devices exhibited excellent n-channel performance with an average electron mobility up to 0.14 $cm^2/V\,s$ at operating voltages below 3 V. The extracted $R_C W$ was as low as 18 $k\Omega$ cm at V_{GS}=3 V. These devices showed stable electrical behavior under multiple scans and low threshold voltage instability under continuous electrical bias stress when tested in inert atmosphere.

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