Next-Generation Microvia and Global Wiring Technologies for SOP

Venky Sundaram, Rao R. Tummala, Fellow, IEEE, Fuhan Liu, Paul A. Kohl, Member, IEEE, Jun Li, Sue Ann Bidstrup-Allen, and Yoshitaka Fukuoka, Senior Member, IEEE

Abstract—As microsystems continue to move toward higher speed and microminiaturization, the demand for interconnection density both on the IC and the package levels increases tremendously. The 2002 ITRS roadmap update identifies the need for sub-100-μm area array pitch and data rates of 10 Gb/s in the package or board by the year 2010, requiring much finer lines and vias than the current microvias of 50 μm diameter and lines and spaces of 25 μm. After a brief description of the future need for high-density substrates, the historical evolution of microvia technologies worldwide is summarized. With the move toward highly integrated and higher performance system-on-a-package (SOP) technology, the demand for microvia wiring density in the package is increasing dramatically requiring new innovations in fine line, ultralow-loss, and ultrathin-film dielectrics. The low-cost needs of this technology are driving research in high throughput and large area processes in dielectric and conductor deposition. The third section of this paper describes in detail some of the key emerging global microvia research and development in the fabrication of microminiaturized, multifunction SOP packages including rapid curing of low-loss dielectric thin films on organic substrates, environmentally friendly high-speed electroless copper plating, ultrafine lines, and spaces down to 5 μm and low-cost stacked via structures without chemical-mechanical polishing. This paper concludes with a perspective on future directions in dielectrics and conductor materials and processes leading to ultrahigh-density and low-cost microvia technologies for build-up SOP implementation.

Index Terms—Conductors, embedded passives, fine lines, global interconnect, high speed, low-loss dielectrics, microvia, PWB, stacked viss, system-in-a-package (SIP), system-on-a-package (SOP), thin film.

I. INTRODUCTION

THERE is a trend in electronic systems toward miniaturization and higher functionality, driving the demand for greater interconnect density at the IC, package, and board levels. Area array solutions such as flip-chip and wafer level packaging will become increasingly critical for chip to next level interconnections. Table I summarizes the needs for 5 μm line and space microvias technology identified by the IC roadmaps (2002 ITRS) and electronics product roadmaps (2000 NEMI).

The 2003 ITRS Roadmap calls for organic substrates with less than 100-μm area array pitch flip and data rates of 10-15Gb/s in the package or board by the year 2010 [1]. The NEMI 2000 roadmap defines the need for 4–8 layers of 5–10-μm wiring for future system boards [2]. There is a critical need, therefore, for substrate technology with >5000 cm/cm² wiring density to interconnect I/O density of >10000/cm². Signal integrity for 10-15Gb/s data rates requires ultralow loss dielectric materials with loss tangent ~0.001. Power integrity to support >200 W power with <90 mV ΔI noise translates to embedded decoupling in the package with >0.1 μF capacitance. Signal delay in global interconnects on ICs will dominate gate delay and thus impact system performance. With the availability of high-density substrates with 3–5 μm linewidths, system-on-a-package (SOP) provides a unique opportunity for global wiring to be off-loaded to the package for enhanced performance. In contrast, the current leading-edge microvia substrates in the industry provide only 500–1000 cm/cm² wiring density using epoxy-based materials with high loss and high moisture uptake. Further, low-loss laminate dielectric materials can only be used in 2–5 mil-thick films and, thus, pose wiring density limits. There is a further need to lower the cost, thus driving large area processing solutions such as the proposed SOP to meet ultrahigh-density wiring and ultrahigh-speed signals in a single package with integrated passive and active digital, RF, and optical components.

Some of the latest advances in microvia technology for next-generation SOP packaging are reviewed and discussed in this paper, along with a brief review of the historical evolution of this technology.

II. HISTORICAL EVOLUTION OF MICROVIA TECHNOLOGIES

The historical evolution and future trend in microvia technology are shown in Fig. 1. Microvia technologies, also called build-up substrates or boards were pioneered at IBM Japan since 1987 to support the needs of area array assembly of ICs. There are two main classes of microvia technologies, thin film and thick film. The first group is based on thin-film technology combined with conventional PWB—cores with through hole plating such as SLC by Japan IBM [3], IBSS/AAP10 by Ibiden [4], DYCOSTrate by Dyconex [5], VIL by Japan Victor [6], CLLAVIS by CMK [7] and others. These technologies are further classified by microvia formation processes as follows. SLC and IBSS/AAP10 are photo-via processes. DYCOSTrate is by plasma via process and VIL and CLLAVIS are laser via processes. The second group is based on thick film technology combined with conventional through hole plating. These are ALIVH by Matsushita [8] and B2™ by Toshiba/DCT/T/DNP [9]. The ALIVH microvias are formed by laser drilling and...
TABLE I
IC AND SYSTEM BOARD ROADMAPS DOCUMENT THE NEED FOR 5 μm MICROVIA TECHNOLOGY

<table>
<thead>
<tr>
<th>Roadmap</th>
<th>System/IC Need</th>
<th>Microvia Substrate Need</th>
</tr>
</thead>
<tbody>
<tr>
<td>IC</td>
<td>• 0.07μm IC Gates</td>
<td>• 5-10μm lines and spaces</td>
</tr>
<tr>
<td></td>
<td>• 10000 I/Os/cm²</td>
<td>• 10-15μm stacked vias</td>
</tr>
<tr>
<td></td>
<td>• 50-100 μm area array pad pitch</td>
<td>• &lt;1μm/\text{inch} warpage</td>
</tr>
<tr>
<td></td>
<td>• Minimize Global Wiring Delay</td>
<td>• Transfer from IC to Board</td>
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<td></td>
<td>• High Performance Systems Wiring</td>
<td>• 5-10μm wiring</td>
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<td></td>
<td>• 4-8 layers of wiring</td>
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Electronic Systems

The SOP technologies are expected to lead packaging developments starting around 2007. To meet the electrical and thermal characteristics of these type of packages, ultrahigh-den-
Density interposer substrates are being developed worldwide, including not only with embedded passive devices (EPD) such as capacitors, resistors, and inductors, but also embedded active devices (EAD) within the ultrahigh-density multilayer thin film wiring with low dielectric constant and low dissipation factor materials on high strength core substrates having through microvia interconnections [14]. One such ultramicrovia Si-interposer substrate structure is shown in Fig. 1, as an example of a future SOP package. In general, three kinds of EPD materials are now available: (1) low cure temperature polymer thick-film paste compatible with organic substrates; (2) high-temperature fired inorganic thick-film paste compatible with ceramic substrates; and (3) thin-film passive materials using vacuum processes. In general, better tolerance of passive elements can be obtained with thin film technology. However, most current materials have limitations on values of resistance, capacitance and inductance as well as power dissipation, breakdown voltage, high-frequency characteristics, and so on. Therefore, a new generation of EPD materials based on nano technology is anticipated in the near future. General design rules of the aforementioned microvia technology generations are summarized in Table II. The ultrafine wiring on future interposer substrates will need to be 3–10 μm lines and spaces and electrical modeling will be essential in determining maximum wiring lengths to meet high-speed signals with acceptable conductor loss.

### III. Emerging Microvia Research and Development

The next generation of microvia substrates for fully integrated SOP will have not only extremely high-density wiring, but also interconnections for embedded passive and active components as well as provide global wiring on the package. Innovative solutions are needed to address these challenges in electrical and thermomechanical design, integration of ultralow loss, low- and high-k dielectrics, conductor geometries with submicron precision, and low-cost processes for multilayer stacked via interconnects. The following sections review some of the key recent developments in next-generation build-up microvia for SOP substrate at the Packaging Research Center, Georgia Tech.

#### A. Electrical and Thermomechanical Design

Fig. 2 illustrates the escape routing necessary for 100 μm pitch area array packaging using 50 μm bumps and spacing.

For area array pitch of 100 μm and lower, multilayer wiring up to 10 signal layers with 10 μm lines and spaces is necessary. The design of 50 Ω impedance microstrip transmission lines for such fine conductor geometries requires low-loss dielectric thin films in the thickness range of 10–15 μm. Signal speeds in the multiple-GHz range in the package imposes submicron tolerances on conductor geometry and dielectric loss below 0.001. Global wiring on chip is typically less than 1 μm width using 1–2 μm dielectric thickness. The resistivity and conductor loss of such fine lines limits the high-speed performance of global interconnects on large (1.5–2 cm) ICs. The ability to fabricate 50 Ω copper lines in 3–5 μm widths using 5-μm-thick dielectric films will enable the integration of global interconnects in the SOP package substrate for enhanced performance and reducing global wiring delay.
The substrate design process also requires attention to package or board core materials, both to achieve stacked vias without capture pads as well minimize stress on the solder joint between IC and the SOP package. There is increasing acceptance of the need for low CTE package substrates and a number of new materials in the 8–12 ppm/C CTE range are being developed for enhanced reliability of fine pitch area array packages. Examples include Hitachi MCL-E-679F and 679LD laminates with CTE in the 9–12 ppm/C range and organic laminates with Cu-Invar-Cu cores. CTE match between package substrate and the silicon chip has the potential to eliminate the use of expensive underfill process and materials for reliable flip-chip interconnect. Multilayer buildup with layer to layer registration better than 1–5 µm requires package substrates with exceptional dimensional stability and minimum warpage during processing. Ultrahigh modulus (>450 GPa), large area C-SiC composite substrates are being developed and evaluated for ultrahigh-density buildup of SOP packages [15], [16]. The role of low CTE and high modulus in multilayer thin-film build-up process has been evaluated through extensive thermomechanical modeling [17]. Fig. 3 illustrates the effect of substrate modulus on warpage during high-density wiring fabrication.

**B. Dielectric Materials, Processes, and Properties**

There are several critical performance requirements that a polymeric dielectric material must meet for use as a dielectric build-up layer in the microvia fabrication process. For high-frequency mixed-signal SOP packages, a material with a low dielectric constant and a low dielectric loss tangent is needed. Differences in the coefficient of thermal expansion (CTE) of the materials used in the high-density interconnection packages are primary sources of stress. Hence, selection of dielectrics with matched-CTE throughout the package is desirable. Cracking of the dielectric layer can also be minimized by utilizing materials with a high elongation-to-break and a lower modulus. The dielectric material must be thermally stable and not outgas at all temperatures experienced during processing and use. Degradation and solvent loss from the material can lead to delamination and degradation of properties, including adhesion, dielectric properties, and mechanical properties. In addition, the dielectric must possess a processing temperature window that is below the degradation temperature of all materials present in the package. The dielectric material should adhere well to the substrate and metal interconnect present in the microvia board in addition to adhering well to itself. Delamination of the dielectric layer can result in package failure or long-term reliability problems. The dielectric should have a low moisture uptake. Water absorption in the dielectric layer can result in undesirable changes in adhesion, electrical properties, and stress.

1. **Current Dielectric Materials**: Currently, most microvia build-up layers in high-density packages use epoxy-based dielectrics and low-cost organic core substrates (e.g., FR4 epoxy fiberglass boards) [18]. Epoxies have been widely used in the microvia boards due to their excellent adhesion to a variety of substrates, good thermal stability, low processing temperature (<150 °C), and low cost. However, epoxies also have higher dielectric constants (3.5–5.0) than many other polymer
dielectrics and have high water uptake (0.3–1.0 wt%). New materials, with lower stress are required to minimize film fracture along via holes in high-density packages. Some high-performance dielectrics like A-PPE from Asahi-Kasei, LCP from Rogers and Gore, and hydrocarbon-ceramic 4000 series from Rogers are gaining acceptance for high-frequency applications. A summary of high-performance build-up dielectric materials used in microvia substrates is shown in Table III along with their key electrical properties and processing methods.

The ideal dielectric material for future high-density packaging should have low loss and dielectric constant at GHz frequencies along with low CTE and high strength, and very low moisture absorption and stability over operating temperatures. Thin films are essential to satisfy impedance requirements and low processing temperatures to prevent degradation of the temperature sensitive organic board. For example, Table IV shows the extent of imidization achieved in a film cured for 1 h in a conventional thermal furnace at 200 °C, as well as superior electrical properties and processing methods.

Variable frequency microwave (VFM) curing of high-performance polymers has been investigated as a low-temperature curing alternative to conventional heating in a thermal oven [19]–[23]. The unique feature of VFM heating, as compared to conventional heating, is the ability to quickly and repeatedly step through a range of frequencies. This stepping process provides a time-averaged uniformity in the energy distribution throughout the cavity and thereby eliminates the nonuniformities in temperature that occur in single frequency microwave chambers [24]. The VFM technique also allows metals and conducting materials to be placed in the microwave cavity. By cycling through thousands of frequencies in less than one second, the residence time of any established wave pattern is on the order of microseconds and problems with charge buildup and arcing are eliminated [25].

Tanikella [19] demonstrated the feasibility of rapid curing of polyimides on organic substrates using VFM processing. Organic boards, such as FR4 are not significantly heated by microwave energy, but the precursor solutions of polyimide couple the microwave energy efficiently. As a result, full curing of the polyimide precursors is achieved without thermal degradation of the temperature sensitive organic board. For example, Table IV shows the extent of imidization achieved in a particular polyimide film (HD Microsystems PI 2611, whose monomeric system consists of biphenyltetraacryxylic acid and phenylene-diamine) processed on an FR-4 board using both conventional heating in a thermal oven and VFM processing.

It can be seen that a higher extent of imidization can be achieved by VFM processing for a much shorter cure time as compared to conventional thermal curing. For example, a 4-h thermal furnace cure at 175 °C gives 50% imidization while a 5-min VFM cure at 200 °C gives an extent of imidization of 92%. Further, a 5-min VFM cure at 200 °C gives 100% imidization without degradation of the epoxy board. Only 73% imidization is achieved in a film cured for 1 h in a conventional thermal furnace at 200 °C and films cured for 1 h at 250 °C achieve 100% imidization, but the FR-4 board is decomposed. Moreover, Fourier transform infrared analysis confirms that there are no differences in chemical structure between a fully imidized system processed using VFM curing at 200 °C compared with a film processed in a conventional thermal oven at 350 °C (see Fig. 4). Hence, it has been demonstrated that a high-performance polymer dielectric can be fully processed on a temperature sensitive organic board, without obtaining board degradation.

In addition to the development of new processing techniques, the formulation of new chemistries may enable the formation of high-performance insulation layers with sufficiently low processing temperatures to prevent degradation of temperature sensitive boards. Photosensitive dielectric materials based on polynorbornene chemistry have been developed with low processing temperatures (<160 °C) as well as superior elec-
trical and thermomechanical properties [26]–[28]. Performance properties include a dielectric constant of 2.5 (measured at 50 MHz), moisture uptake of 0.3 wt%, a tensile modulus of 0.5 GPa and residual stress (measured on a silicon substrate) of less than 4 MPa. This chemistry represents a substantial improvement in performance properties over epoxy-based systems, and still enables low temperature processing on FR-4 boards.

As the demand for lower dielectric constant materials continues, increasing attention has been focused on porous dielectric materials to satisfy future high-density interconnection requirements. The advantage of these materials is clear: no fully densified materials can match the ultralow dielectric constant values that can be obtained when air (i.e., pores) is added to the films. The formation of porous dielectric films and the effect of adding porosity on lowering the dielectric constant have been established [29]–[32]. However, formation of nanoporous films frequently requires high-processing temperatures and, therefore, is incompatible with microvia formation on FR-4 boards. Although the technology is promising for obtaining low dielectric constant goals, new porous dielectric chemistries are required for low temperature processing on organic boards.

3) New Conductor Metallization Processes: Metallization of SOP substrates is typically accomplished by electroless and/or electroplating. The simplest and potentially lowest cost metallization process is the “fully additive” process where electroless plating is used to build the full thickness of the metal layer [33]. Electroless plating is a low cost and batch processing technique suited for high-volume manufacturing. However, traditional electroless baths have low deposition rates and use formaldehyde, a carcinogen. Also, the high pH of traditional electroless copper baths can degrade some photoresist. A novel formaldehyde-free electroless copper plating chemistry with low pH (<9.0) and high deposition rates (3–4 μm/h) has been developed to meet the wiring needs of future SOP packages.

Electroless copper plating involves the reduction of Cu²⁺ ions to copper metal and the surface catalyzed oxidation of a reducing agent [34], [35]. The catalytic oxidation of formaldehyde increases with hydroxide concentration and is only effective at pH above 11. Several electroless copper solutions using nonformaldehyde reducing agents have been reported and the process involving hypophosphite is shown in (1) [36]–[41]

\[
\text{Cu}^{2+} + 2\text{H}_2\text{PO}_2^- + 2\text{OH}^- \rightarrow \text{Cu} + 2\text{H}_2\text{PO}_3^- + \text{H}_2. \tag{1}
\]

However, the inherent drawback for using hypophosphite as the reducing agent is the weak catalytic activity for the oxidation of hypophosphite on copper. While the initial substrate surface is palladium-activated, once it is coated with copper, the reaction slows because copper is not a catalytic material. One way to compensate for the poor catalytic activity of copper is to add nickel ions to the solution. The codeposited nickel in the copper deposit serves to catalyze the oxidation of hypophosphite, thus increasing the overall deposition rate [42]. Thiourea (tu) and diphenylthiourea (DPTU) have been shown to increase the deposition rate of electroless copper plating solutions that use HEDTA as the complexing agent and sodium hypophosphite as the reducing agent.

**Table V**

| COMPOSITION AND OPERATING CONDITIONS OF THE ELECTROLESS COPPER PLATING SOLUTION |
|------------------|------------------|
| CuSO₄·5H₂O       | 0.04 M           |
| NaH₂PO₃·H₂O      | 0.12 M           |
| HEDTA            | 0.08 M           |
| H₂BO₂            | 0.48 M           |
| NiSO₄·6H₂O       | 500 ppm          |
| Polyethylene Glycol| 200 ppm         |
| pH               | 9.3              |
| T(°C)            | 70               |

*Fig. 5.* Effects of the thiourea concentration in the copper plating solution on the deposition rates and resistivity of the electroless copper deposits.

*Fig. 6.* Effects of the DPTU concentration in the electroless copper plating solution on the deposition rates and resistivity of the copper.

a) The Effect of tu and DPTU on Deposition Rates: When only a small amount of tu was added into the electroless copper plating solution (see Table V) with N-(2-hydroxyethyl)ethylendiaminetriacetic acid trisodium salt hydrate (HEDTA) as the complexing agent and hypophosphite as the reducing agent, the deposition rate of copper plating increased significantly, as shown in Fig. 5. The color of the deposits changed from black in the absence of tu in the solution to semibright at 0.5 ppm tu. In addition, the resistivity of the copper deposits decreased due to changes in the structure of the deposits. Unfortunately, as the tu concentration was increased, the plating rate decreased slightly. When the tu concentration was more than 1.0 ppm, the copper deposit became brittle and appeared black, similar to when there was no tu.

DPTU had a similar beneficial effect on the deposition rate as tu in the electroless copper plating solution. Fig. 6 shows the average deposition rate of the electroless copper plating solution
and resistivity of the deposit as a function of DPTU concentration. Although the deposition rate with DPTU was less than that with tu, the resistivity of the copper deposit was lower and nearly the same as that obtained with formaldehyde-based electroless copper solutions [43].

b) Surface Morphologies of Copper Deposits: Fig. 7 shows the surface morphologies of the copper deposits from the electroless solutions with and without additives. The topography of the copper deposited from the hypophosphite electroless copper plating solution was relatively rough with small growth colonies and resulted in higher resistivity. When tu and DPTU were added in the solution, the copper deposits became more uniform and the growth colony size increased.

The optimized low pH formaldehyde-free plating chemistry shown in Table V with small additions of thiourea and DPTU was used in a fully additive build-up process on photodefensible epoxy dielectric. The photoresist used was Shipley Eagle NT-90, a negative acting liquid resist with 3–5 μm resolution. Fig. 8 shows the top view of 25–75 μm fine lines and spaces fabricated to 10-μm copper thickness.
C. Novel Structures for Future Microvia Boards

The typical methodologies used to increase wiring density are (1) reducing the linewidth and line space; (2) increasing the number of layers; and (3) using small capture pads. Additionally, next generation of microvia substrates also require low cost processes. The research at PRC is focused on all of these including (1) ultrafine lines of 3–5 μm dimensions; and (2) stacked microvias of 10–15 μm diameter. Precise control of the photolithography process was combined with high-resolution liquid photoresists coated as thin films to achieve copper lines with <5% control of X, Y, and Z dimensions.

Recent research has showed that the above feature sizes are indeed achievable [44]–[46]. A cross-section micrograph of a comb structure having linewidths of 10 μm and space of 10 μm on a build-up high-Tg FR-4 substrate is shown in Fig. 9. The metal thickness of the comb is 10 μm (Aspect Ratio = 1.0). Fig. 10 illustrates the top view of an extremely fine structure. Here, a 20-μm-wide and 9 500-μm-long structure made of 4 μm copper lines were formed on a build-up epoxy dielectric layer coated on a high Tg FR-4 laminate. Semiadditive metallization using electroless copper thin seed layer and pattern electroplating were used to form the structure on a build-up layer. The thickness of the plated copper was 4 μm (Aspect Ratio = 1.0). These structures were obtained by using Shipley Eagle NT-90 liquid photoresist and a chrome on glass photomask.

Surface roughness is a critical factor for both fine line lithography and metallization. Comparisons of typical epoxy dielectric surfaces obtained by permanganate desmear treatment and CF3/O2 plasma roughening is shown in Fig. 11. Permanganate or other wet etch processes result in a dielectric surface with roughness of the order of 2–3 μm depth and large pits, as seen in Fig. 10(a). Multilayer thin-film wiring on such a surface would result in latent defects in the traces and inconsistent dielectric separation between metal layers. The plasma treatment on the other hand produces a fairly uniform roughness on the surface that is typically <1 μm deep. The plasma process has been successfully implemented to fabricate the fine lines shown in Figs. 8 and 9. Additionally, a planar surface is required for fabrication of fine lines on large substrates due to depth of field and contact limitations during lithography. The adhesion of the photoresist during metallization and copper to dielectric peel strength are also lower for finer geometries due to the smaller contact area.

An additional barrier to achieving the target wiring density is the size of capture pads. The via grid and pitch have to be of similar dimensions as the I/O pads. Via and pad geometries have migrated from the conventional dogbone structure to via-in-pad structures with conformal vias (shown in Fig. 12). For future fine pitch flip-chip interconnects, it will be necessary to migrate
to planar pad structures with filled and stacked vias and minimum capture pad size as shown in Fig. 12.

A novel low-cost process for fabricating multilayer stacked via structures has been developed using a panel electroplating and subtractive etch process called P2ES (panel plating etched stud) [47]. Filled stacked vias of 50, 75, and 100 μm diameter up to four metal layers have been demonstrated using this low cost large area approach that does not involve any chem.-mech polishing (CMP). A schematic of the process sequence for the P2ES process is shown in Fig. 13(a). Since this process utilized photoresist to define the via structures, it does not have any minimum size limitations common to conventional laser and photovia processes. Furthermore, this process is versatile and can be used in conjunction with most liquid, dry film, and RCC dielectrics. Stud height uniformities of less than 1 μm have been demonstrated using this technique on 300 mm × 300 mm FR-4 substrates as seen in Fig. 13(b). A typical four-metal layer structure used in a build-up SOP application is shown in Fig. 14. This process is currently being extended to ultrafine microvias of 10–15 μm diameters. The stacked via structure along with the ultrafine lines can potentially meet the interconnection and global wiring requirements of next-generation SOP packages.

IV. CONCLUSION

In spite of the tremendous progress in microvia and high-density substrate technologies in the last two decades, a new set of substrate and dielectric materials and processes are needed. Several dielectric materials including BCB, A-PPE, LCP offer the potential to satisfy the electrical performance specifications in the short run but new materials with low dielectric loss and processable into thinner films at lower cost are needed in the long run. These, together with high-k dielectrics processed as thin films, form the basis of highly integrated and high performance packages to provide digital functions of the SOP mixed signal systems. Thus, lower k and low-loss compatible dielectrics along with innovative conductor metallization processes for multilayer build-up processes are expected to lead to microminiaturized and multifunction SOP packages with unparalleled performance, cost, and reliability.

ACKNOWLEDGMENT

The authors acknowledge the contributions of faculty, research staff, graduate, and undergraduate students at PRC.

REFERENCES


Venky Sundaram received the B.S. degree in metallurgical engineering from the Indian Institute of Technology, Bombay, and the M.S. degree in ceramic and materials engineering from the Georgia Institute of Technology (Georgia Tech), Atlanta.

He is a research staff member with Georgia Tech Packaging Research Center (PRC) and is currently coleading the SOP package substrate development program at the PRC. He is also a Ph.D. degree candidate in materials science and engineering at Georgia Tech. He has more than seven years experience in high-density microvia board and thin-film technology. He has more than 30 publications, four patents pending, and a number of invention disclosures in SOP substrate technology and RF/digital packaging. He has presented industry short courses on "Embedded Passives" and "High Density PWB Technologies."

Mr. Sundaram is a member of the High Density Substrate Technical Committee (TC-6) of the IEEE-CPMT society, PRC program manager for the SOP Technology Transformation Partnership with Endicott Interconnect, New York, and the High-Density Substrate Task Leader for the multimillion dollar Nano-Wafer Level Packaging Program.

Rao R. Tummal received the B.E. degree in metallurgical engineering from the Indian Institute of Science, Bangalore, and the Ph.D. degree in materials science and engineering (MSE) from the University of Illinois, in 1989.

He is an Endowed Chair Professor in electrical and computer engineering and MSE with the Georgia Institute of Technology (Georgia Tech), Atlanta. He is also the Founding Director of the Microsystems Packaging Research Center (PRC). The PRC is currently the largest and most comprehensive microsystems packaging center involving 250 students, 30 faculty, and 50 global companies, and was funded by the National Science Foundation (NSF) as one of its Engineering Research Centers in the United States, the Georgia Research Alliance, and the electronics industry, where he is pioneering the system-on-a-package (SOP) vision for mixed-signal systems of the next decade. He is also a Temasek Professor, NUS, Singapore. Prior to joining Georgia Tech, he was an IBM Fellow where he invented a number of major technologies for IBM’s products for packaging, displaying, printing, and magnetic storage that include LTCC and scale-up of multilayer alumina ceramic. He was also part of the pioneering team that developed the industry’s first flat panel display based on gas discharge display. He was the Director of the Advanced Packaging Technology Laboratory for all of IBM in 14 labs across the United States, Europe, and Japan. He edited the first undergraduate textbook Fundamentals of Microsystems Packaging (New York: McGraw-Hill) currently used by 43 universities around the world. He edited the first modern book in packaging Microelectronic Packaging Handbook (1988) which began to catalyze the academic research and educational programs. During this time, he began to lecture and advise universities in this area throughout the United States. Three notable examples are: Chairman of Advisory Board at the Massachusetts Institute of Technology, Cambridge, from 1988 to 1993, at the University of California at Berkeley from 1984 to 1987, and at the University of Illinois, Urbana, from 1983 to 1986. He left IBM in October 1993 and, two weeks later, wrote the winning NSF proposal for an NSF-Engineering Research Center on SOP. He has published 350 papers and holds 71 U.S. patents.
Dr. Tummala received 16 technical, outstanding, and corporate awards from IBM, the highest Faculty Award at Georgia Tech, alumni awards from the University of Illinois and IISe, the David Sarnoff award from the IEEE for MCM, the Dan Hughes Award from IMAPS, the Engineering Materials Award from ASME, the Total Quality Manufacturing Award from SME, and the IEEE’s Major Educational Innovation award. He is a member of NAE, IMAPS, and the American Ceramic Society, and Past President of the IEEE CPMT and IMAPS societies.

Fuhan Liu received the M.S. degree in electron physics from Fudan University, Shanghai, China, in 1965. Currently, he is a Research Engineer at NSF-Packing Research Center (PRC) at the Georgia Institute of Technology (Georgia Tech), Atlanta. Prior to coming to the United States in 1997, he was an Associate Professor in the Department of Material Science and Deputy Director of High Density Electronic Packaging Laboratory at Fudan University. He had been a Visiting Scholar at Brandeis University (1987–1988), Wayne State University (1997–1998), and International Microelectronics and Packaging Society (IMAPS, 1997). Currently, he focuses on the R&D of fabrication and integration of high-density wiring and optoelectronics for systems-on-package, material evaluation, processes development, and testing. Dr. Liu received the Global Collaboration Award for his outstanding contributions to the NSF Programs and numerous national outstanding awards from China. His paper on “Nitrogen Temperature Super- Conducting Ring Experiment” was voted as the “Memorable Paper of the American Journal of Physics (AJP) since 1933” and his name was listed in the “AJP All-Star” team.

Paul A. Kohl (M’92) received the Ph.D. degree from The University of Texas at Austin in chemistry in 1978. He was with AT&T Bell Laboratories, NJ, from 1978 to 1989. At Bell Laboratories, he was involved in new materials and processing methods for semiconductor devices. In 1989, he joined the faculty of the Georgia Institute of Technology, Atlanta, where he is currently a Regents’ Professor. His research interests include ultralow-k dielectric materials, interconnects for microelectronic devices, and electrochemical energy conversion devices. He has more than 130 journal publications and 30 patents.

Jun Li received the B.S. and Ph.D. degrees from the Harbin Institute of Technology, Harbin, China. He is currently a postdoctoral fellow at the School of Chemical Engineering, Georgia Institute of Technology, Atlanta, GA. His research interests include electroless plating, electroplating in microelectronics fabrication, battery, fuel cell, electrode materials, and electrochemical analysis.

Sue Ann Bidstrup-Allen received the S.B. degree from the Massachusetts Institute of Technology (MIT), Cambridge, MA, and the Ph.D. degree in chemical engineering from the University of Minnesota, Minneapolis, MN. She is currently a Professor with the School of Chemical and Biomolecular Engineering, Georgia Institute of Technology (Georgia Tech), Atlanta. Prior to her appointment at Georgia Tech, she and spent two years as a Postdoctoral Associate with the Electrical Engineering Department, MIT. Her research interests intersect the areas of polymer engineering, microelectronic materials, and processing. Dr. Bidstrup-Allen is a Fellow of the Society of Plastic Engineers and a recipient of the National Science Foundation Presidential Young Investigator Award, the DuPont Young Faculty Award, and the Georgia Tech Faculty Leadership Award.

Yoshitaka Fukuoka (M’02–SM’04) received the M.S. degree in electrical engineering and the doctoral degree in electrical engineering concerning MCM technology, both from the Nagoya Institute of Technology, Japan, in 1975 and in 1990, respectively. He joined Toshiba Corporation, Tokyo, Japan, in 1975 and developed MCMs for main frame in the computer division. He then joined the Research and Development Center of Toshiba Corporation to develop high-density packaging technology and 3-D mounting MCM technology for space and defense electronics and medical equipments. He moved to the printed circuit boards and Module division in Toshiba Corporation where he developed Buried Bump Interconnection Technology (B3ITM). He retired from Toshiba Corporation in 2002 and established a technical consulting company Worldwide Electronic Integrated Substrate Technology Inc. (Weisti). He is presently President of Weisti.

Dr. Fukuoka is a committee member of the International Microelectronics And Packaging Society (IMAPS), JIEP, IEEJ, and IEICE societies.