EPRI Technical Report

New Power Converter Topologies for Minimizing Energy Consumption of Electronic Appliances

[Product ID 2106AFU]

Final Report, June 2011

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ACKNOWLEDGMENTS

The following organization, under contract to the Electric Power Research Institute (EPRI), prepared this report:

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This report describes research sponsored by EPRI.

This publication is a corporate document that should be cited in the literature in the following manner:

New Power Converter topologies for Minimizing Energy Consumption of Electronic Appliances. EPRI, Palo Alto, CA: 2011. 2106AFU#.

ABSTRACT

The growth of consumer electronics in the household and office space has made electronic loads a significant portion of the grid. The total energy consumed by these appliances is typically governed by the energy losses in their idle mode or lightly loaded condition. The power supplies in these appliances are typically designed for thermal management at the maximum power point and with low cost in mind. Most power supplies have lower efficiencies at light loads than at their rated loads. If the unit spends most of its time at light load, then the energy consumption will be much higher compared to a situation where the power supply is optimized for overall energy consumption with a specified load cycle.

Considering that most electronic appliances are produced in high volume, the use of power supplies that permit easy custom design makes sense from the standpoint of energy efficiency. Over the past few years, multiple topological changes and design changes that aim to improve the efficiency of the power supplies have been proposed. However, not much work has been done to address the issue of reducing idle mode losses or to improve the efficiency of the power supplies at a low cost.

This work first builds up a business case to show that a market for low cost and high power rating electronic devices which exhibits high power efficiency exists. It then proposes a novel, yet simple, low cost solution to improve the efficiency of existing power supplies without major changes to their existing design. The claims are backed up by simulation results and a working prototype. Finally, a ROI model is presented to showcase the effectiveness of the proposed solution in today's consumer market.

The proposed novel device is just one example of how better design can significantly improve the efficiency of power supplies and still have a viable and profitable business model. It aims to overthrow misconceptions which associate higher efficiency with higher cost and thus pave the way for many more innovations to reduce the energy footprint of the low cost consumer electronics sector on the US power grid.

Keywords
Efficiency, consumer electronics, idle mode, power grid

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1
INTRODUCTION

The number of electronic appliances in households has increased significanltly in recent years. These appliances operate on dc power whereas the power grid supplies ac power. The appliances use either an internal or an external power supply to convert the power grid ac voltage to the required dc voltage levels. Most of these loads are plugged in to the wall permanently and cause significant parasitic losses, even when inactive. Such losses are referred to as standby losses.

Power supplies used in electronic appliances aren't designed for maximum power efficiency. Instead, their design is driven by cost considerations, optimum performance at the appliance's peak operating point, and the thermal efficiency of the power supply. Such a design methodology results in low, light load efficiencies. This presents an issue, since modern appliances spend most of their time in standby, which translates to a light load condition. The design of power supplies for peak operating point efficiency causes the energy losses of electronic appliances to be a lot higher than they should be. A strong case exists for a better and more adaptable design of power supplies used by electronic appliances.

The main aim of this project is to develop cost effective and efficient power supply design solutions that exhibit improved matching of load requirements over defined operating cycles. The main benefit would be to eliminate additional energy losses that occur during an electronic appliance’s standby mode or light load condition. It is also imperative that these solutions be minimally intrusive and easily adaptable to existing power supplies without incurring a high design overhead.

2
PROCEDURE FOR MEASUREMENT OF THE EFFICIENCY OF COMPUTER POWER SUPPLIES

Two products with high market penetration and high standby mode usage were chosen to strengthen the case that there exists a strong potential and market to improve the design of the power supplies in consumer electronics.. Preliminary investigations reveal that personal computers and printers would be the ideal markets for building the business case for low cost, high efficiency at low power mode power supply design. A varied mix of personal computers and printers were tested to measure their operating efficiency and estimate their energy consumption over a one year period. This chapter outlines procedure to accurately measure the operating efficiency of computer power supplies.

The continued introduction of multiple power converter topologies that drive widely varying loads at different voltage levels necessitates the creation of a standard procedure for measurement of power supply efficiency. This procedure would fulfill the dual purpose of helping the consumer in making an informed decision when purchasing a power supply and in helping the power supply designer in understanding power supply requirements. In addition to these two basic purposes, standardization also helps in quantifying the energy consumed in the power supplies on a nationwide scale and in understanding the benefits and effects of mitigating this loss. There exist numerous rating agencies, including EPRI , which oversee the measurement and quantification of the efficiency of power supplies and rate their energy efficiency with programs such as ENERGY STAR.

The existing procedures to test the power supplies consistently and accurately across different testing benches have been specified in [1] and [2].

Measurement Test Setup

The generic test setup to measure the efficiency of the power supply is proposed in [3] and is shown in Figure 2.1. The terms dictated by the standards [1] and [2] that are relevant in measuring the efficiency of the computer power supplies are also detailed below.

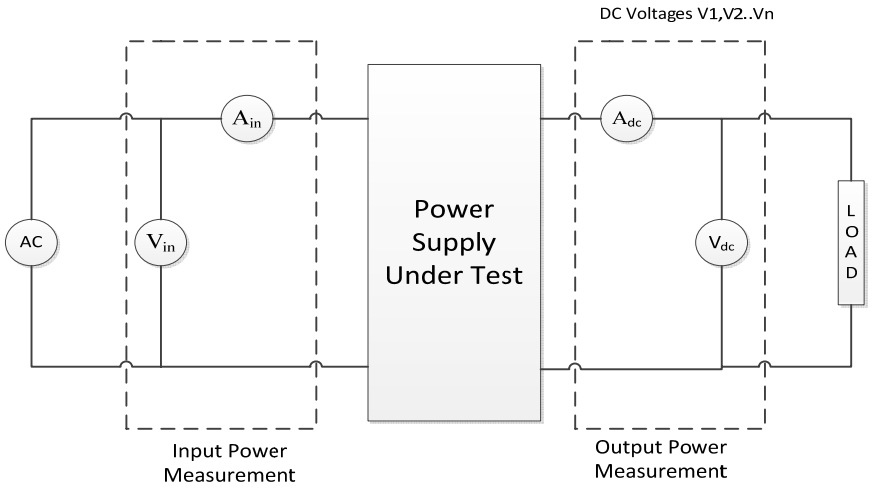

Figure 2-1
Generic Test Setup to Measure the Efficiency of Power Supplies [3].

The test setup consists of an ac voltage source on the input side which supplies the input power to the power supply under test. The standard [1] necessitates that the variation in input voltage should not be more than ±0.1% of the specified source voltage value and the THD should not exceed 2% up to and including the 13th harmonic [2]. The power supply is to be suitably loaded according to the testing procedures by an appropriate rheostat or another suitable dc current source. The dc loads must draw current with an accuracy of ± 0.5% within the current loading set point for each output voltage. The power measurements are to be made with suitably calibrated voltmeter and ammeter or power meters; measurements of power 0.5W or greater have to be made with an uncertainty of less than 0.5% at a 95% confidence level. The input power is to be computed using an averaging technique over a minimum of 32 input cycles and DC measurements for voltage should have an uncertainty of less than 0.1% and corresponding current measurements should have an uncertainty of less than 0.5%.

Existing Loading Procedure of Power Supplies

The loading criteria proposed by [3] for single output voltage systems is simple and based on rated dc output current and not on rated dc output power, i.e. 25% loading of a 100W, 5V, 20A system means the current source is adjusted to draw 5A of current from the system. However for multiple output voltage systems, the loading procedure is not as simple and requires use of sophisticated methods. A loading criteria based on a proportional allocation method proposed in [3] to load power supplies with multiple output voltages is explained in this section. According to the proportional allocation method each output is loaded proportionally, i.e. 20% loading means each of the outputs are loaded to 20% of their full load output value (e.g. a 5V, 20A output is loaded to 4A and a 12V, 10A output is loaded to 2A). Derating is applied in cases where the sum of individual maximum outputs exceeds the total rated output of the power supply.

The proportional allocation method helps in standardizing the efficiency measurement procedure, but has the disadvantage of being too general. In applications where the power supply

is always disproportionally loaded (e.g. one output is loaded more than the other outputs), this test procedure fails to provide an accurate model of the actual conditions under which the power supply is operating and therefore the measured efficiency does not correlate with the actual operating efficiency of the power supply. A different method to measure the efficiency of multiple output power supplies for specialized applications is detailed below.

Customized Efficiency Measurement for Computer Power Supplies

The efficiency of power supplies used in desktop computers has been measured in the past. The existing techniques are extremely generic and do not provide an accurate representation of the operating efficiencies of the computer power supplies. A different method for measuring the efficiency of computer power supplies was defined for this project. The block diagram of the setup used to record the efficiency of computer power supplies is shown below in Figure 2-2.

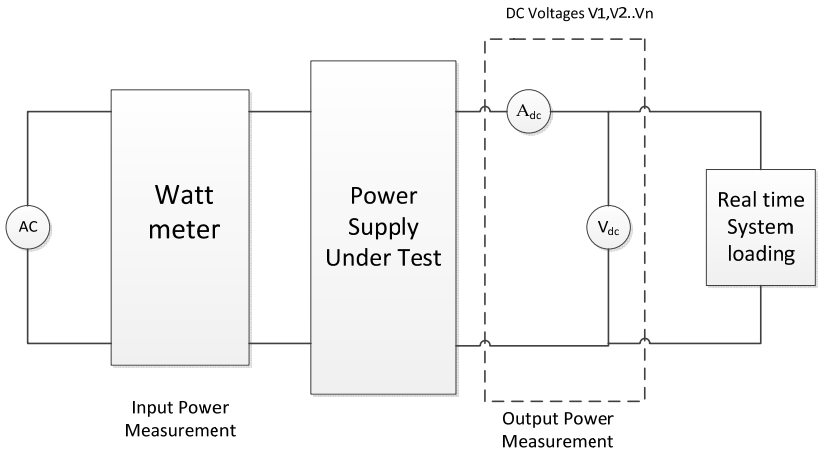

Figure 2-2
Online Energy and Efficiency Measurement Setup

The wattmeter measures the input power while the output power is measured with ammeters and voltmeters on the output load side. In the case of multiple output systems, such as computers, multiple ammeters and voltmeters are required to measure the output power. For a particular loading condition, the efficiency of the power supply is calculated as

$$\eta = \frac{\text{Output Power}}{\text{Input Power}}$$

The main difference between conventional efficiency measurement techniques and this method is measurement during real time operation rather than under laboratory conditions. This method of testing helps in computing the operational efficiency of the power supply rather than a worst case or best case efficiency. Computer loads are extremely variable and their operating point changes within milliseconds. In order to measure the efficiency accurately under real time loads, measuring instruments should have data logging capabilities to record the measurements so that input and output power measurements can be synchronized with each other and the efficiency can be measured over a wide range of operating points.

Figure 2-3
Watts up Meter monitoring the AC input power of Desktop Computers

A Watts-up meter was used to measure the input power and also to record the measurements for a considerable amount of time (nine hours of measurement with a resolution of one second). A picture of the meter is shown above in Figure 2-3.

To measure the output power, it is sufficient to measure the output current since the output voltage is fixed and has stringent regulation bands within which they operate. Measuring the output current for computer power supplies is difficult as there are multiple outputs coming out from the power supply and the space for monitoring the dc output non-intrusively is extremely limited. In this experiment, two or three clamp-on dc current measurement sensors (as much as the space constraint permits) coupled with data loggers were used to monitor the dc outputs for a fixed period of time for a typical operating cycle (loading) and this process was repeated for the same operating cycle and power supply until all of the dc output data was captured.

The typical operating profile for a PC load has to be defined so that it can be used to compare the energy consumed by different power supplies over a day. Commonly used PC software application tasks, like web browsing or running a video, were defined and the input and outputs of the power supplies were monitored to analyze the effect of the different applications on the operational efficiency of the power supply. Another advantage of defining a typical operating cycle is that it helps in computing the amount of energy lost in the power supply on a typical operating day. The energy loss difference for the different power supplies can be quantified by computing this loss for the same operating cycle for different power supplies. It provides vital information about the margin for energy savings through power supply design improvement.

A typical PC operating load cycle was defined and run manually. The operating cycle consisted of usage of internet based applications (browsing, mailing, web videos and games) for three minutes. This specific application was chosen since it provides a controllable mix of loads from idling (doing no active work), basic light level loading (checking e-mail, browsing) to extremely high loading (HD web streaming video) of the power supply and is also easily replicable.

Initially a sampling rate of one second was used. This caused inconsistencies between the input and output power measured (output power was greater than the input). A more in-depth analysis

of the data showed that one of the power supply outputs (12V) was changing very quickly (faster than 1 second) and the sampling rate of 1sample/sec was not fast enough for this output so the input and output power measurements obtained were not synchronized. The frequency of output variation was so high that with a 1 sample/sec sampling rate, the data recorded was instantaneous sample data (at random points over one second time period) and not the averaged value per second. All the dc outputs (5V, 3.3V, -5V and -12V) other than the 12V output were measured and logged using the current clamps and data loggers (one sample per second) whereas the data from the 12V output was logged using a Tektronix Digital Oscilloscope at a sample rate of 40,000 samples per second.

Using this procedure, desktop computer power supplies can be tested and a close approximation of their operating efficiency obtained.

3
MEASUREMENT OF EFFICIENCY AND ESTIMATION OF ENERGY WASTED IN COMPUTER POWER SUPPLIES

This chapter outlines the measurement of efficiency of computer power supplies in the market today, computes the energy waste projections on a nationwide scale and determines the feasibility to improve existing power supply designs such that the energy losscan be minimized.

Three power supplies were tested using the measurement setup and the operating cycle proposed in Chapter 2. The power supplies were carefully chosen so that they represented a good mix of devices that exist in the market today (from low end to high end). The configuration of the computer system used to load the power supply was an Intel Pentium D 82945G processor with 3GB DDR2 RAM, 80 GB Hard drive, 256MB RAM NVidia Graphics card and a DVD-CD-RW. The graphs showing the input and output characteristics for one of these power supplies is shown below in Figures 3-1 and 3-2.

Power Supply 1: Diablotek DA 350W Power Supply (Cost: $20)

PC loading: Usage of Internet based Applications for three minutes (23 – 49% of full load)

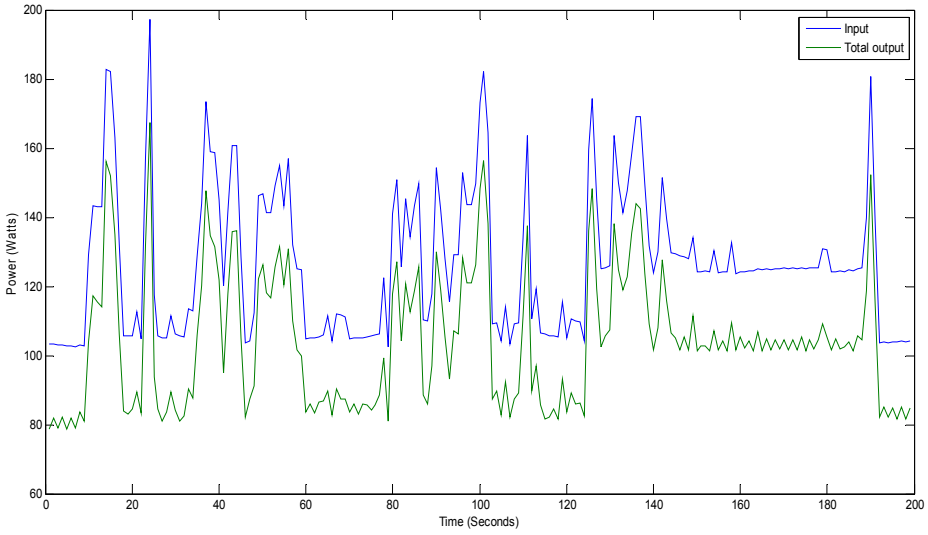

Figure 3-1
Input and Output Power Characteristics of the Diablotek Power Supply

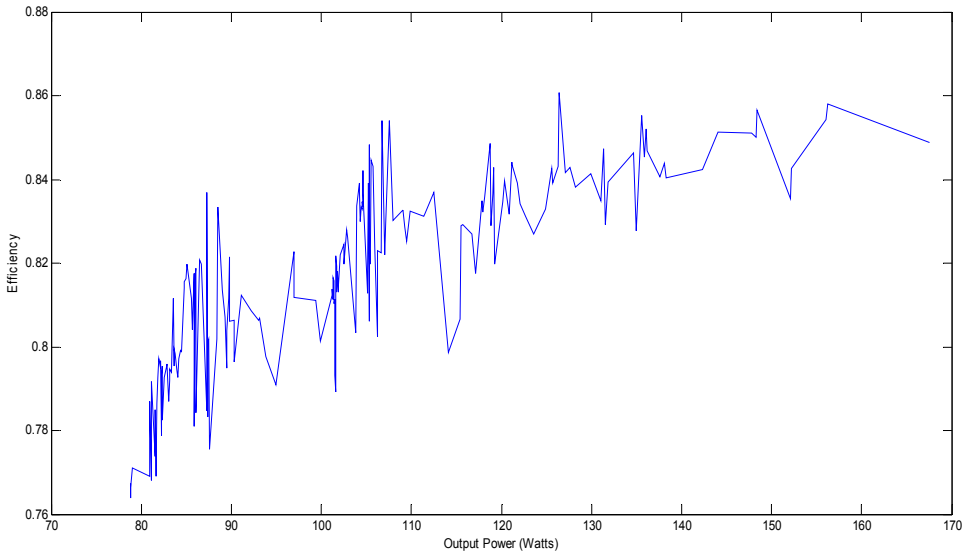

Figure 3-2
Efficiency vs. Output Power Characteristics of the Diablotek Power Supply

The average and idle mode efficiency and the input power factors for the three power supplies are shown below in Table 3-1.

Table 3-1
Summary of Test Results for the three Computer Power Supplies

	Diablotek 350W	Antec – Basiq 350W	Thermaltake Lite Power
Idle Mode Efficiency	74.5%	80.2%	85.9%
Average Efficiency	77.5%	82.5%	88%
Input Power Factor	0.55-0.6	0.58-0.64	0.96-0.99

Existing Energy Star 80 plus Efficiency Standards

The testing protocol of the Energy Star Program [3] recommends measuring the efficiency of the power supply under test at 20, 50 and 100 percent of full load output. They recommend a proportional allocation method for providing consistent loading guidelines for multiple output internal dc-dc power supplies, i.e. 20% loading means each of the outputs are loaded to 20% of their full load output value (e.g. a 5V, 20A output is loaded to 4A). Derating is applied in cases where the sum of individually maximum outputs exceeds the total rated output of the power supply The results from the above experiments show that under normal operation of personal computers, most of the power is being consumed by the 12V output of the power supply. Almost 75% of the load is consumed by the 12V output while the remaining 25% is shared between the 5V (20%), 3.3V (< 5%) and -12V (<1%) outputs. So 20% loading in this case is not 20% by proportional allocation, but 20% load as consumed by the personal computer itself. The efficiency measurement results obtained by following the Energy Star Program recommended

methods do not correlate with the results obtained and tabulated in Table 3-1, nor do they represent the actual operating efficiency of the power supply.

Energy Usage Projections per annum

To access the impact of energy lost in the different power supplies on a nationwide scale, it is necessary to calculate the energy use and waste projections from both households as well as commercial applications.

Energy Consumption Projections for Households

The data from [4] suggests that globally, in an average household, the computer is used 23 days a month on average. During this time, it is powered on for 7 hours and 34 minutes of which it is used effectively only for 2 hours and 51 minutes. The data also suggests that 63% of time spent by the user is on internet usage. The energy usage projections are computed by approximating (the other applications or loads also have an approximately similar profile as the internet usage profile) the entire effective usage time of the user to their internet usage. The energy usage and waste computations and projections for power supply 1 (Diablotek) during the active mode of operation is shown below. The computations are performed using the data from Figures 3-1 and 3-2.

Energy spent during three minutes of active usage = 8.34 Watt-hours

Energy wasted during three minutes of active usage = 1.86 Watt-hours

Approximate Projection of Energy spent per year = 5.7 kWh

Approximate Projection of Energy wasted per year = 1.27 kWh

The energy usage and waste projections during the power supply's idle mode of operation are shown below. Idle mode of operation for the computer is defined as the time during which the processor of the computer is doing no active work [5].

Time spent idling in a year = (7 hrs 34 mins – 2 hrs 51 mins)*12 = 56 hrs and 36min

Energy spent in idling time = 113.8 *56.6 = 6.44 kWh

Energy wasted during idling = (113.8 – 85.3) * 56.6 = 1.61 kWh

This computation is performed for the other two power supplies as well and the calculations are shown in Appendix A. Table 3-2 below shows the energy usage and waste projections for all three power supplies for the household application. The projections are very conservative.

Table 3-2
Energy Waste Projections for Computer Power Supplies

	Diablotek 350W	Antec – Basiq 350W	Thermaltake Lite Power
Energy wasted idling (kWh/year)	1.61	1.21	0.76
Energy wasted in active mode (kWh/year)	1.27	0.92	0.58

Assuming 60% of the US population has access to computers and 25% of them use the computers regularly, then the amount of energy wasted in power supplies per annum in US households in idle mode is approximately 34GWh/year.

Energy Consumption Projections for Households

The results of a survey [31] conducted on computer usage time in offices s in the US under various power modes are presented below in Table 3-3.

Table 3-3
Time Spent by Computers under Various Power Modes

	Hours per day spent in Sleep	Hours per day spent in Idle Mode	Hours per day spent in active mode
Without Power Management	0.0	23.3	0.7
With Power Management	16.0	7.3	0.7

Energy Waste Projections for three different power supplies computed using data from Table 3-3 are given below:

Table 3-4
Energy Waste Projection for Computer Power Supplies in Offices

	Diablotek-350W		Antec – Basiq 350W		Thermaltake Lite Power	
	Energy wasted idling (kWh/year)	Energy wasted in active mode (kWh/year)	Energy wasted idling (kWh/year)	Energy wasted in active mode (kWh/year)	Energy wasted idling (kWh/year)	Energy wasted in active mode (kWh/year)
Without Power management	242.37	9.51	181.4	6.89	114	4.35
With Power Management	75.94	9.51	56.83	6.89	35.73	4.35

The results from Table 3-4 show that a considerable amount of energy is being wasted in these power supplies, especially during the idle mode of operation. Even assuming a modest number of

10 million office computers, the amount of energy wasted in the high end power supplies with power management is 350GWh/year in the idle mode of operation alone.

These results clearly indicate that there is great potential to improve the efficiency of the computer power supply and that even one watt of energy saved would have a tremendous impact.

4
TESTING OF PRINTERS AND ESTIMATING THEIR ENERGY CONSUMPTION

Many other electronic loads, like printers, microwaves, LCD Televisions, cell phone chargers, etc. also show a wide range in average to peak power useage. It is likely that the power supplies in these devices were designed for maximum power delivery point and may have poor efficiency at lower power levels. It is important to research potential for energy use reduction through power supply redesign for these high penetration electronic loads. In The above applications were tested and it was determined that, other than for the printers, the light load energy consumption of the rest of appliances was extremely low. This chapter provides the results from testing of various printers ranging from household use to commercial multifunction printers and their energy consumption is projected to investigate the potential for energy consumption reduction.

Market Research

The data from [6] suggests that in the second quarter of 2010 alone, the sales of printers worldwide amounted to 29 million units. The US alone accounted for 6.5 million units of sales. The laser segment accounted for 27% of the market share or 7.8 million units. [6] Multi-functional printers (MFPs) took up 62% share in the laser segment or 4.8 million units [6]. This data suggests that the printer market is huge with sales of commercial grade MFPs in the US alone amounting to 1 million units and basic MFPs, 3.3 million units.

Energy Consumption of Printers

With such a large market share, even one watt of continuous energy waste in these printers amounts to 226GWh of energy waste per year in the US alone in the newly sold printers. This data suggests that there may be a potential for energy consumption reduction in the printers. However a wide variety of sample data from testing different types of printers is required to justify the cause. The energy consumption of one basic laser jet printer and three commercial grade multifunctional laser jet printers were monitored and the results are detailed in the sections below.

Energy Consumption and Projection of Basic Laser Jet Printer

A HP Laser Jet 4250 printer (printer 1) was tested to determine the amount of energy consumed under various load cycles. The power consumption cycle of the HP Laser Jet 4250 for printing a single sheet of paper is shown in Figure 4-1.

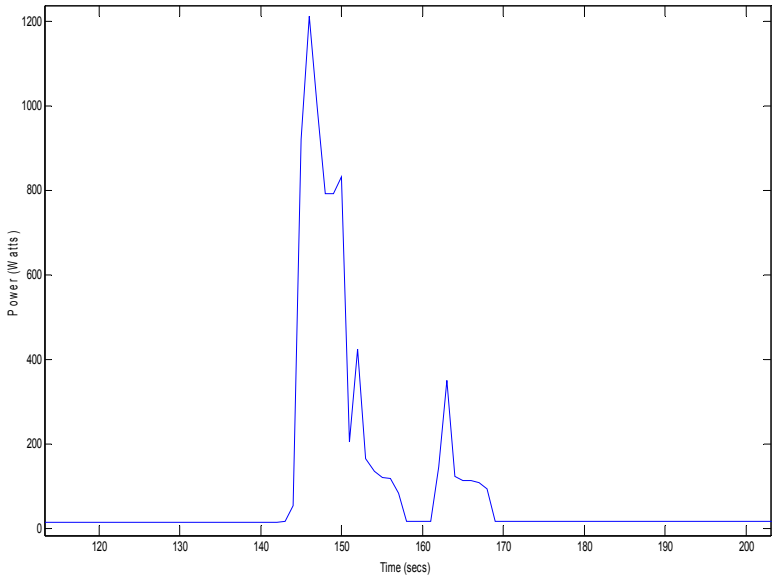

Figure 4-1
Power Consumption Cycle of a Printer for Printing one Sheet of Paper

The power consumed by this printer in its idle state is 17W.To measure the amount of energy consumed by the printer for actively printing different quantities of paper, the energy consumed for printing 1, 2, 3, 4, 5 and 10 sheets of papers was measured. The results of the experiment are shown below in Table 4-1 and Figure 4-2.

Table 4-1
Energy Consumed by Printer 1 for Printing Different Quantities of Paper

Sheets of Paper Printed	1	2	3	4	5	6
Energy Consumed (Watt Hours)	2.23	2.45	2.78	3.18	3.50	5.11

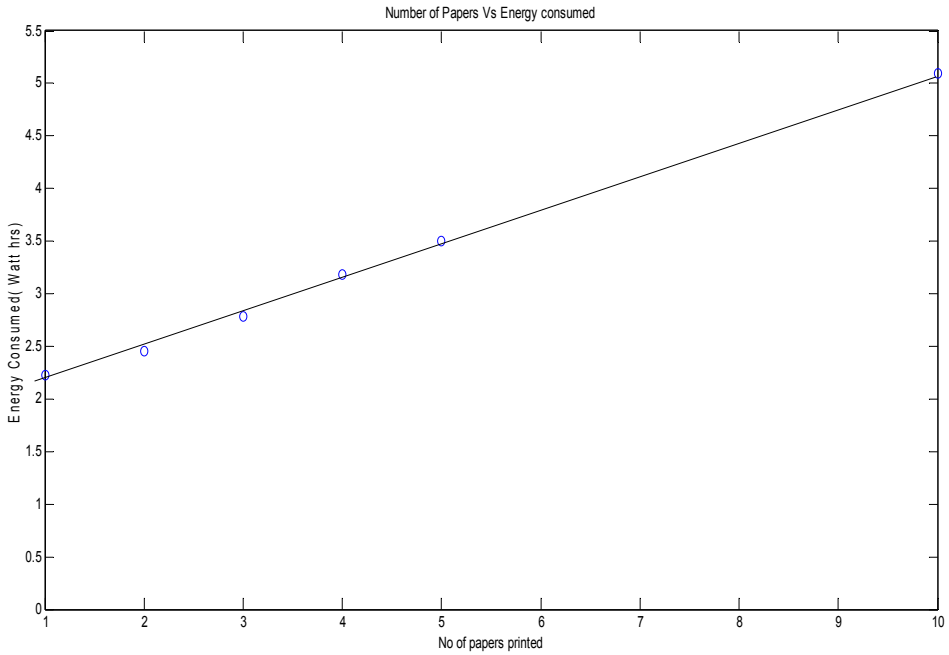

Figure 4-2
Plot showing the Energy Consumed by Printer 1 for Printing different quantities of Paper

Printing the first sheet of paper consumes 2.23 Watt-hours of energy and for every additional sheet approximately 0.22 to 0.32 Watt-hours is consumed. The response is almost linear and the amount of energy this printer will consume for printing any arbitrary number of sheets of paper can be predicted. The power and energy consumption of the printer 1 under different modes of operation have been tabulated in Tables 4-2 and 4-3. The idle mode, standby mode and the energy saver modes or states of operation for the printer are detailed in the sections below.

Table 4-2
Power Consumed by Basic Laser Jet Printer in Idle Mode of Operation

	HP Laser Jet 4250
Power Consumed in Standby Mode	19W
Power Consumed in Energy Saver Mode	17W

Table 4-3
Energy Consumed by Basic Laser Jet Printer while Printing

	HP Laser Jet 4250
Energy consumed to print a single sheet of paper	2.23Wh
Energy consumed to print the next sheet of paper	0.23-0.32Wh

Energy Usage Projections (per annum)

The loading cycle of the printer 1 was monitored on a busy weekday to compute the energy usage projections per annum for the given printer. The results of the experiment are shown below in Figure 4-3.

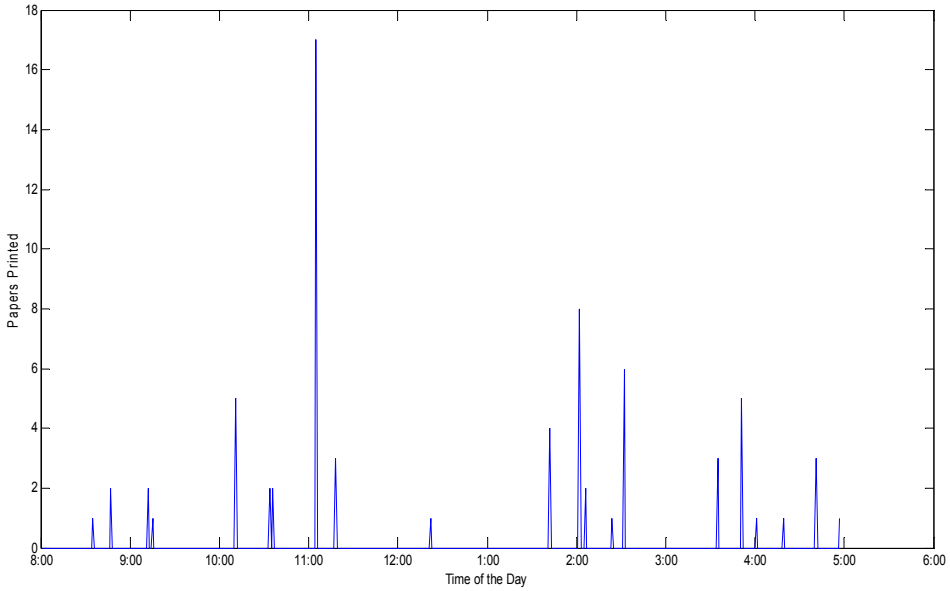

Figure 4-3
Load Cycle of HP Laser Jet Printer 4250 for One Day

It was assumed that the printer is used actively for five days of the week, fifty two weeks of the year and that the daily load cycle is the same throughout the year**.**

The energy consumed by the printer in a day in its active mode is 62.8 Watt-Hours (load cycle shown in Figure 4-3) and the energy consumed by the printer in a day in its idle mode is 408 Watt-Hours (17W × 24 hours). The projected energy consumed by the printer in a year is computed and the results are shown in Table 4-4.

Table 4-4
Projected Energy Consumed by Printer 1 (per annum)

Mode of Operation	Energy Consumed per Year	Energy Consumed by 13.2 Million units of basic MFPs
Active Mode (used 5 days of the week)	16.3kWh	216GWh
Idle Mode (used 7 days of the week)	149kWh	1964GWh

It can be clearly seen from the results shown in Table 4-4 that the amount of energy consumed by the basic laser jet printer is substantially more in the idle mode of operation than when the printer is being actively used (for this particular load cycle).

Energy Consumption and Projection of Commercial Grade MFPs

The energy consumed by three commercial grade multi-functional printers under different modes of operation was measured using the Watts-up power meter. The power and energy consumed by the Ricoh-Atcio MP4000 laser jet printer over a 10 minute period of time is shown in Figure 4-4.

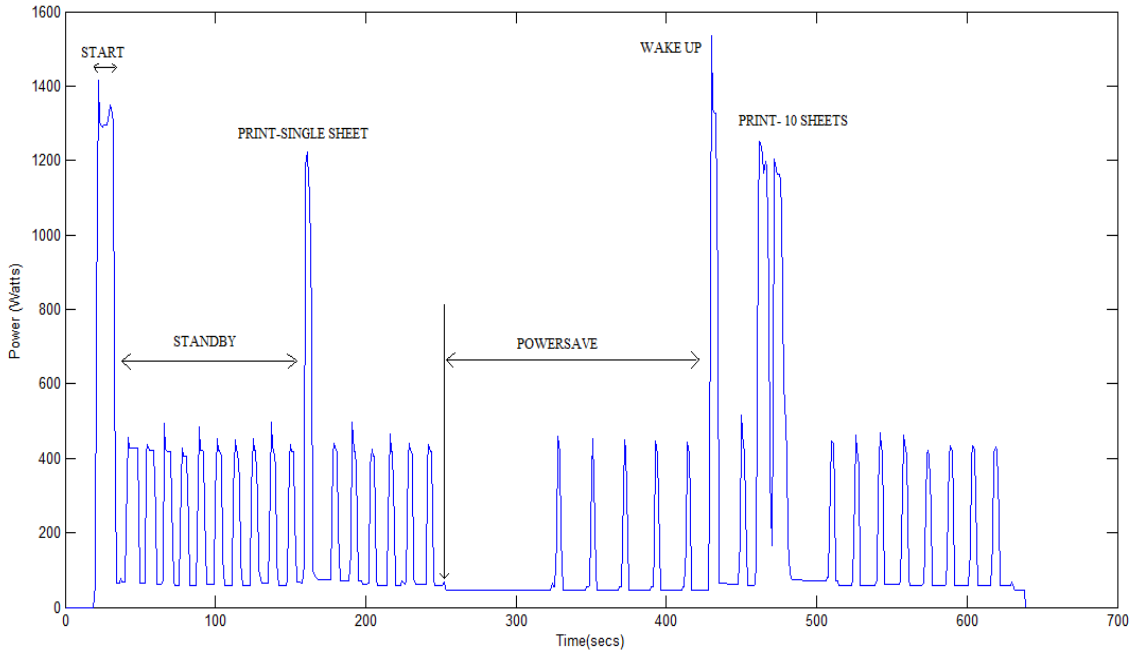

Figure 4-4
Power and Energy Consumed by Ricoh-Atcio-MP 4000 Laserjet MFP under Different Modes of Operation

When a printer is perfroming active work such as printing, it is defined to be in its active mode of operation. From Figure 4-4, it can be seen that even when the printer is not printing and is in its standby mode of operation, power is still being consumed. This is because the printer

consumes energy every few seconds during the standby mode to maintain the temperature of its fuser.If the fuser is not maintained at a particular temperature, when the print command is given, it would take some time for the printer to heat up the fuser before starting to print. The energy saver mode in this printer saves energy by maintaining the fuser at a lower temperature than in the standby mode. The definition of energy saver mode and standby mode may vary from printer to printer. Some new models use instant on fuser whereby the standby and energy saver modes do not have to maintain the fuser at a particular temperature reducing the energy consumed during these modes. The common factor in all of the printers is that during the standby mode and energy saver mode of operations, the printer is not doing any useful work and consumes significantly lesser power than in their active modes. The modes of operation of a printer can be broadly classified into active mode operation and idle mode operation (standby and energy save modes).

The power and energy consumed by the three commercial grade MFPs under different modes of operation are shown in Tables 4-5 and 4-6.

Table 4-5
Power Consumed by Commercial MFPs in Idle Mode

	Ricoh Atcio MP4000	Konica Minolta Bizhub 420	Oce im3512
Power Consumed in the Standby Mode	145W	180W	185W
Power Consumed in the Energy Saver Mode	95W	56.6W	66.5W

Table 4-6
Energy Consumed by Commercial MFPs while Printing

	Ricoh Atcio MP4000	Konica Minolta Bizhub 420	Oce im3512
Energy consumed to print a single sheet of paper	1.65Wh	1.42Wh	1.76Wh
Energy Consumed to print a single sheet of printer (double sided printing)	2.48Wh	2.19Wh	2.94Wh

Energy Usage Projections (per annum in US)

To estimate the energy consumed by these printers over a period of a year, the printers have been assumed to operate on a very heavy duty cycle printing a hundred thousand sheets per year. The estimated energy usage calculations are shown for the Ricoh-Atcio-MP4000 laser jet printers. To estimate worst case scenarios, each print is assumed to be in cycles of 10 pages. The energy and time consumed for printing 10 sheets of paper in this printer has been experimentally computed to be 6.57Wh and 20 seconds respectively. The printer is assumed to be in power save mode for 16 hours a day and in standby mode for 8 hours a day (i.e. when not in active operation).

The energy consumed for printing one hundred thousand sheets per year is 65.7kWh (10,000 sets of 10 sheets × 6.57Wh/10sheets). The time consumed for printing one hundred thousand sheets is approximately equivalent to three days (20s × 10,000 / (3,600 × 24)) of continuous usage of the printer. Then the energy consumed by this printer in its idle mode per year is 973kWh per year ((95Wh×16 hours/day + 145Wh×8 hours/day) × (365-3) days).

The energy projection computations are performed similarly for the other two MFPs and the results are shown in Table 4-7.

Table 4-7
Energy Usage Projections for Commercial Grade MFPs per annum

	Energy consumed per annum (kWh)		
	Ricoh Atcio MP4000	Konica Minolta Bizhub 420	Oce im3512
Active Mode (One hundred thousand sheets per year)	65.7	55	71
Idle Mode	973	850	935

To calculate the overall energy consumption in the commercial grade printers sector, total sales of 4 million units (1 million per quarter) are assumed to be distributed equally among the three tested MFPs. The energy consumed by 4 million units of the commercial grade MFPs per year in active mode is 256GWh ((65.7 + 55 + 71) kWh × 4 million units × 0.333). The energy consumed by 4 million units of commercial grade MFPs per year in idle mode is 3,680GWh.

It can be clearly seen that the energy being consumed even in the worst case biasing (towards active mode) is higher in the idle mode of operation. From the results obtained in this chapter, it can be seen that there clearly exists a potential to reduce the energy being consumed by these printers in their idle mode of operation.

5
PROBLEM IDENTIFICATION AND PROPOSED SOLUTION

The results from Chapters 3 and 4 suggest that there is a considerable amount of power being consumed and wasted in printer and desktop computer power supplies, especially at light load. There is a clear potential for redesigning the power supplies for better efficiency.

One of the main aims of this research work is to identify a component inside the power supply which is a major contributor to the overall losses and that can be redesigned to improve the overall efficiency using minimal design changes and at minimal cost. The motive is to establish a business case for high efficiency, lower cost power supplies.

Identification of Loss Components of the Power Supply

To redesign the power supply, it is necessary to determine which elements of the power supply are lossy, whether the losses are concentrated or distributed and how cost effectively can these losses be removed. The mid-cost range Antec 350W power supply was broken down and the circuit was removed from its housing. From the circuit board, the circuit of the power supply was retraced. A general block diagram of the power supply in open loop mode is shown in Figure 5-1.

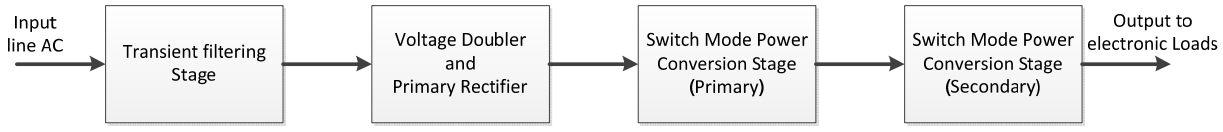

Figure 5-1
Basic Block Diagram of a Commercial Switch Mode Power Supply

The switch mode power supply used here consists of four main operational stages:

1. Transient Filtering Stage - The input line ac is filtered to remove grid transients and to prevent noise generated from within the circuit from entering into the power line.

2. Voltage Doubler and Primary Rectifier - This stage doubles the voltage if the ac input source used is 120V and proceeds to rectify and filter this ac voltage.

3. Switch Mode Power Conversion Stage (Primary) - One of the many dc-dc power converter topologies is used in a switching configurationto convert the rectified output (dc) from the previous stage into high frequency ac.

4. Switch Mode Power Conversion Stage (Secondary) - The outputs from the previous stage are stepped down using a high frequency transformer and then rectified, filtered and output to the electronic loads

The transient filtering and voltage doubler stages consists of filter elements like ferrite coils, inductors, capacitors, resistors and protection elements like fuses. The power loss in these circuits are minimal and limited to just the losses in their equivalent series resistance (esr). The primary rectification stage consists of diodes and capacitors which rectify and filter the input ac into dc. The diodes in this stage conduct current only for a very small period of time, once in every 10-15 cycles depending on the value of the input capacitor. The losses in this stage should also be small. The majority of the power appears to be lost in the switch mode power supply in the switching elements of the power converter stage.

To confirm this hypothesis and find the actual components or parts of the circuit in which most of the energy is wasted, the circuit schematic of the power stage of the Antec-350W Power supply was simulated using MATLAB in open loop mode. The circuit schematic of the power stage of this power supply used in the simulations is shown in Figure 5-2. The simulation results were then used for computation of losses. The losses were computed for three operating points of the power supply ranging from idle mode (mode 1), mid-scale output (mode 2) and peak output conditions (mode 3). The losses in the various elements of the power supply under these three modes of operation are shown in Table 5-1.

Table 5-1
Loss in Various Elements of the Power Supply under Three Modes of Operation

S. No	Elements	Mode 1	Mode 2	Mode 3
1	Input diode bridge	0.5W	0.86W	1.16W
2	Input Power Switches (Conduction)	0.9W	1.56W	2.1W
3	Input Power Switches (Switching)	2.4W	4.2W	5.66W
4	Output Diode Rectifiers	8.79W	13.29W	15.86W
5	Resistances	4.2W	4.2W	4.2W
6	Cooling Fan	2W	2W	2W
	Total Estimated Loss	18.8W	26.1W	31W
	Actual loss	20.1W	27W	33W

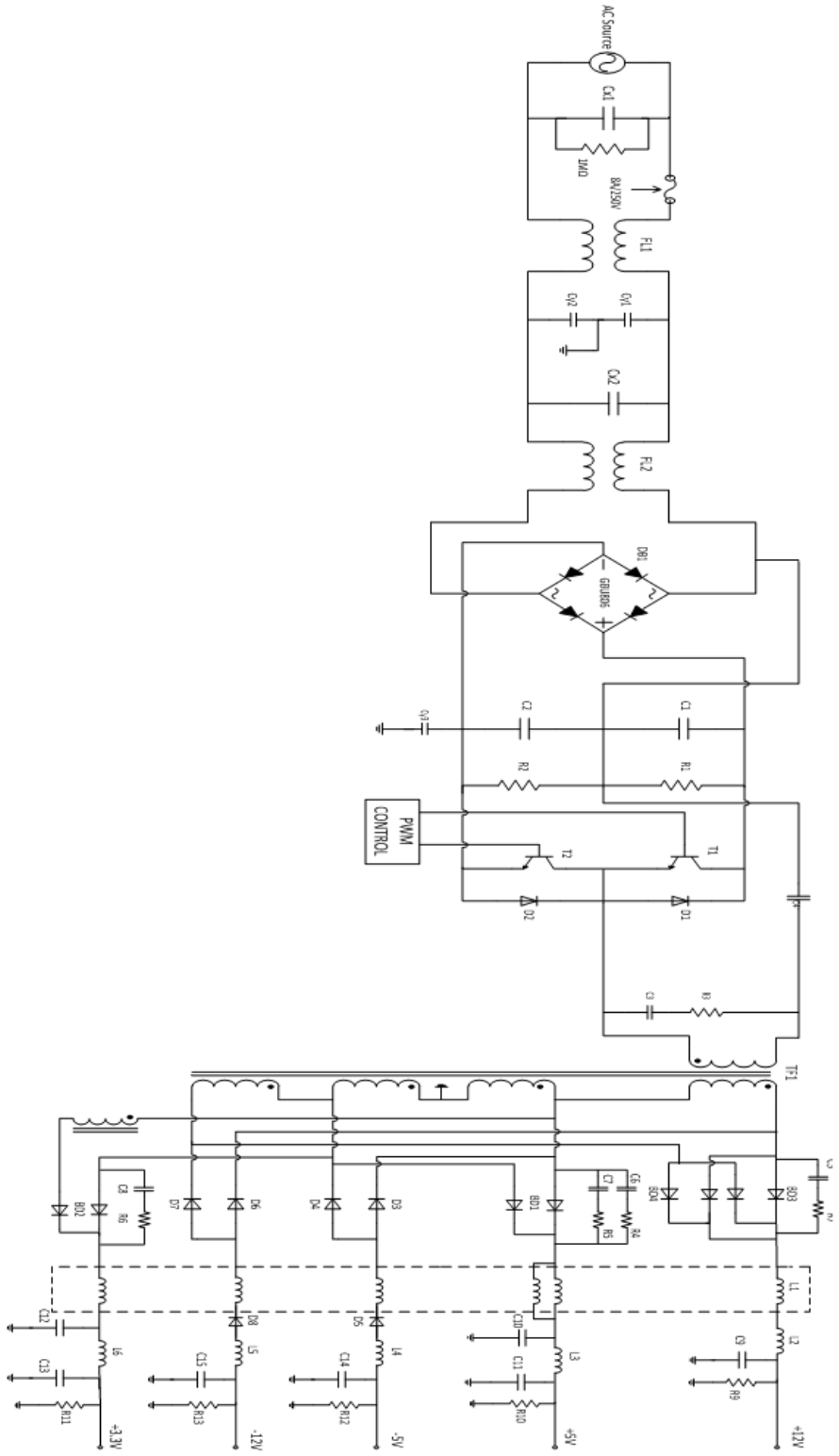

Figure 5-2
Schematic of the Power Stage of the Antec-350W Power Supply

The losses in the power supply under study have been classified into six major areas. The first three areas belong to the input side circuit of the power supply and are fairly distributed. The losses in the resistances and cooling fan are due to extremely cheap and careless design and can be easily eliminated by using simple design changes or better control methods.Most power supplies in the market eliminate this loss. However a major portion of the losses is concentrated in area four (diode rectifier). Since the computer and printers present a low voltage, high current load, the losses in the diode rectifier are further exaggerated.

The results of Table 5-1 and the analysis performed above shows that the diode rectifiers are the biggest contributors to the energy loss in the power converter. A solution which targets elimination of this loss would definitely have a large impact. A simple solution to this problem to eliminate the diode rectifier loss is to replace the diodes with synchronous rectifiers operating in the third quadrant [7]. The synchronous rectifier is an electronic switch (mostly MOSFET) that is gated and controlled to operate just like the diode.Because of its low on-state resistance the power loss across the synchronous rectifiers is extremely low, especially at low loads.

The concept of synchronous rectifiers has existed for more than 25 years and yet the adoption rate into the market has been extremely low and limited to the expensive high end power supplies. Green energy initiatives by various organizations such as Energy Star, etc. have increased the research in this arena, but still most of the power supplies use diode rectifiers. The main reason for slow adoption is it is expensive if rated for the full rated current. It also requires control,additional sensing, and complex control circuitry. Any implementation of the synchronous rectifier would require design changes to control circuits and algorithms, introducing additional components in the already crowded power supply circuit board in addition to the increased cost of control circuits and the synchronous rectifier.The cost of the synchronous rectifier has been steadily decreasing with advances in semiconductor technology and can be expected to decrease further if economies of scale are introduced.

The results shown in Chapters 3 through 4 clearly indicate that losses in the standby mode of operation of the devices employing a power supply far exceed the losses during the active mode of operation as the device spends most of its time in standby or sleep or idle mode of operation. Therefore using an expensive synchronous rectifier rated for full load current when the device is actually going to operate under light load conditions for most of its life is not an efficient design.

Proposed Solution

A two terminal device is proposed which can be paralleled with the existing diode and controlled in such a way that under light loading conditions, the synchronous rectifier operates and eliminates the rectifier loss. Under high current mode of operation, the diode conducts and the circuit operates as if the synchronous rectifier was not there. A low current synchronous MOSFET could then be used which would decrease the cost of the proposed solution but would have maximum impact on energyconsumption. The proposed device is completely self controlled and does not require external circuitry [8]-[9]. All of the sensing that is required to control the synchronous rectifier and operate as a diode are obtained from the voltage information across the two terminals of the device. This solution is minimally intrusive as it can be directly paralleled with the existing diode rectifier, or in some cases, even replace the existing rectifier. No change

of existing control circuitry, algorithms or design change of the power supply board layout is required. This solution is also topology independent as the two terminal device tries to emulate the diode operation exactly. The proposed solution addresses all of the challenges that have prevented entry of synchronous rectifiers into the main stream, low cost power supply market.

The two terminal SSSR (Self Sufficient Synchronous rectifier) device not only provides the logic to control the on-chip synchronous rectifier, but also the control power for the logic devices and to drive the synchronous rectifier. The basic block diagram of the proposed SSSR device is shown below in Figure 5-3.

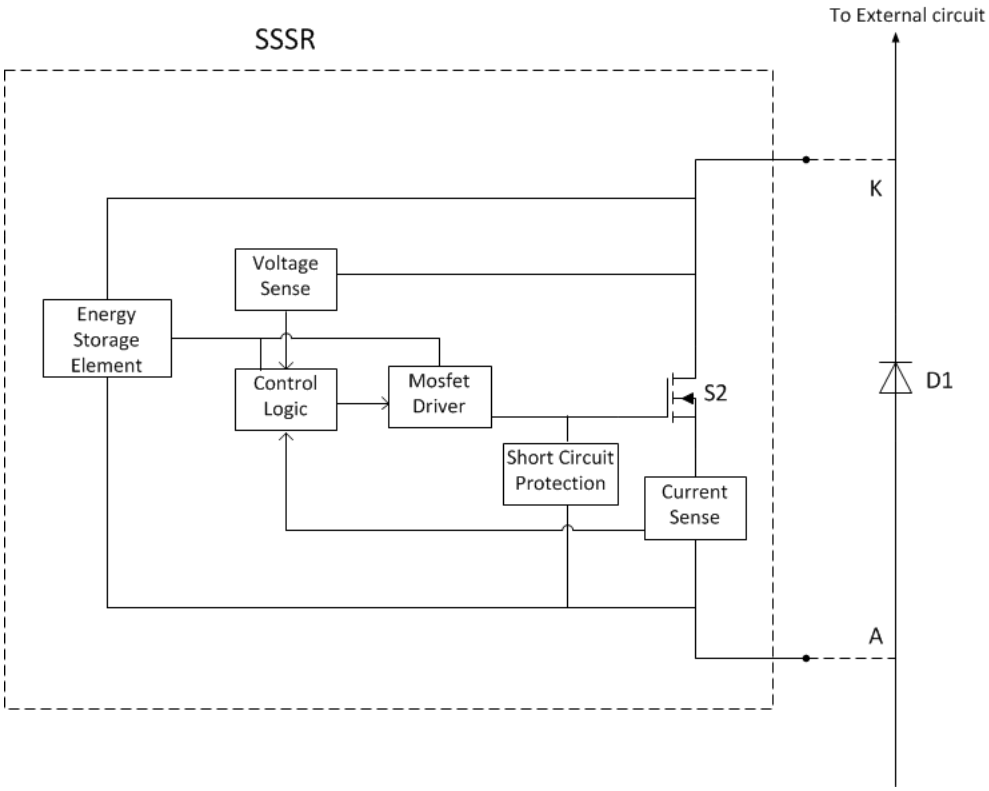

Figure 5-3
Block Diagram of the Proposed Self Sustained Synchronous Rectifier (SSSR)

Operation of the SSSR

The SSSR is a two terminal device that tries to emulate the exact operation of the diode. The active element in the SSSR is a synchronous rectifier S2 which is controlled appropriately to mimic the operation of the diode. The device senses the voltage across the synchronous rectifier and the current through it to control the rectifier appropriately. When the primary switch is conducting, the voltage V_{AK} across diode D1 and the SSSR is less than zero. The SSSR control senses this and prevents the synchronous switch S2 from turning ON for the entire period when the primary switch is ON. However during this period, the energy from the external circuit is stored in the energy storage element of the SSSR. This energy is used to power the control and

drive circuits of the SSSR when the synchronous switch is turned ON. The block diagram of the SSSR under this mode of operation is shown in Figure 5-4.

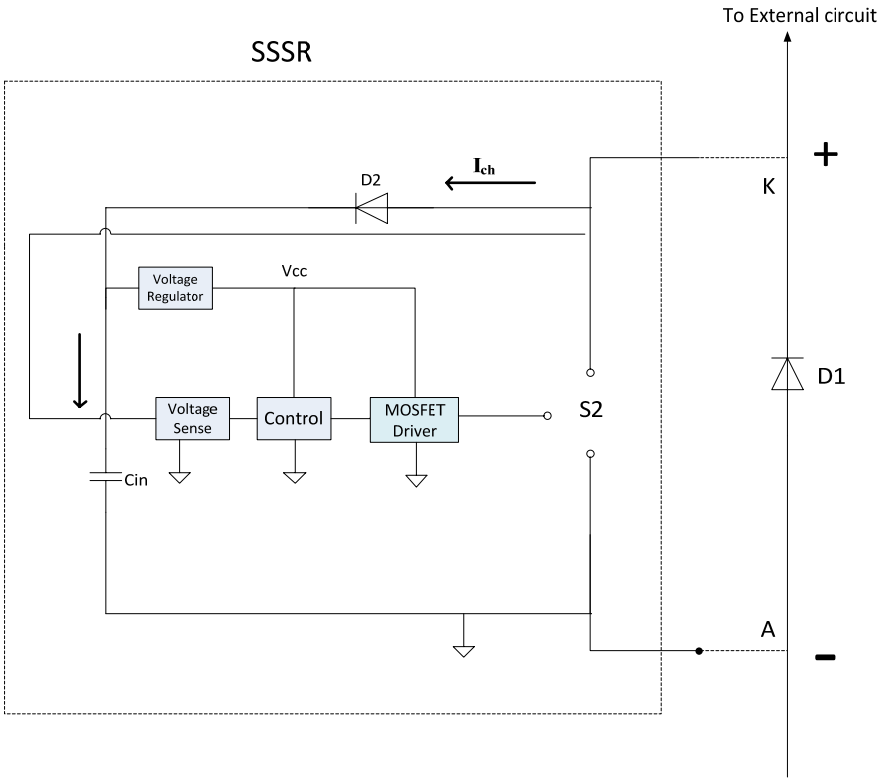

Figure 5-4
Operation of the SSSR when $V_{AK} < 0$

During light load operation (when the power supply is operating in standby, idle or sleep modes) when the current through the device ($I_{SW} = I_{LOAD}$) is less than a reference current I_{REF} (or equivalently $V_{AK} < V_{REF}$, where $V_{REF} = I_{REF} \times R_{DS\,(ON)}$), the SSSR is turned ON and it operates instead of diode D1, removing almost all of the losses across the otherwise lossy diode rectifier. However when the load current increases above I_{REF} , the SSSR turns off and allows the diode carry the load current. Now the circuit operates as if the SSSR were not present in the circuit and losses in the power supply remain the same as before (plus additional control power loss for the SSSR, which is very low). These two modes of operations are illustrated below in Figures 5-5 and 5-6.

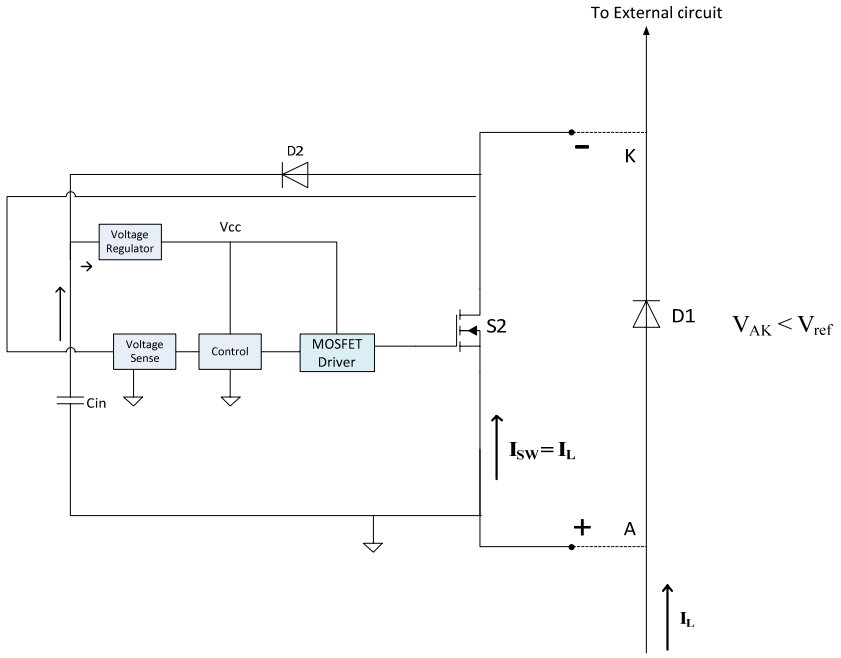

Figure 5-5
Block diagram of the SSSR when V_{AK} > 0 and the Load Current (I_L) is Less than the Reference Current (I_{REF})

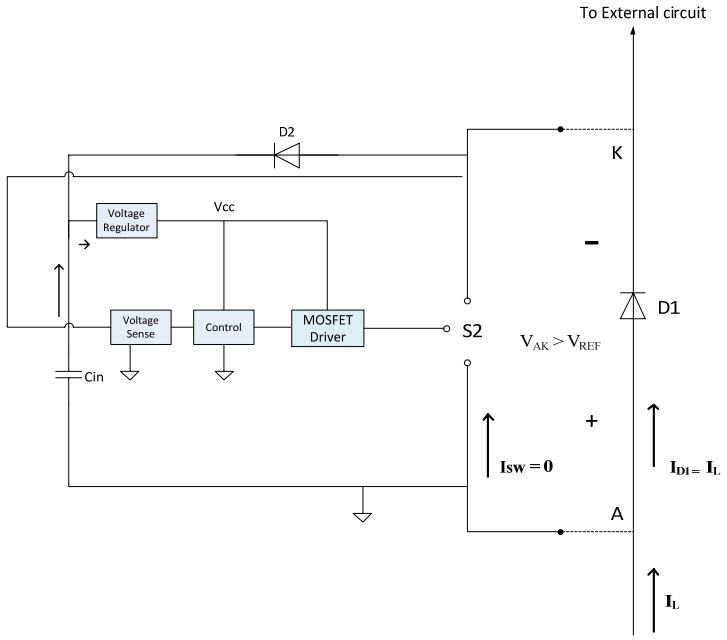

Figure 5-6
Block diagram of the SSSR when V_{AK} > 0 and the Load Current (I_L) is Greater than the Reference Current (I_{REF})

The control logic used to control the SSSR is summarized in the Table 5-2 below.

Table 5-2
Control Logic for the SSSR

S. No	Voltage across the device (V_{AK})	Load Current (I_L)	State of the SSSR
1	$V_{AK} < 0$	Any	OFF
2	$V_{AK} > 0$	$I_L < I_{REF}$	ON
3	$V_{AK} > 0$	$I_L > I_{REF}$	OFF

Test Bed

A test bed was required to implement the SSSR and test its effectiveness. A simple buck converter was used as the test bed. The circuit diagram of the Buck converter and its corresponding operating conditions are shown in Figure 5-7.

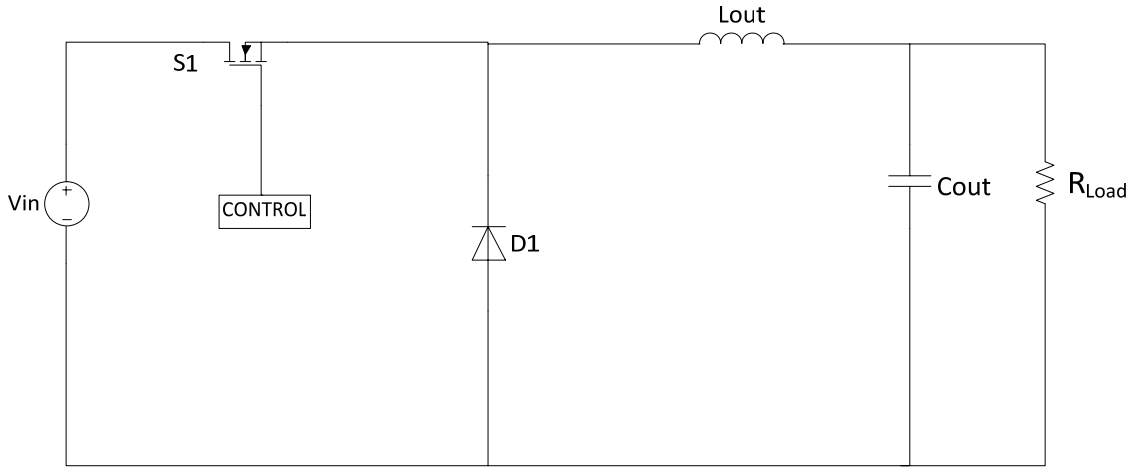

Figure 5-7
Basic Buck Converter

The SSSR is used to replace the free-wheeling diode D1 and evaluate its effectiveness. The circuit diagram of the SSSR implemented on the conventional buck converter is shown below in Figure 5-8.

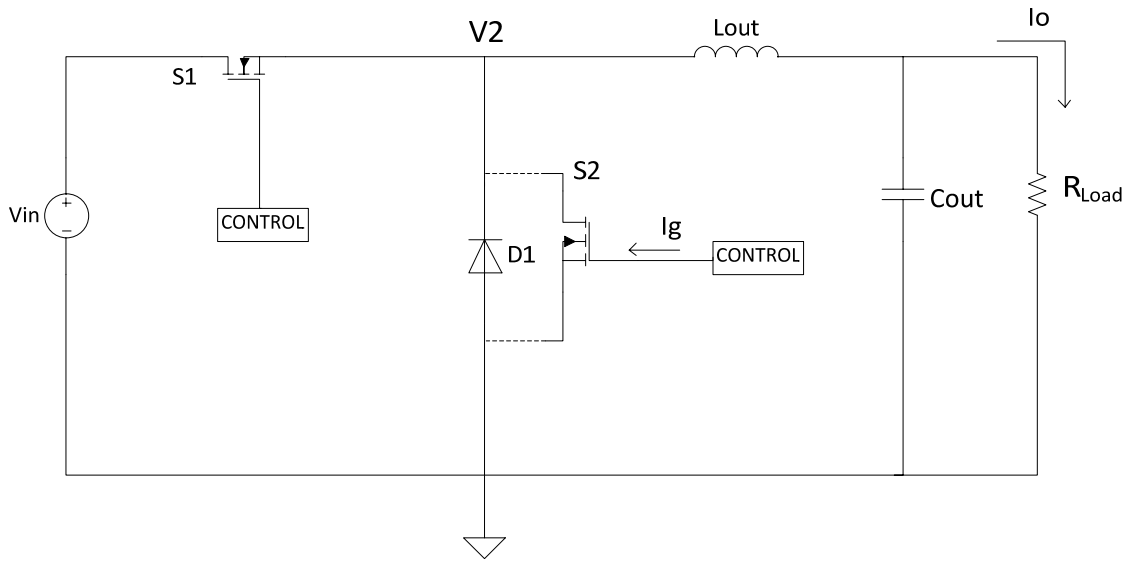

Figure 5-8
SSSR implemented on the conventional Buck Converter

The simulation and experimental results in implementing the SSSR on the test bed are detailed in the following chapter.

6
SIMULATION AND EXPERIMENTAL RESULTS

Simulation Results

The SSSR and corresponding test bed circuitry were implemented and simulated using the SABER simulation package. The circuit parameters and operating conditions used in the simulation are summarized below in Table 6-1.

Table 6-1
Circuit Parameters and Operating Conditions used in the Simulation Circuit

S. No	Circuit Parameter	Value
1	Input Voltage (Vin)	10V
2	Unregulated Output Voltage (Vout)	5V
3	Switching frequency	10kHz
4	V_f of freewheeling diode D1	1.8V
5	$R_{DS\ (ON)}$ of Synchronous MOSFET used in SSSR	200mΩ
6	Reference Current (I_{REF})	1A

The simulation results obtained are shown below in Figures 6-1 and 6-2. When the primary switch is turned OFF, initially the body diode starts to conduct as shown in 6-1. However this is sensed by the SSSR which immediately turns ON the synchronous rectifier switch of the SSSR. Now, the body diode's voltage gets clamped by the conduction voltage of the synchronous switch which is less than the ON state forward voltage drop of the diode (V_f) and hence the diode remains turned OFF.

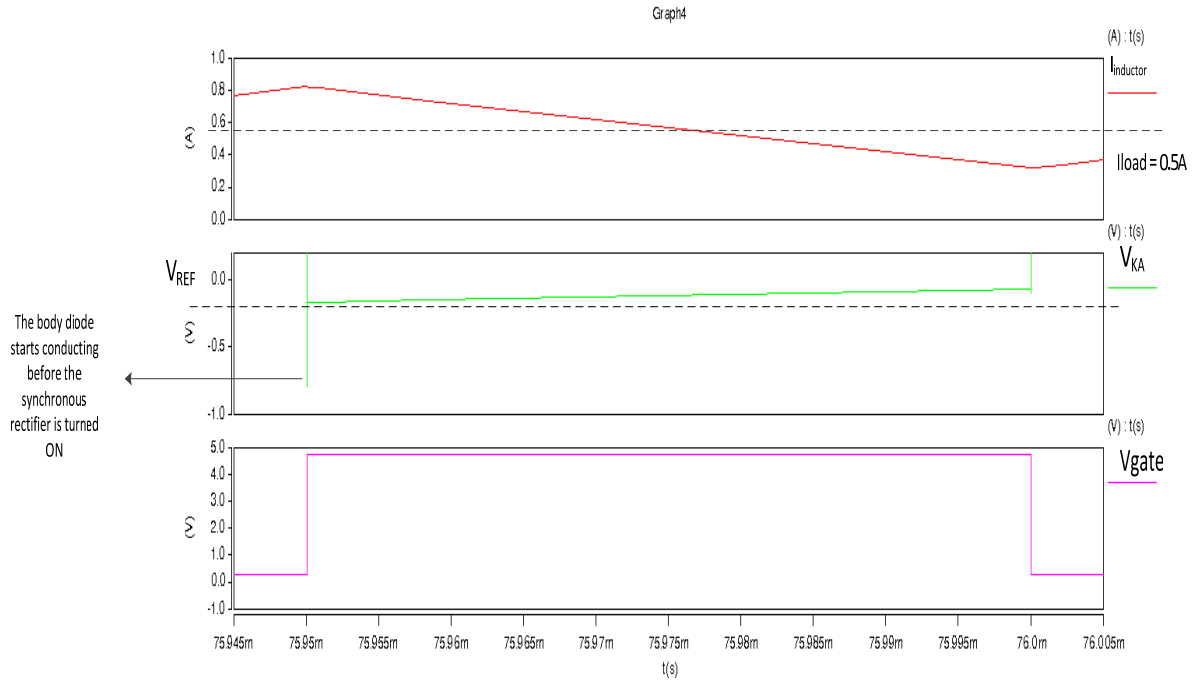

Figure 6-1
Waveforms of the SSSR when the Load current is Less than the Reference Current

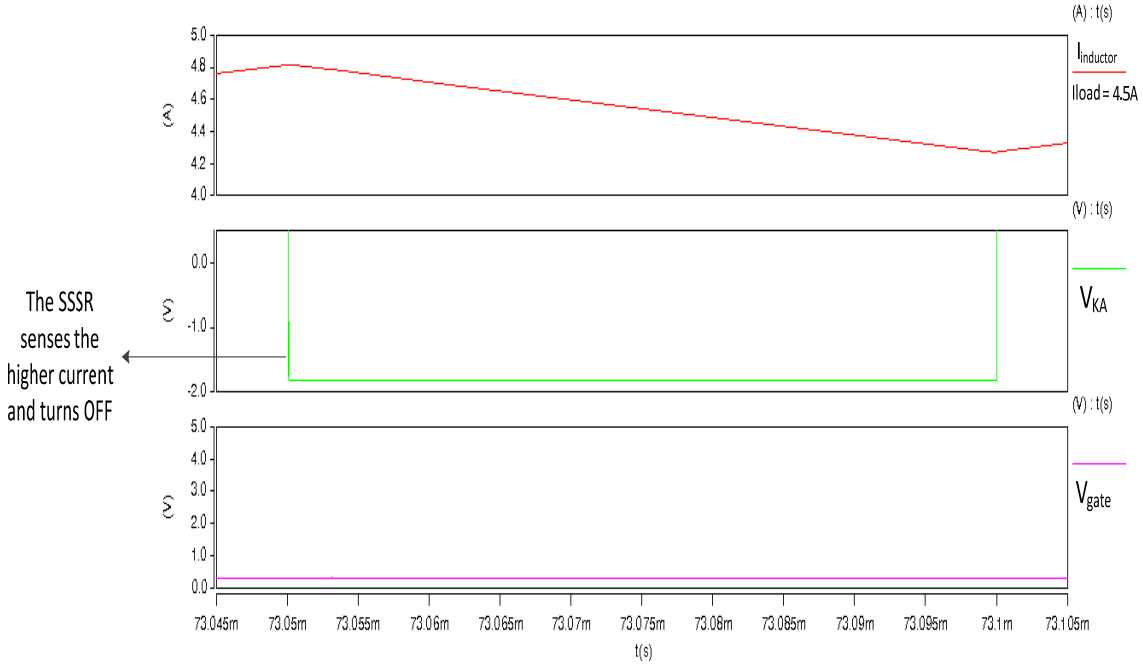

Figure 6-2
Waveforms of the SSSR when the Load current is Greater than the Reference Current

Also, as the load current is less than the reference current in this case, the synchronous switch remains ON for that entire switching cycle. However, if the load current is greater than the reference current, the current sense circuit turns OFF the synchronous MOSFET as shown in Figure 6-2.

The simulation results demonstrate that the circuit and principle of the SSSR are working.

Laboratory Testing and Experimental Results

The test bed was built using a prototyping board and the SSSR was implemented using discrete components. The results below validate the effectiveness of the SSSR in the laboratory.

The circuit parameters and the operating conditions of the SSSR and the test bed used in the laboratory are detailed below in Table 6-2.

Table 6-2
Circuit Parameters and Operating Conditions of the Experimental Setup

S. No	Circuit Parameter	Value
1	Input Voltage (Vin)	10V
2	Unregulated Output Voltage (Vout)	5V
3	Switching frequency	10kHz
4	V_f of freewheeling diode D1	0.6V
5	$R_{DS\ (ON)}$ of Synchronous MOSFET used in SSSR	50mΩ
6	Reference Current (I_{REF})	2A
7	Duty Cycle of Operation	0.5

In Figure 6-3, the circuit diagram of the buck converter (without the SSSR) with the voltage across the diode rectifier is shown.

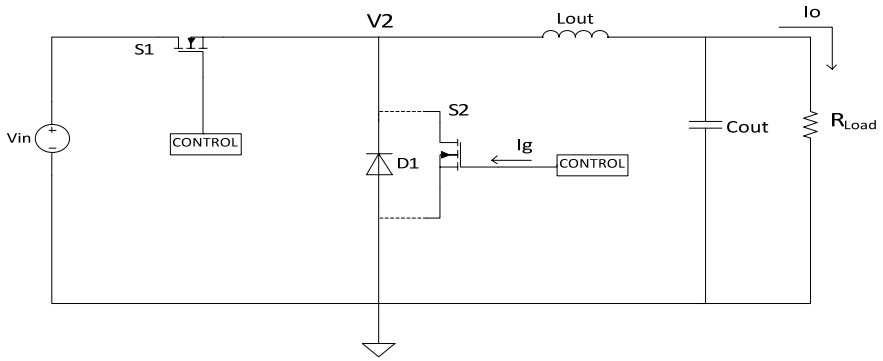

Figure 6-3
Test Bed

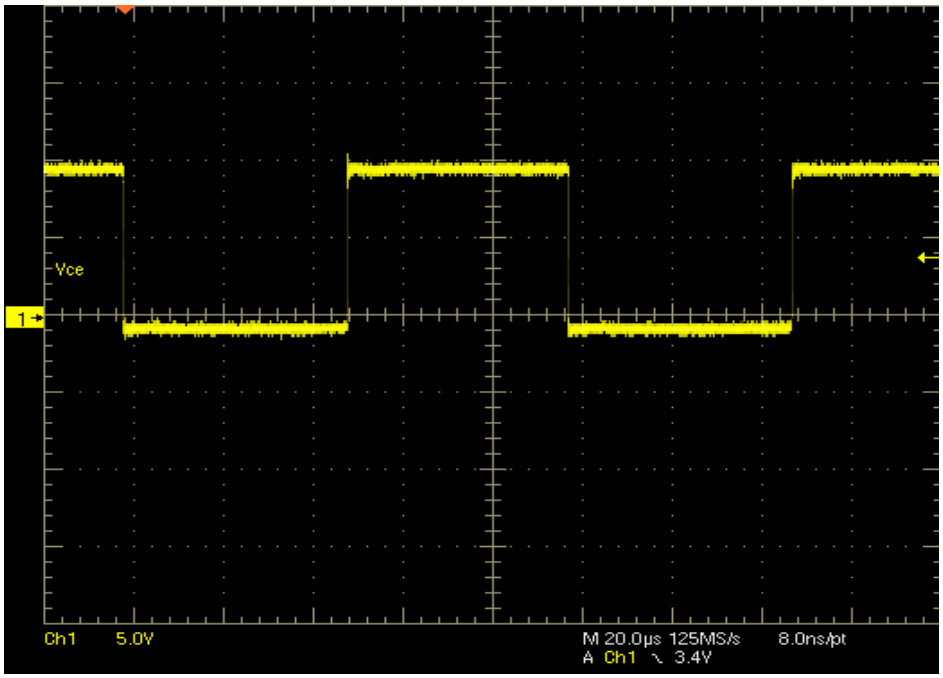

Figure 6-4
Voltage V2 across the Diode Rectifier

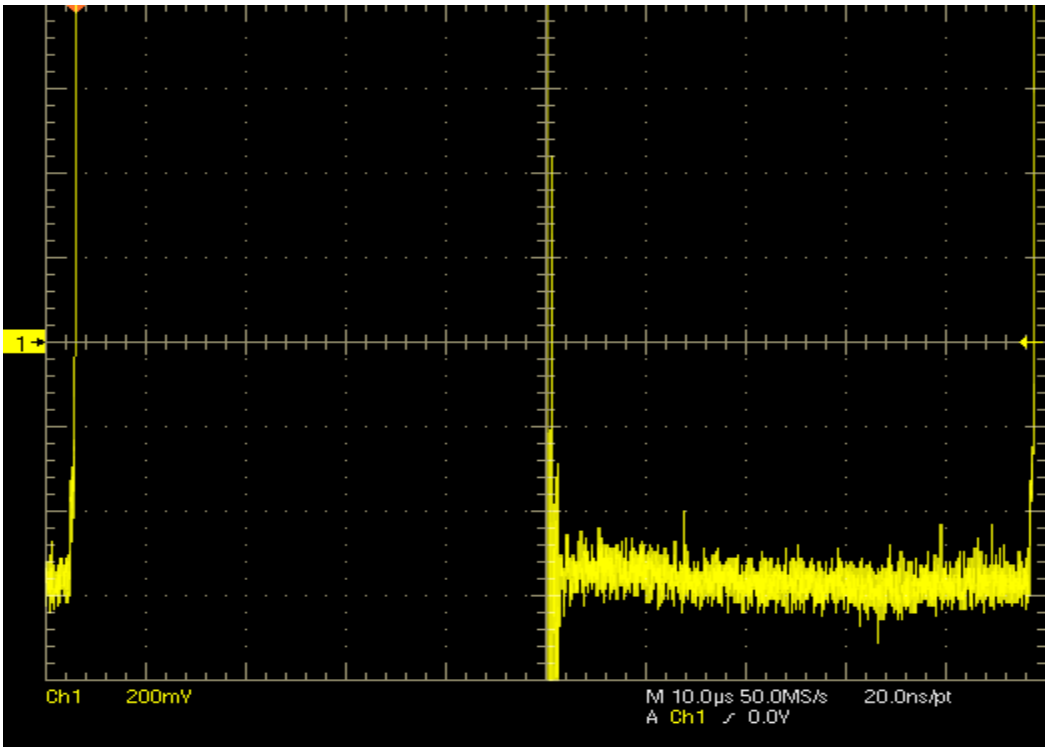

Figure 6-5
Voltage V2 across the Diode Rectifier when the Diode is Conducting

The Figure 6-5 above shows the voltage V2 across the diode, in a buck converter without the SSSR. There is a voltage drop of nearly -0.6V when the diode is conducting.

The SSSR is now implemented on the test bed by paralleling across the terminals of diode D1. During light load conditions, when the load current Io is less than the reference current I_{REF}, the switch S2 (of the SSSR) conducts and hence almost completely eliminates the loss due to the diode rectifier. This is shown in Figure 6-6 where under light loading conditions (I_{LOAD} (=1A) < I_{REF} (=2A)) switch S2 conducts and hence the voltage across the diode rectifier is $V_{KA} \approx 0$.

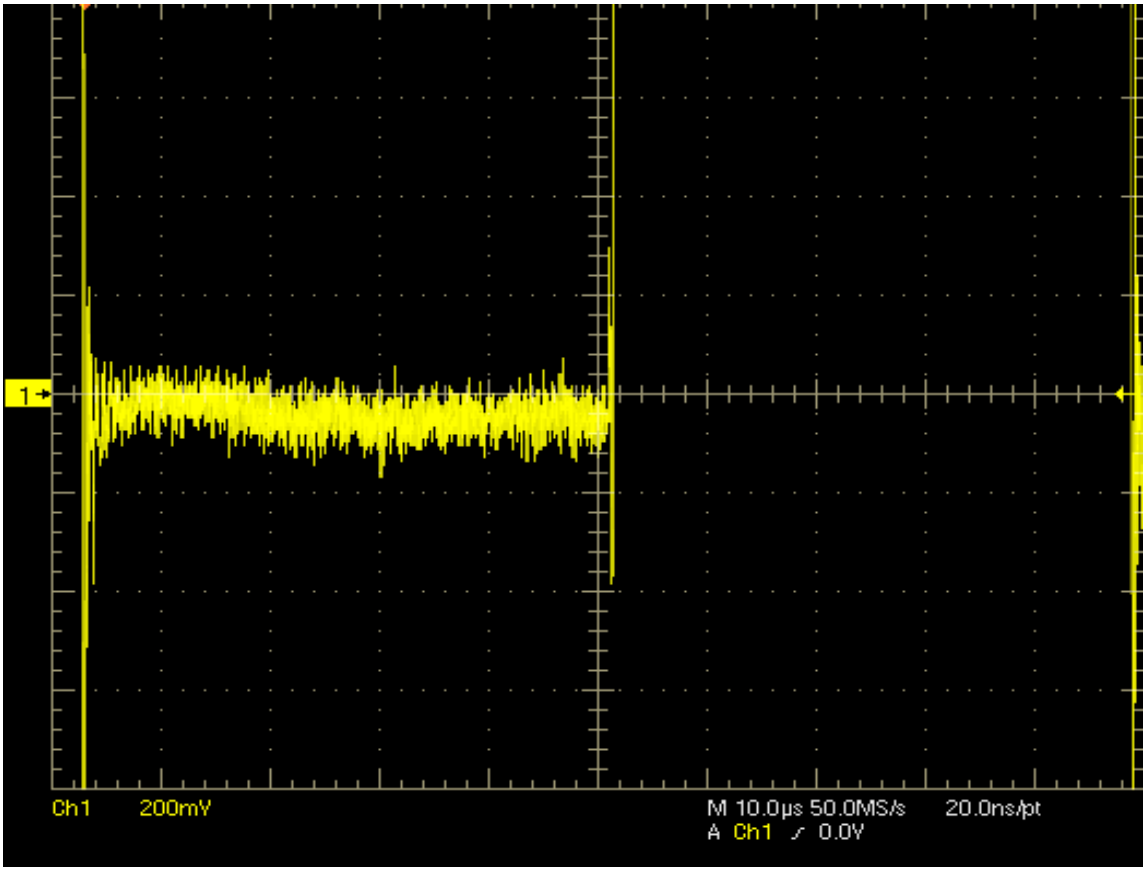

Figure 6-6
Voltage across the SSSR under Light Load Conditions

When the load current becomes greater than the reference current, the switch S2 turns OFF and allows the diode to conduct. This feature of the SSSR is illustrated in Figure 6-7 where the load current (2.5A) is greater than the reference current (2A) and switch S2 turns OFF and the diode conducts resulting in a voltage drop of $V_{KA} \approx -0.6V$ across the SSSR.

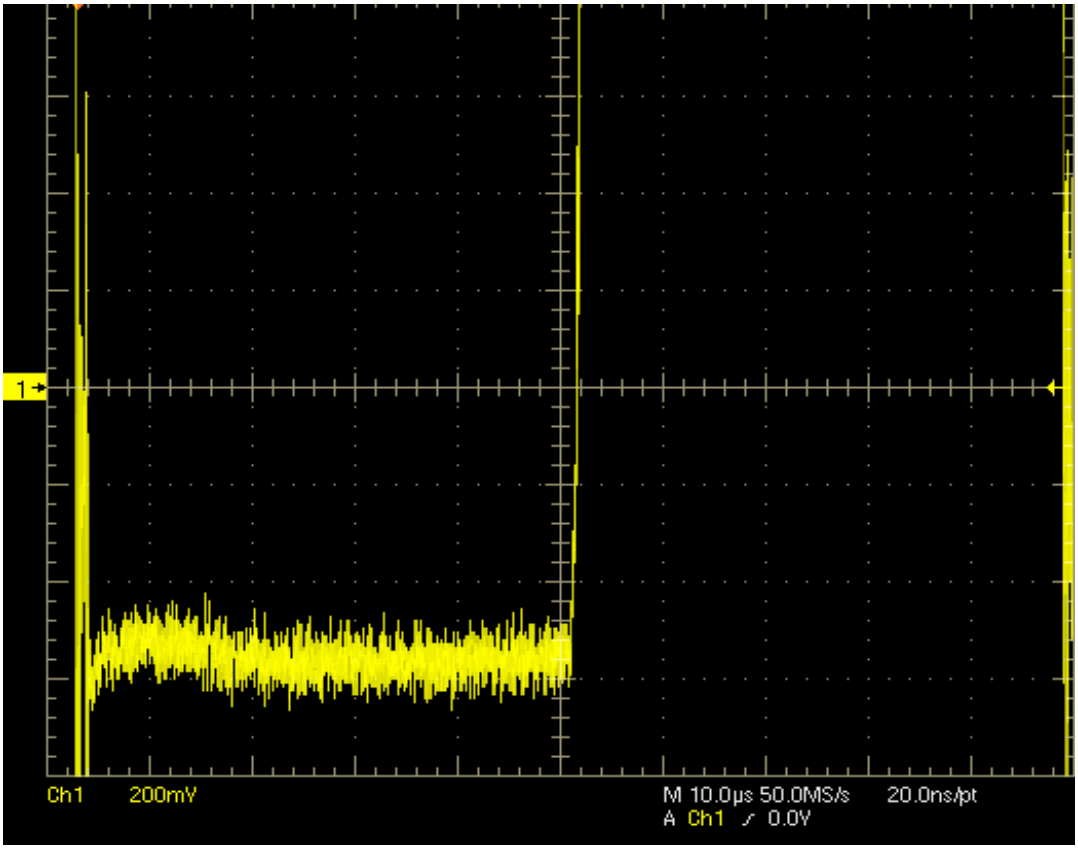

Figure 6-7
Voltage across the SSSR under Heavy Loading Conditions

The results obtained from Figures 6-6 and 6-7 clearly demonstrate the operation of the SSSR in the laboratory test bed.

Testing the SSSR on a Commercially Available Power Supply

The prototype of the SSSR was also tested on a commercially available dc-dc converter. The photographs of the SSSR proof of concept board and that of the SSSR being tested on a commercial power supply are shown in Figures 6-8 and 6-9.

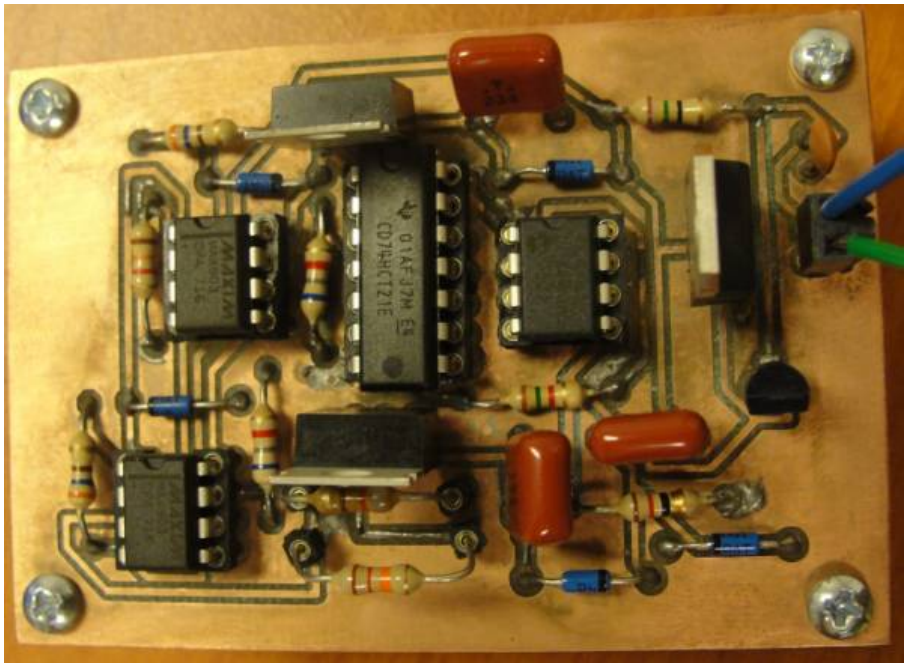

Figure 6-8
Proof of Concept Two Terminal SSSR Board

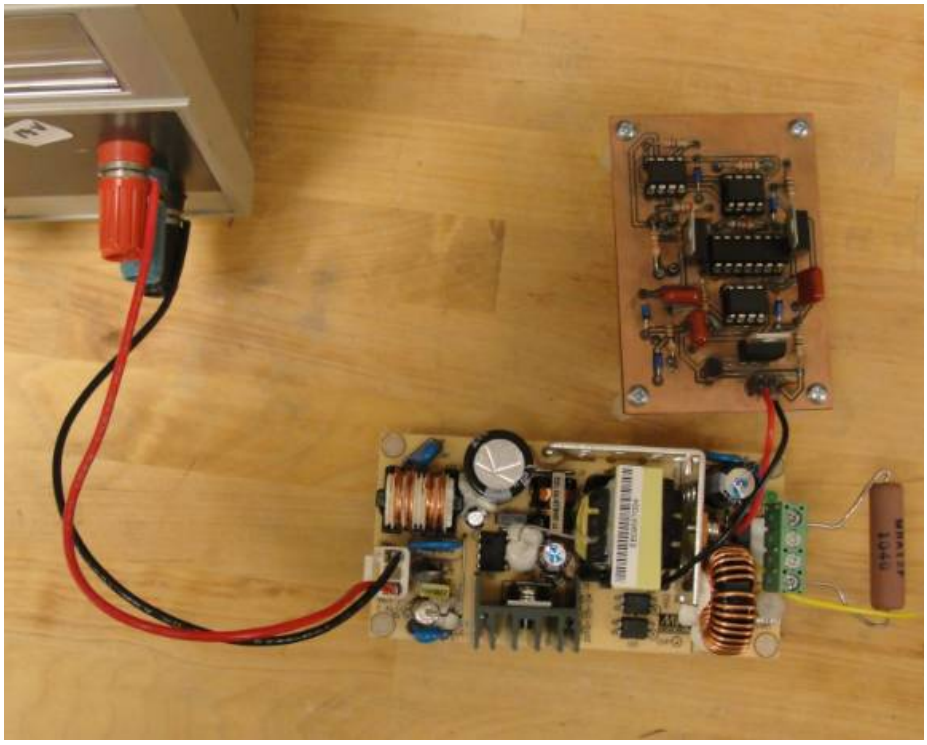

Figure 6-9
SSSR Tested on a Commercial Power Supply.

The circuit parameters and operating conditions of the commercial power supply are shown below in Table 6-3.

Table 6-3
Circuit Parameters and Operating Conditions of a Commercial Power Supply

S. No	Circuit Parameter	Value
1	Input Voltage (Vin)	10V
2	Regulated Output Voltage (Vout)	5V
3	Switching frequency	83kHz
4	V_f of freewheeling diode D1	0.45V
5	$R_{DS\ (ON)}$ of Synchronous MOSFET used in SSSR	50mΩ
6	Reference Current (I_{REF})	2A

The operation of the commercial DC-DC power supply with and without the SSSR are illustrated in Figures 6-10 and 6-11.

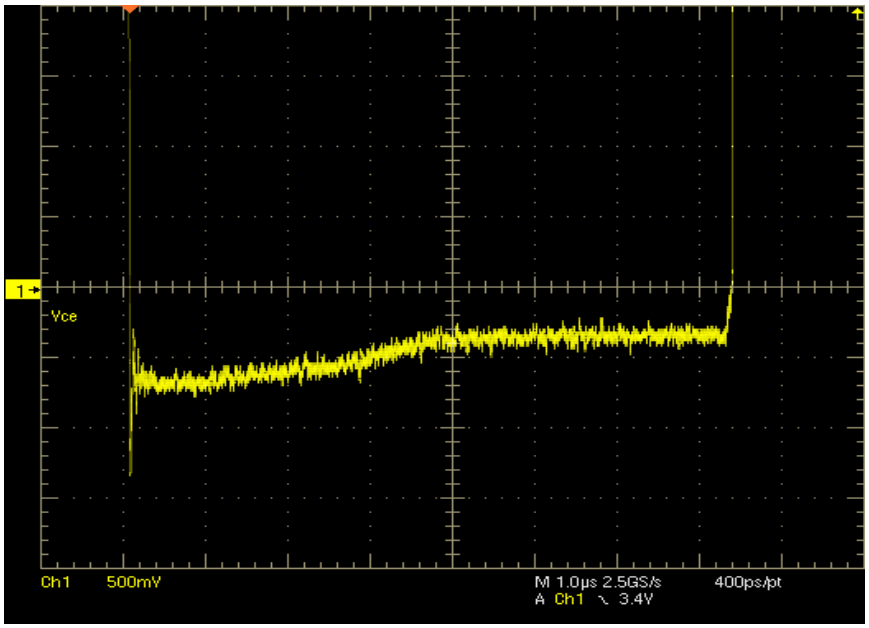

Figure 6-10
Voltage across the Diode Rectifier in the Commercial Supply without the SSSR

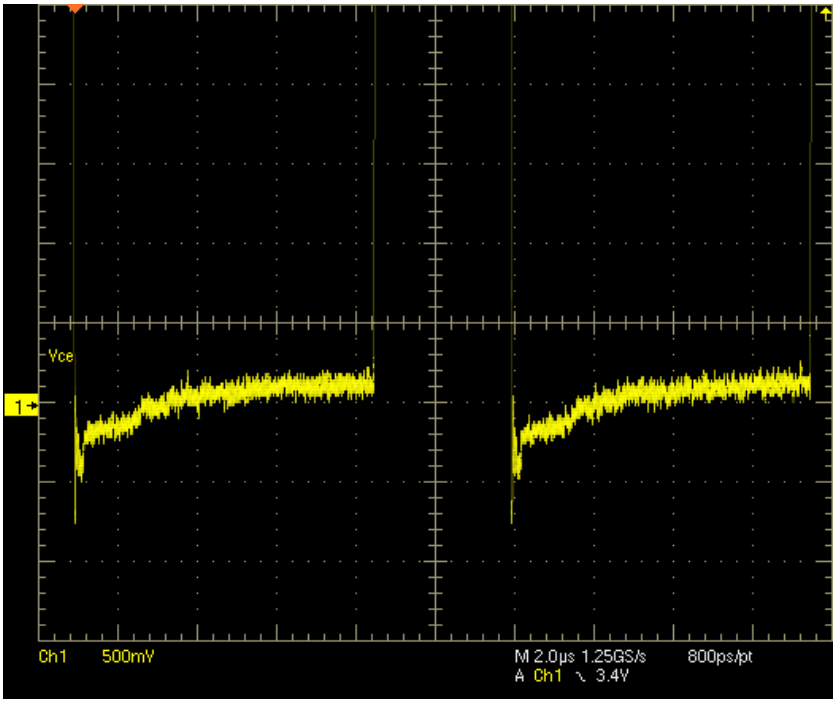

Figure 6-11
Voltage across the Diode Rectifier in a Commercial Power Supply Augmented with the SSSR under Light Load Conditions (I_{LOAD} = 1A)

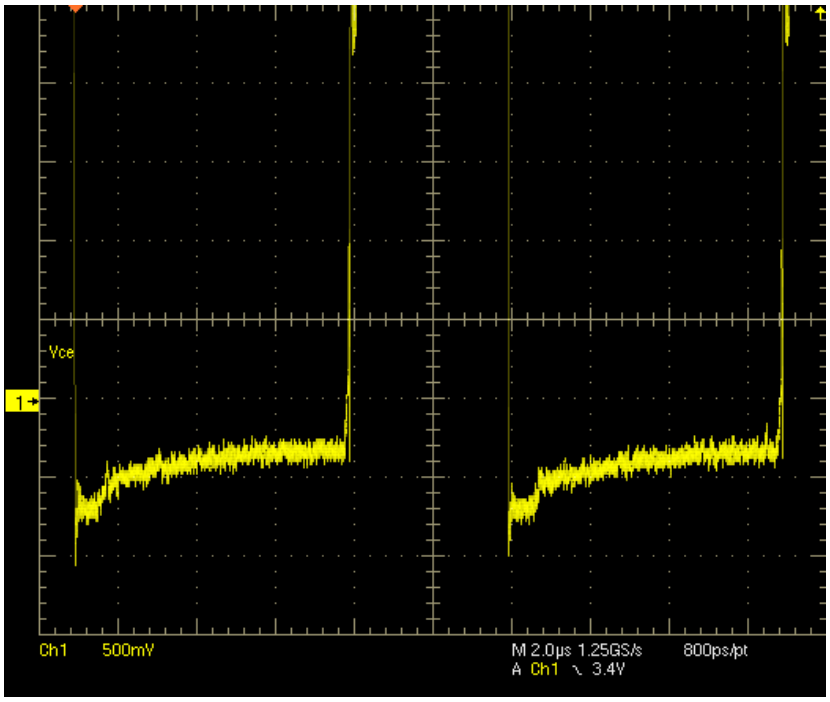

Figure 6-12
Voltage across the Diode Rectifier in a Commercial Power Supply Augmented with the SSSR under Heavy Load (I_{LOAD} = 5A)

Figures 6-10, 6-11 and 6-show that the SSSR works as proposed in eliminating the voltage drop across the diode rectifier terminals of the commercial DC-DC converter under light load conditions. The SSSR has been demonstrated in the laboratory as well as on a commercial product over a frequency range of 10 – 83 kHz.

Comparison of Losses in a System with and without the SSSR

The benefits of augmenting the output diode rectifier with the SSSR are determined by computing and comparing the losses across the diode rectifier with and without the SSSR. The losses are computed and compared for the buck converter test bed. The condition under which the test bed is operated is shown in Table 6-2. The system is operated under light load conditions (Load current = 2A).

Operation without SSSR

When the system is operated with the diode rectifier, the energy lost in the diode rectifier is in the form of conduction losses. The conduction loss across the diode is given by the formulae $V_f \times I_d \times D$, where V_f is the forward voltage drop across the diode, I_d is the current through the diode (in this case I_d = load current) and D is the duty cycle of conduction. The forward voltage drop across the diode as seen from Figure 6-5, is 0.6V. The conduction loss in the diode rectifier = $0.6 \times 2 \times 0.5 = 0.6$W.

Operation with SSSR

The diode rectifier of the test bed is augmented with the SSSR. The synchronous switch of the SSSR conducts since the load current (2A) is less than or equal to the reference current (2A) and thus prevents the diode across it from conducting.

The power that is lost in the SSSR can be classified into (a) conduction losses and (b) power that is required to control and drive the SSSR. The conduction losses in the SSSR is due to the conduction of the synchronous switch and is given by the formulae $I_{SW}^2 \times R_{DS\,(ON)} \times D$, where I_{SW} is the current through the synchronous switch (in this case, $I_{SW} = I_{LOAD}$) and $R_{DS\,(ON)}$ is the ON-state resistance of the MOSFET. So the conduction loss in the SSSR, $P_{cond} = 2^2 \times 0.05 \times 0.5 =$ 100mW. The power that is required to control and drive the SSSR was experimentally measured to be 42mW.

Comparison of Losses

Under the specified operating conditions, the total power lost in the diode rectifier was observed to be 600mW, whereas the total power lost in the SSSR was 142mW. From the results obtained, use of the SSSR reduced the energy lost in the diode rectifiers by 75%. A savings of 450mW has been achieved for this system under loading conditions with a reference current of 2A. The design of the SSSR can be modified to accommodate higher reference currents depending upon the type of intended application after performing a cost benefit analysis to determine whether

the power saving obtained offset the costs involved in upgrading to a higher current synchronous switch in the SSSR.

Impact Analysis of the SSSR

A preliminary return of investment analysis was performed taking into consideration that 450mW of continuous power usage was saved by using a SSSR under the light load condition. The amount of savings in energy for the test bed system by using the SSSR over a period of year = energy saved per hour × number of hours in a year = 450mWhr × 24 × 365 = 3.94kWhr. The cost of power is assumed to be 10 cents per kWhr. The cost at which the SSSR has to be priced to break even within periods of 1 to 5 years is shown in Figure 6-13.

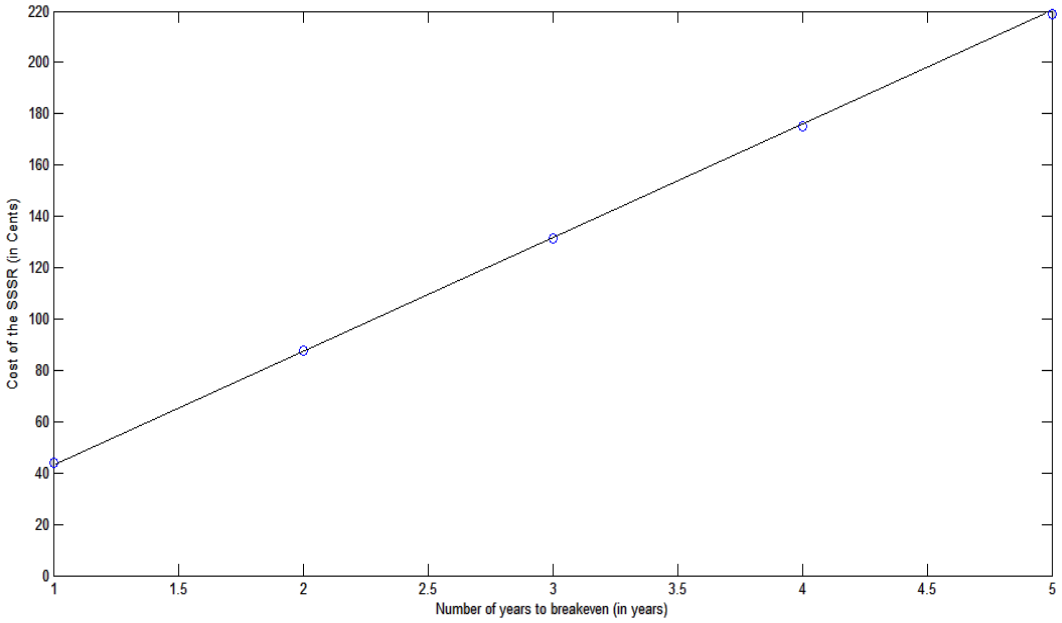

Figure 6-13
Number of years to breakeven with the cost of the SSSR

The system wide impact of using the SSSR is very large. If the power supply of every new printer sold in the U.S is augmented with this two terminal device, and if the conservative estimate of 450mW of continuous power savings obtained for the test bed is extended for the printers, then the amount of energy saved per year in printers in the U.S alone is 104GWhr. That is the equivalent of removing 209 coal plants (500MW each) from the grid for one hour, preventing one hundred thousand tons of CO_2 from reaching the atmosphere [10].

7
CONCLUSION

The main focus of this research was to develop a business model to show that redesigning of the existing power supplies towards a more energy efficient design is both technically feasible and economically viable. Computer and printer power supplies were identified as the main target applications. 3.68TWhr of energy is consumed by commercial grade multi functional printers and 1.96TWhr is consumed by household printers in the idle mode of operation in the US alone every year. In the personal computing arena, the amount of energy wasted in the home and office computers are approximately 34GWhr and 350GWhrs respectively. The important factor in the above projections is the fact that this energy is being consumed when they are not in active use, but under idle mode of operation. A market definitely exists for redesign of the power supplies since more than 1TWhr of energy is being wasted every year in the power supplies of electronic appliances in the US when they are not doing any amount of useful work.

A new device, called a self sustained synchronous rectifier (SSSR), has been devised to improve the efficiency of power supplies in the idle mode. The proposed device is cheap, self-controlled, self-powered, and has high impact in mitigating the losses in the power supply. The device consumes minimal space and can be easily augmented to any external power supply, regardless of the type of the converter used. A proof of concept board of the device is built using discrete components and its effectiveness proven on a commercial dc-dc power supply. Even under the most conservative estimates, the cost of the SSSR is offset by the direct savings in energy. The impact when this device is implemented on a system wide scale is found to be tremendous. The implementation of just this one device in all of the new printers being shipped in the US alone will save 104GWhr of energy in one year from being wasted in power supplies. That is equivalent of relieving the atmosphere from one hundred thousand tons of CO_2 burden. If the device is adopted on a nationwide scale, it could have a wide impact in reducing the carbon foot print of electronic devices on the U.S power grid.

Through this research it has been clearly shown that redesigning power supplies for higher efficiency at low cost is not only a possibility for better design and profits but an avenue for reducing the impact of the US grid on the atmosphere. It is hoped that this report will break the misconceptions that higher efficiency and lower cost don't go hand in hand and serve as a stepping stone for more innovation in the power supply design market.

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REFERENCES

References

1. IEEE 1515-2000, *IEEE Recommended Practice for Electronic Power Subsystems: Parameter Definitions, Test Conditions, and Test Methods.*
2. IEC 62301, Ed. 1.0, *Household Electric Appliances-Measurement of Standby Power.*
3. A. Mansoor, B. Fortenbery, B. Vairomohan, T. Geist, P.M. Ostendorp, C. Calwell, R. Rasmussen, D. McIlvoy, "Generalized test protocol for calculating the energy efficiency of internal ac-dc and dc-dc power supplies," www.efficientpowersupplies.epri.com (Accessed March 12,2011)
4. T. B. Visage, "Computer Usage in Daily Life", Proceedings of Chi-2009, pp. 575-874, 2009.
5. N. Horowitz, "Recommendations for tier 1 energy star computer specification", NRDC, Austin, Texas, 2005, www.energystar.gov (Accessed January 27, 2011)
6. "Worldwide Quarterly Hardcopy Peripherals Tracker," IDC Press Release, August 2010, www.idc.com/getdoc.jsp?containerId=prUS22476810 (Accessed February 6th 2011).
7. M. W. Smith, K. Owyang, "Improving the efficiency of low output voltage switch mode converters with synchronous rectification," Proceedings of POWERCON 7, p. H-4, 1980.
8. C. Y. Lim, Y. C. Liang, N. Balasubramanian, "A smart power synchronous rectifier by CMOS Process", IEEE Transactions on Power electronics, vol. 25, no. 9, 2010.
9. H. Pan, Y. C. Liang, R. Orunganti, "Design of smart power synchronous rectifier," IEEE Transactions on Power electronics, vol. 14, No. 2, 1999.
10. "Comparisons of life –cycle greenhouse gas emissions", www.wikipedia.org/wiki/Comparisons_of_life-cycle_greenhouse_gas_emissions (Accessed June 8, 2011).