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TASK REPORT 1: PROJECT E21-Z75

NASA NEW MILLENIUM PROJECT

A. Chatterjee attended the first New Millenium IPDT meeting 7/17-7/20 (1995). At this meeting, the Millenium Program and its organization structure were discussed and presented by NASA. Also, roadmapping tasks were assigned to all the IPDT team members and the overall scope of the program was discussed.

A. Chatterjee and David Schimmel attended the second New Millenium IPDT meeting from 8/13 -8/18 (1995). At this meeting, Georgia Tech’s involvement in the New Millenium was clearly defined. It was determined that Georgia Tech would play a key role in the test development effort for the microelectronics architecture.

As a result of the first two IPDT meetings, Georgia Tech undertook a literature search and review of existing test methods for 3-D and other multi-chip modules. This literature search resulted in the report included with this task report.
Multi Chip Module Testing Using Scan and BIST Methods

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Abstract

The combination of VLSI chips densely packaged into a MultiChip Module (MCM) offers tremendous benefits in performance, cost and space. Unfortunately, it also poses some major testing challenges that need to be resolved before it becomes a widely adopted solution. Among the most challenging problems are achieving acceptable MCM assembly yields and meeting product quality requirements. Both these problems can be significantly reduced by adopting adequate testing approaches which guarantee the quality of the incoming bare (unpackaged) dies prior to module assembly, ensure the integrity and performance of the assembled MCMs, and help isolating defective parts prior to the repair process.

This report presents Built-In-Self-Test and Boundary-Scan based testability approaches that are incorporated in the design phase of the MCM to resolve the above problems. The feasibility of the approaches are evaluated and an efficient solution is provided.
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1 Introduction

Over the last few years, increasing industry demand for high speed and smaller form factor electronic circuitry has led to the development of alternative packaging techniques. The Multi-Chip Module (MCM) technology is a key technology that meets the current miniaturization and performance demands [1, 2]. Advanced consumer products, such as personal digital assistants (PDA) and military equipment need MCMs primarily to achieve smaller size systems, whereas telecommunications equipment and supercomputers require MCMs to achieve operations with very high speeds.

MCMs today consist of single packages capable of supporting multiple bare-dies and/or discrete components [3]. It combines several dies with a custom designed substrate structure using different types of chip-to-substrate attachment techniques, such as wire bond, TAB or flip-chip [4, 5]. Multiple substrate technologies are currently in use to provide high density interconnect circuits for signals, power and ground [4, 5]. Three main examples of such substrate technologies are:

- MCM-C: Uses thick film technology to form conductive patterns and are constructed from ceramic (C) or glass ceramic materials.
- MCM-L: Uses laminate (L) structures and employs an advanced form of printed circuit board (PCB) technology to form predominantly copper conductors and vias.
- MCM-D: Uses deposition (D) of thin-film metals on unreinforced dielectric materials over a support structure of silicon or metal to form multi-layer signal conductors.

There is always a compromise between cost, performance and volume for choosing an MCM technology for a particular application. In general, MCM-L is used for mid-range performance and low cost needs (when wiring density requirements are
less than 200 cm/cm²). MCM-D leads to the highest performance, cost and wiring density (≥ 1000 cm/cm²) and MCM-C shows excellent power distribution and cost effectiveness if the wiring is greater than 200 and less than 1000 cm/cm². Figure 1 shows an MCM with dies flip-chip bonded to the ceramic substrate.

![Diagram of an MCM with labels: Die, Ceramic Layers, Signal, Gnd, Vcc, SIGNAL, VCC, GND.](image)

**Figure 1:** An example MCM.

Despite these benefits, MCMs have been slow to penetrate high volume markets such as computers, communications and consumer electronics due to the unsatisfiable quality of unpackaged chips or bare dies, the low yield of MCM assembly, high cost of MCM manufacturing, and complexity of test and rework. All the above factors ultimately lead to very high cost of MCMs. A significant (20-30 %) portion of the cost of an MCM is associated with the test, diagnosis and repair of the MCM [6]. Hence it is crucial that the test cost of MCMs is reduced.

Towards this end, this report discusses various test approaches, based on BIST and Boundary Scan (B-S), which enhance testability of MCMs at lower cost. These techniques are evaluated and the most effective solution provided. The report is organised as follows:
Section 2 discusses the MCM test problem. Section 3 and 4 introduces the BIST and Boundary Scan concepts, respectively, that are used for testing MCMs. Section 5 presents BIST and B-S based MCM test schemes. Evaluation of the techniques is provided in section 6. This is followed by summary of the report and some concluding remarks.

2 Multi-Chip Module Testing Problem

A Multi Chip Module test has a dual nature. It combines the complexities of chip and printed circuit board (PCB) testing [7, 8, 9]. An MCM manufacturer views his MCM as a board, and hence requires adequate diagnosis to replace its bad chips or repair its interconnects. This is a characteristic of board testing. Also, since an MCM is destined to be mounted on a board, its user requires a defect rate as low as the other chips on the board. Therefore, an MCM and its chips need to be tested as completely as the other chips. Thus MCM test covers the test requirements of complex chips and the diagnostic requirements of boards.

The MCM process flow can be divided into four non-overlapping processes, as shown in Figure 2. They are: (1) process of fabricating the wafer, (2) the production of individual bare dies, (3) the fabrication of substrates, and (4) the assembly of bare-dies and substrates to compose MCMs. Testing takes place during each of the these four processes and are shown by shaded boxes. They are also divided into four set of activities that correspond to the MCM production processes. They are: wafer test, bare die test, substrate test and assembled module test and rework. These steps constitute the MCM test and diagnosis problem.

Traditionally, bed-of-nails testers are used to test printed wiring boards. However, because of the high chip density and small interconnection line dimensions of emerging MCMs this approach cannot access the internal lines. Even if this could, this type of tester is extremely costly for most MCMs. In addition, external testers
are rapidly approaching another physical limitation: the circuits-under-test are faster than the delay along the tester probe circuitry [10, 11]. The test problem at each of the four stages of production of MCMs is described in the following subsections.

2.1 Wafer and bare die test problem

The wafer and die yield plays an important role in the overall MCM yield. The conventional test at the wafer level is limited to a simple parametric test and low speed functional test to verify if the die is alive. The full test is performed only after the die is packaged [12]. The bare die yield effects the yield of the MCM significantly.
For example, a 50-die MCM with a 95% yield of the incoming die results in a 7.7% yield of the assembled MCM before testing. This means that more than 90% of the assembled MCMs must be diagnosed and repaired, a costly and time-consuming task [6]. The incoming yield of bare die must be pushed to nearly 100% to produce a module yield high enough to have a cost effective MCM process [4, 5]. Thus the following three test sequences must be performed on the die before they are integrated with the substrate: (1) Input/Output parametric test, (2) Complete functional at-speed test, and (3) Burn-in. This provides the Known Good Die (KGD).

The input/output parametric test verifies that the finished die meets input/output voltage and leakage specifications. A standard procedure using wafer probes is used. The functional at-speed test of the die is needed to detect delay type faults which are not manifested during the conventional low-speed wafer test. The existing wafer probes cannot be used for at-speed testing as they have speed limitations and are very expensive [13]. Burn-in is required for chips to identify if they have latent failures. This is usually done on packaged dies. Several experimental approaches based on temporary die packaging have been reported [14, 15]. But they are very expensive. Thus, wafer and die testing for MCMs face three major difficulties: the first is the need of known good die quality with very high yield, the second is the speed limitation of existing wafer probes, hence the problem with performance testing; and the third is the problem of burn-in associated with the required reliability testing.

2.2 Substrate test problem

The substrate test is as important as the die test for MCM yield. The usual substrate testing failure types include opens, shorts and bridging faults. Substrate test is done by flying probes measuring resistance or capacitance of the nets [4, 5]. The probes may damage the substrate and are slow for substrates with a large number of nodes. Contactless probing schemes such as electron beam test is much faster than mechanical probing but is very expensive [16]. However, results show that the existing
mechanical probing techniques are effective for substrate test [16].

2.3 MCM assembly test problem

The MCM assembly test requires an interconnect test, a full functional test and a performance test [17, 18]. Due to MCM bare die handling and bonding processes, there is a chance of damage to the die and substrate. In addition there are thermal stresses which are present when the module is powered. This can also result in damage to the die and the substrate. Hence, we need to run a thorough test again after mounting the die on the substrate. The full functional test of the die on the MCM assures that all the die are functionally correct. On the other hand, the interconnect test assures that all the die are properly connected to the substrate. But these two tests do not verify that all the die on a MCM substrate properly communicate with each other. An overall MCM performance test detects propagation delays (path delays) including die delays, interconnection delays and substrate routing delays. Other factors that reduce the performance of an MCM, ie. timing skews between die, ground bounces, variations in loading on the die outputs are also identified by the performance test for the entire MCM [5].

Due to the very limited accessibility to the MCM circuitries, it is impossible to test the interconnects and the die with conventional probe techniques. The speed limitation of automatic test equipments (ATEs) limits the performance test of the MCM. An MCM performance test requires a tester with the capability of high speed test vector application over very high pin counts. If at all possible, this can only be realized by very expensive ATEs. These are mainly IC testers. The IC testers do not provide diagnostic information for bad component isolation as ICs do not need repair information. Module level probing techniques can provide such diagnostic information, but due to the density of today's MCMs probing turns to be almost impossible. Thus a new approach is needed for interconnect test, functional at-speed test and performance test of the assembled MCM.
Finally after the faults in the MCM are detected, the MCM may enter a repair cycle. The number of repair cycles depends on the MCM technology used and the cost effectiveness of the repair. This problem also needs to be addressed along with the test of the MCM.

Thus it is evident that conventional probe techniques are not satisfactory for MCM testing. An obvious approach to alleviating the need of sophisticated testers at all levels of integration is to incorporate the tester into the circuit under test itself; hence the notion of Design For Testability (DFT). Thus, to produce high quality and cost effective MCMs, we must include test and fault diagnosis as critical requirements early in the design cycle. Treating test as an afterthought in this process may result in high costs and be impossible to accommodate later. The design for testability approach eliminates the need for expensive testers and provides a mechanism for accessing and exercising internal design circuitry.

The two most common design for testability techniques applicable to MCMs are Boundary Scan (B-S) and Built-In-Self-Test (BIST). In the following sections, the two techniques are briefly described.

3 Boundary Scan Overview

Boundary Scan (B-S) is a general testability strategy that allows controllability and observability of the I/O pins of an IC/die embedded in a system. The IEEE/ANSI standard 1149.1-1990 [19] is an industry wide accepted set of guidelines to implement boundary scan. The architecture of Boundary Scan associates a memory cell with each input and output of a chip. These memory cells are connected serially to form a shift register. The chip also contains a four-port standard connection, the Test Access Port (TAP), which provides access to this shift register and controls the various chip test modes.

Figure 3 shows a general form of a chip which supports the B-S standard.
The application logic represents the normal chip design prior to the inclusion of logic required to support the standard. This circuitry may include DFT or BIST hardware. If so, the scan paths are connected via the test bus circuitry to the chip's scan-in and scan-out ports. This is shown in the figure by the connection from TDI to $S_{in}$ and $S_{out}$ to TDO. The normal I/O terminals of the application logic are connected through boundary-scan cells to the chip's I/O pads.

The test bus circuitry consists of the boundary scan registers, a 1-bit bypass register, an instruction register, several miscellaneous registers and the TAP. The TAP consists of four lines, namely a test clock (TCK), a test mode select (TMS), the test data in (TDI), and the test data out (TDO).

Test instructions and data are sent over the TDI line. Test results and status information are sent from the chip over the TDO line. The state of the test circuitry in the chip is defined by the state transitions on the TMS line which are decoded by
the TAP controller.

The test bus and the control logic operates as follows:

1. An instruction is sent serially over the TDI line into the instruction register.

2. The selected test circuitry is configured to respond to the instruction. This may involve sending more data over the TDI line into the register selected by the instruction.

3. The test instruction is executed. Test results are shifted out of the selected registers and transmitted over the TDO line to the bus master. New data is shifted into the registers while results are shifted out over the TDO line.

Figure 4: Chips on a board connected in a B-S chain.

The boundary scan standard is used predominantly for testing printed circuit boards. The B-S cells of all the chips on the board are connected into one single scan path, where the TDO of one chip is tied to the TDI of another chip, except for the initial TDI and last TDO ports which are tied to the distinct terminals of the board (Figure 4). Using this configuration various tests can be carried out, including (1)
interconnect test, (2) snapshot observation of the normal system data, and (3) testing of each chip. To implement these tests, three test modes exist, namely external test, sample test, and internal test. The test modes are subsequently explained.

**External test mode**

This mode is used to test the interconnect between chips for shorts, opens and stuck-at-faults. The test data is shifted into the boundary scan registers of all chips and the data is driven out of output pads of the chips. This data is captured by B-S input cells in the chips. The captured data is now shifted out to check if the correct response was received. During this mode the application logic is cut off from the external logic by the boundary scan register. This mode is enabled by the EXTEST instruction.

**Sample test mode**

In this mode the boundary scan cells in the signal path between a chip I/O pins and the application logic do not interfere with the operation of the board logic. The I/O data associated with the chip is sampled (captured) into the boundary scan registers and shifted out while the board remains in normal operation. This mode is selected by the SAMPLE instruction.

**Internal Test mode**

In this configuration, the inputs to the application logic are driven by the input boundary scan cells, and the response is captured in the output boundary scan cells. If the chip has BIST, the BIST operation can be activated to test the chip. This mode is used for at-speed test of the chips and is enabled by selecting the INTEST or RUNBIST instruction.

Further details of the test modes are described in [19].
4 Built-In-Self-Test Overview

Built-in-self-test (BIST) is a design for testability technique that allows a circuit to test itself [20, 21]. Testing (test vector generation and test response analysis) is accomplished through built-in hardware features. BIST architecture consists of several key elements, namely, (a) test pattern generators (TPGs), (b) Output Response analyzers (ORAs), (c) circuit under test (CUT), (d) Distribution system (DIST) for transmitting data from TPGs to CUTs and from CUTs to ORAs, and (e) BIST controller for controlling the BIST circuitry and CUT during self-test [22]. The TPG produces input test sequences (stimuli) for the CUTs. The ORA compacts output response sequences and generates the signature. Comparing the signature with the previously calculated signature of the fault-free circuit, the comparator produces a pass/fail signal [22, 23]. The general form of the BIST structure is depicted in Figure 5.

![Figure 5: General form of BIST architecture.](image)

Various levels of chip level BIST have been used during the last decade [21, 23, 24, 25]. Similar to any additional added features BIST causes additional on-chip
real estate. However, the benefits of using BIST seem to dominate. Typically BIST schemes detect single stuck-at faults in the functional circuitry. Most schemes can detect some other faults as well. The ideal BIST scheme would be a generic one that would be applicable to any block in the chip. However, such schemes are not practical due to the fact that digital chips today consist of blocks of different types of structures, device densities, and fault models associated with each. For example, embedded memory blocks like RAMs or ROMs consist of structures which are much denser than random logic blocks and have distinct sets of faults in addition to single stuck-at-faults. Hence specific BIST schemes are needed to test each type of block in order to achieve very high fault coverages.

Several schemes to test random logic blocks based on pseudo-random and exhaustive schemes are presented in [25]. Typically, single stuck fault coverages of more than 98% are achieved using these techniques. To test regular structures such as ROMs, RAMs, PLAs, deterministic test approach is used. Examples of regular structure BIST schemes with 99+% fault coverages can be found in [24] for RAMs and [26] for ROMs.

One of the major advantages of BIST, in addition to obtaining very high fault coverages, is its ability to run at system speed. This is ideal for performance tests of the chips. In the following section, several MCM test approaches employing BIST and B-S techniques are presented.

5 MCM Test Schemes

Four elegant MCM test techniques are described in the following subsections. These schemes employ BIST and B-S for test and diagnosis of MCMs.
5.1 A Structured Testability Approach

This technique has been proposed in [17]. The testability approach is based on implementing die level BIST and module level Boundary Scan in the MCM design (Figure 6). The benefits of implementing BIST and B-S in bare-dies is discussed at various stages of MCM testing.

![Diagram showing BIST and B-S features in an MCM](image)

Figure 6: BIST and B-S features in an MCM.

5.1.1 Bare Dies Test Procedure

The test applied on bare-dies consists of parametric test, functional at-speed test and reliability test. The parametric test already exists in conventional wafer test and probes are used to accomplish it. The functional at-speed test becomes possible due to the incorporation of BIST in the design of the dies. The two main problems of wafer testing, namely obtaining very high fault coverage functional test, and running
it at system speed for performance test are greatly simplified due to use of BIST. The execution of this operation is autonomous. It only needs the application of Boundary Scan standard's RUNBIST instruction through the B-S TAP to start the BIST execution, and upon completion, the BIST response needs to be scanned out for evaluation. This is also done through the B-S TAP. During the burn-in test, the BIST can be kept active on the die under test. This allows continuous monitoring of the response status for additional in-process information.

5.1.2 Assembled MCM Test Procedure

The following sequence of tests are performed after the MCM is assembled.

1. **Integrity and identity test:** The boundary scan circuitry is verified before it is used to test the MCM. The B-S standard provides a certain method to perform this test, yielding relevant diagnostic information regarding the location of the failure if any [19]. Subsequently, a test is performed to check the identity of each die. The B-S standard allows permanent storage of die level ID codes. Each die will have its ID code, which will be read through the B-S TAP and be compared with a reference value. This test detects if a wrong die is mounted on the substrate, or a die is not oriented properly.

2. **Interconnect test:** The existence of B-S chain in the module, consisting of the B-S registers of each die and the connections between these registers through the substrate creates a virtual electronic bed-of-nails built into the module. B-S latches provide the stimulus and can sense across all interconnects. This permits testing the interconnect for opens and shorts. The interconnect test needs the use of detection algorithms with high fault coverages. Several algorithms have been developed to automate the generation of test vectors for interconnect test [32, 33]. The B-S standard instruction EXTEST enables this test.

3. **Functional at-speed test:** This operation is similar to the bare-die BIST test. The test vectors are generated in the dies autonomously, due to BIST. Hence
there is no need to access each pin in order to run the functional test. Further, BIST is a built in capability and hence is transparent to transfers between MCM manufacturers. This operation provides diagnostic information also. The comparison of the BIST responses identifies which die has failed.

4. MCM performance test: The BIST implemented in all the dies is used to perform an at-speed BIST on the entire MCM considering it as a single module [29]. Contrary to die level BIST (D-BIST), the pseudo-random test pattern generator of MCM level BIST (M-BIST) uses multiple TPGs, distributed over all dies. Also the ORA is distributed over multiple dies. The outputs of TPGs are connected to the primary inputs of an MCM under test. Hence the inputs of each die are categorized as external inputs (EI) i.e. the primary inputs of an MCM, and internal inputs (II) i.e. the inputs connected to other dies in an MCM. Only the EIs of a given die will be connected to the M-BIST TPG. Similarly, the outputs of each die are categorized as external outputs (EO) i.e. the primary outputs of an MCM, and internal outputs (IO) i.e. the outputs feeding other dies in an MCM. For output data compaction, all EOs of a die need to be connected to the M-BIST ORA. M-BIST is executed in parallel with free running IIs and IOs on all dies. To obtain diagnostic information and locate failed components, the signatures are captured by B-S registers and scanned out for analysis.

Thus in the above scheme, the B-S cells of IIs and IOs must be maintained in a safe state so that there is no internal damage. Two approaches are proposed in [30] to solve this problem. The first is a software approach that disguises the B-S cells of IIs and IOs. The second is implementing the die level B-S register in a way so that these cells are either eliminated from the B-S path or are transformed to redundant cells.

Thus the structured testability strategy impacts the test process at the wafer level, die level, module level and beyond. This strategy needs to be considered during the early product design stages, and helps in meeting the MCM quality requirements.
This strategy is universal since it is independent of MCM’s functionality, adopted technology and complexity.

### 5.2 An Incremental ‘Smart Substrate’ Testability Approach

This technique has been proposed in [27]. The testability approach is based on enabling incremental test of all system components by designing and implementing the test structures into the silicon substrate itself.

The traditional MCMs use passive substrates that enable efficient interconnections and low cost system integration solutions. This results in the system yield problem as the bare dies are not fully tested when they are assembled into the MCM system. Further, the physical inaccessibility of the I/O pins of the component dies after mounting on the substrate reduces observability and controllability. Hence the notion of an active substrate, that incorporates power hungry system elements and extensive design for testability structures into the substrate, built using MOS or bipolar transistors.

Traditional MCM test approaches assume that one can obtain acceptable system yield by using known good die. The solution proposed here is based on the opposite assumption- that MCM system components are incompletely tested, and therefore the system integration strategy should accommodate defective dies without affecting system-level yield. This strategy uses the active substrate to perform testing and assembly in a ‘smart’ way- detecting defective dies instead of demanding defect-free dies. Performing testing this way also makes it possible to detect failures that occur after wafer testing, such as assembly failures. Thus, the smart substrate integration strategy uses the testing logic on the substrate to perform incremental assembly and testing - that is, system and component testing after each new component is connected to the already operational portion of the assembled system.

This is achieved by applying Boundary Scan and BIST in the active substrate. The testing logic is designed to provide the following:
• Separate direct access to each die in the system.

• Boundary Scan testability of component dies, substrate interconnections and glue logic.

• Boundary scan testability of the entire system as a single circuit (potentially facilitating subsequent board testing).

• Selective control of which sections of the system are powered during testing.

Figure 7: Smart Substrate B-S test features.

These features enable individual testing of each component within a fully or partially assembled system. Figure 7 shows the full circuit block diagram of an MCM that includes two dies. Three separate boundary scan chains, each dedicated to one system component, provide boundary scan testing. (In a larger system, access to these chains would be coordinated through a central test controller.) The boundary scan cells implemented in this system support the IEEE standard 1149.1 test functions INTEST, EXTEST and SAMPLE. Finally, the smart logic allows selective connection
of power to the chips in the system. This feature facilitates incremental testing during system assembly and allows selective $I_{DDQ}$ testing of system components.

The incremental tests of the MCM smart substrate system is proposed to be performed in the following three steps:

1. **Testing of unpopulated substrate**: This step is accomplished by testing that the boundary scan chain functions as a shift register and then testing the substrate glue logic using boundary scan in EXTEST mode.

2. **Testing of partially populated substrate**: This step tests subsequently attached dies for I/O continuity, functionality, and communication with previously attached system components. The boundary scan circuitry or the direct access circuitry is used for this purpose. The dies are testing using the boundary scan INTEST mode. Further, partial system test is performed by using the boundary scan logic to Sample signal values in the system (uses SAMPLE test mode).

3. **Testing of fully populated MCM**: A final system test is executed as a standard system test supported by the boundary scan. Thus this consists of individual direct access test of each chip in the system, boundary scan test of each chip in the assembled system (INTEST mode), boundary scan test of glue logic in the assembled system (EXTEST mode), at-speed test using boundary scan SAMPLE operation.

By testing in this manner— that is, by combining test and assembly operations—one can detect faulty components immediately after assembly. Consequently, diagnosis and rework are simple and more effective for maximizing system-level yield. Further enhancement to the above testing methods could be provided by application of BIST directly into the system substrate to test the individual dies. Increased control could be provided over chaining of different subsets of boundary scan cells. Thus in a smart substrate MCM system, one can provide all the testing options without redesigning the system’s components. Thus, the system enables a virtual BIST and BS technique by means of ‘non-BISTed and non-BSed’ components. A cost effectiveness study of the test structures placed on the MCM substrates against the BS and BIST
structures placed on the dies have been presented in [34, 35]. The results show that the use of active substrates to implement incremental testing tends to have better cost results and higher yields.

5.3 A Test Controller Inclusion Approach

This strategy involves inclusion of a test controller die that has testability features incorporated in it for enhanced testing of the MCM. Not all the dies on the MCM have IEEE 1149.1 capability. Hence, to facilitate interconnect and functional test of these dies several techniques have been proposed in [28, 30, 36].

Interconnections between dies on the MCM can be classified into one of the two categories: connections between two pins on boundary scan dies and connections where at least one of the dies has no boundary scan capability. In the former case, the interconnections may be verified using techniques specified in [32, 33]. The latter case, however, becomes more complicated and therefore the test technique chosen will depend upon the level of visibility present at the interconnecting points. Two categories of interconnections are introduced in this case.

1. A die that does not contain B-S capability has all of its input pins accessible either through boundary register cells in other dies or directly via the module I/O pins.

2. A die that does not contain B-S capability has at least one input or output that is inaccessible through a boundary register cell in other dies or the module I/O pin.

Category 1 dies may be verified by simply creating a digital test that uses the boundary-register access for applying and receiving the test vectors. If a test is created such that all of the die pins are toggled, then the interconnections are verified. An added benefit is that this type of test will also verify, to some degree, the functionality of the die being investigated.
Category 2 dies present a more difficult problem. There is no access to the interconnect node, so the die test must be propagated through intervening dies to the inputs and outputs being investigated. Of the various techniques investigated, the best is the use of a logic simulator to generate tests for the entire cluster of dies through which signals are to be propagated. The pattern set and logic simulation will provide a diagnostic capability via the fault dictionary. Additionally, the I/O and pin fault information will reveal the quality of the interconnect test. It will be necessary to get to 100% coverage on these fault types in order to verify all interconnections in this category. The category 1 and 2 dies are shown in Figure 8.

![Figure 8: Non B-S category dies.](image)

If the complexity of the circuitry of the category 2 is large it is not possible to obtain the needed fault coverage to verify all the interconnects. This problem can be eased by providing some sort of access to these dies through a test controller die (TCD) designed to provide additional visibility and control over non-boundary scan dies. The TCD itself is compatible with the IEEE 1149.1 standard. The strategy is
outlined as follows: If a special 1149.1 compatible silicon die (TCD) is manufactured such that it is capable of capturing data from its inputs, then those inputs could be connected to the category 2 internal nodes to provide the needed visibility. Hence, a simple input-only boundary register built into the TCD is used for this purpose. A faster diagnosis might be provided if CRC accumulation is allowed rather than the bit-wise accumulation of data from the input cells of the boundary register. The test controller die includes a TAP controller and a boundary scan register. Some of the boundary cells are connected to CRC accumulators. This is depicted in Figure 9.

![Test Controller Die (TCD) incorporated MCM](image)

Figure 9: Test Controller Die (TCD) incorporated MCM.

Further if it is needed to provide data to the inputs pins of the non B-S dies, then the TCD could have an LFSR built into it to generate test vectors. The TCD could also include a single bit bypass register and a single IDCODE register incorporated in it so that the MCM is compatible with IEEE 1149.1 B-S standard during board level test.

The main advantage of a separate die for test controller is that the MCM die designers do not have to make any changes to their die designs. Further, incorporation
of the TCD provides a higher fault coverage and improves observability and system level testability. This improves field diagnostics and repair cycle and reduces test equipment costs. However, there are penalties which must be paid for this, the worst of which is the module propagation delays. An additional capacitive load is placed on category 2 interconnecting nodes due to the additional trace and input capacitance of the testability circuitry. Further, the TCD increases the MCM real estate requirements. However, the advantages clearly offset the drawbacks and the feasibility is evaluated in [36].

5.4 BIST based Self Testing Approach

The BIST scheme for MCMs was first proposed in [37]. It uses a parallel shift register sequence generator (SRSG) and a multiple input signature register (MISR). The implementation is called Self-Test Using a MISR and a Parallel SRSG (STUMPS).

Figure 10 shows the general structure used for MCM testing. In this scheme all the shift registers in a die are concatenated in the test mode to form a single shift register latch (SRL). The test patterns generated by the parallel SRSG are shifted into the SRL of the dies using the scan-in ports. The number of clock cycles required is equal to the number of shift registers in the longest SRL on any die. This will cause shorter SRLs to overflow into the MISR but will not affect the correctness of the final MISR signature. After loading the stimuli into the latches, the machine clocks are cycled to capture the test results. The shift registers are then unloaded into the MISR, simultaneously loading the next pseudo-random pattern set from the SRSG. Whether the MCM is faulty or fault free is determined by comparing the signature with the expected signature.

The MISR and SRSG could be implemented as two test dies or could be incorporated in the design of a die in the MCM itself. Subsequent work in [31] applies the outputs of various dies to a linear space compressor instead of a MISR. This technique not only detects faults but also identifies the faulty die. The outputs from
all the dies are compressed into two bits using linear space compressors and compared with two reference signals generated for a fault free system in a comparator. If they differ, fault is detected and the faulty die is identified using \( N = \log_2(M + 1) \) and \( M \) denotes the number of dies in the MCM. This approach provides speedy identification of faulty die. Further, the additional hardware is minimal and can be implemented on an FPGA [31]. These schemes are only applicable to at-speed functional test of the dies on an MCM and are used specifically to identify the faulty ones. They do not address the substrate interconnect test problem.
6 Analyzing MultiChip Module Testing Strategies

Many MCM test strategies have been proposed over the last few decades. The MCM manufacturers have a large variety of test solutions to choose from to incorporate into their MCM design. It is imperative that they choose those techniques that best satisfy them and fulfill their requirements. Towards this end, it is essential that some metrics be defined based on which the numerous test solutions could be graded. Over the years, researchers [6, 38, 39] have proposed several test analyzing strategies.

The two primary quantitative metrics defined to serve as the basis of comparison between the MCM test approaches are:

- Impact on the cost of the MCM.
- Impact on the quality of the MCM measured by the defect level (in parts per million) in the produced MCMs.

The selection of cost as one of the comparison metrics reflects the important role that test plays in determining the final cost of an MCM. It also emphasizes the importance of finding cost-effective solutions and not just test solutions at any cost. The second performance metric serves as a balance against recommending cheap solutions with inferior quality. Hence, the defect level of the produced MCM is used as a measure of quality. In addition to cost and quality, several other evaluation criteria could be used to reduce the search space by eliminating from consideration test methods that do not meet certain expectations and/or constraints. Examples of these criteria are:

- Impact of a test strategy on time to market.
- Capability, extendibility and limitations of test strategy for various design complexities, such as circuit size, pin count, technology variations, and maximum speed.
- Adverse impact of a test method on the reliability of the product.

- Usefulness of a method at higher levels of integration and for field test, diagnosis and maintenance.

- Electrical performance degradation caused by a test method.

- Impact of a test method on manufacturability.

In this report we consider the effect of MCM test strategies on cost and quality of MCMs only, neglecting the other criteria. We present an application specific testability trade-off analysis for a leading edge MCM test vehicle that has been performed by MCC's Commercial Open Systems Consortia Project. The results have been presented in [6, 38]. This MCM contains a large CPU, a large coprocessor chip, and ten 4-Mbit SRAM chips. Five cases of MCMs are analyzed for cost and quality in this section.

The first case is the testability base case defined to serve as the basis for comparing the various test strategies. All the dies are tested at the wafer level by probing methods. After the wafer is diced, the die passing the wafer test are attached to temporary die carriers and the dies are burned in and electrically tested. The substrate is an MCM-L substrate on which the dies are flip-chip bonded. The substrate with interconnections is pretested accurately prior to MCM assembly. The CPU and coprocessor are fully boundary scan standard 1149.1 compatible. However, no BIST is available inside these chips. Further, the SRAMs have no BIST or B-S available for use during testing.

The second case has BIST features in the CPU and coprocessor only, while the other chips are nonBISTed and nonB-Sed.

The third case includes BIST and BS in all the chips (CPU, coprocessor, SRAMs).

The fourth case has a test controller die (TCD) incorporated into the MCM. The test controller acts as the primary test interface of the module to the external
board via a standard test bus interface. It has a test pattern generator and signature evaluation circuitry incorporated into it.

The fifth case employs the use of a partial assembly, test and rework process for the MCM. The MCM is assembled in two phases. In the first phase, the SRAMs are attached to the MCM, tested and repaired (if necessary). Then in the second phase, the CPU and coprocessor are attached, and the full module is tested and repaired. Only the CPU and coprocessor are B-S compatible and all the dies are non-BISTed.

The base case MCM cost was computed to be $846 and the defect level was 10,437 ppm. The cost and defect level for the other cases are listed in the table below.

Table 1: Analyzing Test Strategies.

<table>
<thead>
<tr>
<th></th>
<th>Cost ($)</th>
<th>Quality (ppm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Base Case</td>
<td>846</td>
<td>10437</td>
</tr>
<tr>
<td>Partial BIST</td>
<td>829</td>
<td>2039</td>
</tr>
<tr>
<td>Full BIST</td>
<td>805</td>
<td>1885</td>
</tr>
<tr>
<td>Test Controller</td>
<td>845</td>
<td>2149</td>
</tr>
<tr>
<td>Partial Assembly</td>
<td>795</td>
<td>4589</td>
</tr>
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</table>

We now analyze the test schemes. In case of partial BIST and full BIST, the initial cost of adding BIST is more than offset by the test cost reduction that results from its inclusion. The test cost is reduced at wafer, die and MCM level due to the very high fault coverage enabled by the BIST in a short time. The incorporation of BIST significantly improves the MCM quality. A reduction in cost of 2% to 3% results in the partial BIST case, while a savings of about 5% is realized for full BIST case. The most impressive result from the inclusion of BIST is an almost 80% reduction in the defect level of MCMs (quality in ppm).

It can also be observed that the MCM test cost did not improve by a large margin when a test controller die is used as the cost of the test die itself is large (around $60). However, the defect level of the outgoing MCM decreases by a factor
The partial assembly, test and rework strategy makes it possible to efficiently test the SRAM dies in parallel. A cost improvement of about 6% is realized and the MCM defect level drops by more than half.

Summarizing the above table, we observe that the full BIST has the lowest defect level, but the partial assembly case has the lowest cost. Hence to obtain the most economical long-term solution that takes into consideration subsequent testing requirements is the use of BIST and B-S based solutions in manufacturing the MCM.

Hence the analysis of the trade-offs associated with test strategies for MCMs clearly indicates that incorporating B-S and BIST at die and MCM levels results in optimal cost reduction as well as quality improvement.

7 Conclusion

This report presents Design For Testability techniques for MCM test problem. Several test approaches employing Boundary-Scan and Built-In-Self-Test are presented for enhanced testing of MCMs. These strategies need to be considered during the early design stages, and help in meeting the MCM quality requirements. They impact the test process at the wafer level, die level, module level and beyond.

To properly weigh the benefits of these approaches, two primary metrics are defined to serve as the basis for comparison. The analysis of the test strategies for MCMs clearly indicate that incorporating Boundary Scan and Built-In-Self-Test features at die and MCM level provides maximum quality improvement at minimum costs.
References


A. Chatterjee and Dave Schimmel attended the third NASA New Millenium IPDT meeting from 9/18-9/21 (1995) and a workshop in San Antonio from 10/12-10/15. At these meetings besides roadmapping activities, the idea of developing a low-power asynchronous message router architecture for a flight experiment was developed. It was proposed to build a simple asynchronous router to route messages between a small array of processing elements. The idea was to demonstrate fault-tolerant routing protocols that would have very low power consumption constraints while achieving highly reliable message routing.

Also, the task of testing the 3-D MCM stack to be used in the microelectronics architecture was clearly defined in this meeting. Discussions with Space Computer Corporation and Loral Federal Systems Divisions resulted in a clear definition of the testing task. Also, Loral sent Georgia Tech descriptions of their dual-processor CPU which were analyzed to develop a clear testing strategy for the microelectronics architecture.
Flight Experiment:
Low Power, Scalable, Fault-tolerant Router Technology

David E. Schimmel, Sudhakar Yalamanchili, Abhijit Chatterjee

School of Electrical and Computer Engineering
Georgia Institute of Technology
Experimental Goals

- Demonstrate router technology which is:
  - Low power and power scales with load
  - Scalable from a few to many processors
  - Highly reliable in the presence of static and dynamic faults
  - Retains high performance even in the presence of faults

- A flight experiment is required to:
  - Validate asynchronous design methodology in space
  - Validate fault-detection and distributed recovery in a realistic mission environment
  - Investigate the trade-offs between performance, fault-rate and supply voltage for asynchronous designs
Asynchronous → LP and Scalable

- Multiprocessor communication is bursty
  - Asynchronous design achieves LP because power is directly proportional to network activity — if there are no messages in the network, no power is consumed.
  - Clock distribution consumes significant fraction of overall power, especially when low skew is required, hence no clock implies LP

- Scalability implies processors may be added without impacting system implementation
  - Scalable because synchronization is implicit

- Challenges
  - Difficult to design and verify – must use formal methodology.
  - Must use arbitration for non-deterministic choices.
Asynchronous Example

- Two-phase or four-phase handshake between stages

  ![Handshake Diagram]

- Stage design:

  ![Stage Design Diagram]

- Formal Specification (CSP like)

  \[ \text{\star} \left[ (r_i \land \neg r_{i+1}) \rightarrow a_i \uparrow \parallel (\neg r_i \land r_{i+1}) \rightarrow a_i \downarrow \right] \]
Ariadne - A Self-Timed MB-m Router

- Prototype is for k-ary 2-cubes
- 8 bit half duplex channels
- 2 virtual channels/physical link
- Control channels share a single virtual channel
Ariadne - Performance Results

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Values (ns)</th>
<th>Parameters</th>
<th>Values (ns)</th>
</tr>
</thead>
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<td>Data Path</td>
<td>7.25 +T_{arb}</td>
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<td>10 - 12</td>
<td>Link Cycle (1)</td>
<td>10.15 +t_{sync} +2t_{pl}</td>
</tr>
<tr>
<td>RCU (ack)</td>
<td>5</td>
<td>Link Cycle (3)</td>
<td>9.65 + 2t_{pl}</td>
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<tr>
<td>RCU (bck_hdr)</td>
<td>12 - 14</td>
<td>Link Arb. Time</td>
<td>4.3</td>
</tr>
</tbody>
</table>

Georgia Tech

JPL On-Board Computing Workshop
Direct Multiprocessor Networks

- Physically distributed memory for “scalable” memory bandwidth (busses saturate)
- Multipath networks increase effective bandwidth (and eliminate single point failure modes)
Adaptive Routing

- Congestion Avoidance

- Fault Tolerance

Georgia Tech
Communication Mechanisms

- Wormhole Routing
  - pipelined communication
  - low buffer requirements
  - low message latency

Georgia Tech
Pipelined Circuit Switching (PCS)

- Decouple data flow from path setup
- Increased flexibility in routing around faulty or congested links
- Supports non-minimal routing and backtracking search
- Increased setup time compared to wormhole routing
- No virtual channel restrictions

Georgia Tech
Acknowledged PCS

- Message acknowledgment eliminates time-outs
- Fault recovery—kill flit mechanism
- Graceful degradation
Faulty Pipelined Networks

- **Static faults**: Faults in existence before a message routes
  - WR routing algorithms no longer deadlock-free
  - Minimal routing disconnects some processors
  - Non-minimal routing necessary
  - Requires great flexibility in routing

- **Dynamic faults**: Faults occurring to links in an active virtual circuit
  - Data flits block indefinitely with no routing information
  - Fault recovery mechanism needed
  - Cannot be solved by routing
On-line Fault Detection

• Signature compression to ensure router integrity
  • Signature Compression Circuit (SCC) based on Linear Feedback Shift Register (LFSR)
  • Signature carried in tail flit, and recomputed on message entry to and exit from a node.

• Link time-outs to ensure progress

Georgia Tech

JPL Microelectronics IPDT
Experimental Strategy

- Simplified router core, with scan programmable message and fault injection
Experiment Architecture

- MCM array of routers, FPGA, shared telemetry & control

Other flight experiments on VME card

Experimental MCM

Telemetry Interface

Exp. IF & Fault Injection
Experimental Measurements

- Low and scalable power consumption properties of the asynchronous system through telemetry measurements under varying loads.

- Fault detection of both data and control faults, and associated fault masking and error recovery mechanisms through synthetic fault injection.

- Performance measurements of router technology over a range of supply voltage, including the interaction between voltage, power, fault rate, and performance for these asynchronous systems.
A. Chatterjee attended the fifth New Millenium Workshop from 11/14-11/17. The following proposal for testing/design for testability was the result of the meetings in which Georgia Tech participated.

1.0 Executive Summary

In order to ensure reliable operation of the proposed flight 1 architecture, viable solutions to the problems of design for testability (DFT) for off-line test and built-in self-test (BIST) of the 3-D stacked MCM flight system architecture will need to be developed. Due to the planned new technologies for the New Millenium space flights, these problems take on new dimensions, requiring new testability models and new test paradigms. In this proposal, we seek to address these problems with the goal of identifying architectures and related test protocols that enhance testability and allow easy incorporation of BIST.

The key elements of the proposed test strategy are described in Figure 1, above. Test of the microelectronics systems architecture will be initiated by first running a test program on the dual-processor CPU. This will verify the correct functioning of the CPU unit. Once the CPU is known to be functioning correctly, it will be used to test the rest of the architecture and provide diagnostics for reconfiguration and repair. The CPU may initiate BIST of architecture subsystems through control of the JTAG test architecture (BIST commands may be issued to hardware subsystems through the JTAG test protocol). Alternatively, the CPU may send test commands through the system busses and the tested subsystems may answer “go/no-go” via the communications busses involved. Specialized BIST algorithms and hardware for the different subsystems will be used to provide system-level BIST capability. The JTAG test bus configuration will be optimized to the

![Figure 1. Key elements of DFT/BIST strategy](image-url)
test requirements of the system architecture and 3-D stacked MCM package. The research deliverables will include the following:

- Test (BIST) software prototype that will exercise the different architecture functions and generate system diagnostics from careful analysis of test results (fault syndromes). This test software will exercise the JTAG boundary scan test architecture through the JTAG interface provided by the RAD6000 CPU architecture and execute functional test of the modules connected to the various busses and the busses themselves.
- Methodologies for designing highly reliable JTAG bus architectures through the use of redundant busses. The bus architecture will be optimized for test bus reliability and test time.

In the following, we first address design for testability issues to be investigated in this proposal and then discuss our proposed BIST methodology.

2.0 Technical Approach

We propose a modular BIST approach in which embedded BIST functions are exercised to yield a signature for the complete system architecture.

2.1 BIST of POWER PC module and Assembled MCM Stack

BIST of the microelectronics systems architecture will be enabled by running a test program on the dual-processor RAD6000SC CPU. If the CPU is deemed to be fault-free, then the test program will go into another loop to test all peripheral devices such as the solid state recorder, the bus interfaces, the test circuitry and the science/MEMS payload. Where possible, the test program will issue BIST commands to individual system modules through the JTAG test interface. It may also test chips using tests applied through the JTAG test interface. Testing of buses and bus interfaces will be performed through test of modules attached to the respective bus.

The test program will also be designed to allow maximum possible diagnosis of module failures. Fault syndromes will be constructed by cause-effect analysis of the effect of test procedures on faulty modules. By matching these fault syndromes to the observed fault effects, diagnosis may be performed down to a module or a small set of modules. Once diagnosis has been performed, spare modules may be switched in, disconnecting faulty ones.

2.2 BIST of Other System Functions

We will investigate use of novel BIST methods for BIST of all system functions. For example, the power control unit generates several different supply voltages. A simply way to test for correct operation of the power control unit is to compute a weighted checksum of the generated supply voltages in such a way that the checksum is zero in the fault-free case. Other BIST methodologies will be examined in collaboration with other IPDT members. We will also make recommendations to other IPDT members on use of existing BIST technologies (such as based on current sensing) where feasible. For example, it is almost imperative that some form of parallel BIST of the solid state recorder be performed. The various data busses and bus interfaces will be tested by
sending commands to modules attached to the respective busses from the CPU. Signatures computed by a module in response to commands issued by the CPU over the concerned bus will be transmitted back to the CPU for verification.

Several key issues related to the use of JTAG boundary scan test techniques in 3-D stacked MCMs will be addressed:

2.3 Test, diagnosis and repair of the JTAG boundary scan bus

Prior to application of any test stimulus through the JTAG boundary scan bus, comprehensive testing of the bus will be performed for opens and shorts. Mechanisms for bus repair will have to be provided in case of bus failure. Redundancy in the JTAG test architecture will have to be provided to aid in fault diagnosis and repair/reconfiguration.

2.4 Optimal boundary scan configuration and test procedure

Given the test sets for all the modules to be applied via boundary scan, the number of scan registers for each module and known sets of identical modules, we propose to find the optimal JTAG boundary scan interconnections between modules and the optimal functional and interconnect test procedures so that complete test of the modules as well as the module interconnections can be achieved within a minimal number of test cycles under specified test I/O restrictions and in the presence of multiple scan chains.

2.5 Testability of analog functions and A/D, D/A interface

Fault models for analog functions will be used to define test strategies for off-line testing, online error detection (if desired) and built-in self-test.

3.0 Deliverables

The deliverables include the following:

1. Report describing proposed test architecture framework for microelectronics systems architecture developed in collaboration with Loral and Boeing. This will include descriptions of hardware/ASICs used to enhance testability as well as test algorithms based on this hardware.

2. Prototype BIST software for the Loral RAD6000 dual-processor CPU with diagnostics.

3. A report describing methodologies, algorithms and software (year 2, if applicable) for designing and testing highly reliable redundant JTAG bus architectures.

4.0 Schedule

- Test architecture definition
- Preliminary BIST software
- Reliable and testable JTAG bus
- Bus reconfiguration strategy

Jan Feb Mar Apr May Jun Jul Aug Sept Oct Nov Dec
1996