TCAD SIMULATION FRAMEWORK FOR THE STUDY OF TSV-DEVICE INTERACTION

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TCAD SIMULATION FRAMEWORK FOR THE STUDY OF TSV-DEVICE INTERACTION

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TABLE OF CONTENTS

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LIST OF TABLES

LIST OF FIGURES

SUMMARY

3D IC technology is seen as a potential solution to achieve high performance, complex functionality, a small footprint, and lower power required of modern ICs. Through-Silicon Via (TSV) technology is critical to realizing 3D ICs, because of its advantages compared to other interconnect technologies like wire bond and flip-chip. However, TSVs also introduce challenges that need to be evaluated and addressed during fabrication, design, or layout. In this dissertation, the variation in device performance due to TSV-induced mechanical stress and electrical field coupling between TSV and device are studied using three dimensional TCAD process and device simulation. The analysis considering 40 nm and 28 nm high-k metal gate transistors demonstrates that the TSV only has a minor impact on the off, linear, and on currents of short-channel devices, and that the effect diminishes with technology scaling. The study also shows that the effect of mechanical stress and that of electric field coupling are comparable. Moreover, at current and future technology nodes, their combined effect on performance and leakage can be marginal even at small distances, allowing more aggressive definition for the keep-out zone (KOZ).

INTRODUCTION

As transistors continue to be scaled to smaller technology nodes, it is imperative for packaging and interconnect technologies to keep up in order to meet system demands. 3D integration has emerged as an attractive solution to this demand from the perspectives of performance and functionality [1] [2].

3D integration offers many advantages. The first being a reduction in system/package size, since 3D assembly/integration of dies typically results in a much higher packaging density than planar assembly techniques. The second advantage is an improvement in performance. Interconnections between dies in a 3D stack are typically shorter due to the reduced distance between them. This results in a reduction in signal delays, allowing higher frequency operation. Another advantage of shorter interconnects is a reduction in power consumption, since the signals have to be delivered over smaller distances.

3D integration also makes sense from a functionality standpoint. With the industry focused on integrating more and more functionality on a single SOC die, the challenge is to integrate a wide variety of functionality that may require disparate manufacturing technologies and optimization techniques. Performance, stability, yield and other considerations may dictate the use of different technologies and/or processes, or different configurations and/or optimizations within a particular technology or process, for different applications, like analog, logic, and memory. A decision may also be made to integrate certain passive components, or MEMS devices, etc. on the SOC rather than outside it. In such cases, separating the varied functionality based on the technology and process considerations, assigning them their own dies, and then interconnecting the dies would seem to be the best solution. 3D integration makes this solution possible. Such an approach is apt for say, a CPU that typically consists of logic and memory, in which we

could stack the memory and logic using 3D interconnects, instead of a 2D approach, in which the memory lies to one side of the logic. The 3D solution would result in lower average and worst-case delays, thus allowing for better performance. It also simplifies the process steps required to fabricate each die constituting the stack.

An additional benefit of 3D integration allowing us to separate a system or SOC into multiple dies is that the different dies needn't be homogenous, that is, they needn't be manufactured using the same or even compatible processes. For example, certain image sensing applications may require the use of substrate materials incompatible with Si-CMOS processing for the sensor array, but require high-density circuitry to read the signals from the array, which is best achieved using nanometer node CMOS technologies. In such a case, we could simply manufacture the sensor array and the reading circuitry separately, and connect the two dies using 3D interconnects.

Out of the different methods of connecting dies/wafers, through-silicon-via (TSV) technology has emerged as the 3D interconnect technology. TSVs result in a greater reduction in signal delay and power dissipation compared to wire-bonds. Also, a much higher interconnect density can be achieved with TSVs than with wire-bonds, which require landing pads on both dies for making connections. The higher density enables a much higher bandwidth of operation.

TSVs have lower inductance compared to wire-bonds, as bond wires are typically longer. Also, due to the small distance between two wires, inductive coupling is higher between bond wires.

While TSVs offer many advantages compared to other interconnection methods for 3D IC development, they also raise a number of concerns with regards to scaling and reliability.

Issues pertaining to TSV scaling include the increasing aspect ratio, poor step coverage of the dielectric and metal layers, increase in RC delay because of a limit on how thick the dielectric oxide can be made (which in turn limits the reduction in TSV capacitance), and degradation in joining performance attributable to bump size scaling.

Reliability issues arise from the mechanical and thermo-mechanical stresses that are caused during manufacturing, and their effect on both thermal, mechanical and electrical durability and performance, as well as copper contamination (copper being the most commonly used TSV metal owing to its excellent conductive properties).

Mechanical stresses occurring in a 3D wafer or die can be altered by the wafer thinning process (which is a stress relieving process), CTE mismatch between the bump and adhesive layers, and finally, CTE mismatch between the copper TSV and silicon substrate.

This last cause of mechanical stress, the CTE mismatch between copper TSV and the silicon substrate, is interesting, and needs to be examined in detail. While the mechanical stress caused by this CTE mismatch between copper TSV and silicon substrate can cause physical damage in the substrate, and make it weaker, the induced stress can also affect the performance of transistors that are within its range of influence. Moreover, mechanical stress will impact the performance of transistor circuits in all dies. Therefore, it needs to be understood, and rules and/or design choices need to be made to account for it. One solution is to have a safe keep-out-zone (KOZ) around the TSVs such that the impact of mechanical stress is negligible. However, a large KOZ increases the area and cost overhead.

In order to ensure reliable device and circuit performance in a 3D IC employing TSVs while ensuring maximum area usage and thus minimum cost, the design rules and/or choices need to be optimized, considering the effect of mechanical stress. Therefore, accurate

analysis of TSV-to-device coupling effect is important, and is the focus of this thesis. The methodology employed is a 3D TCAD framework to simulate the process flow that would be used to manufacture a 3D ICs with transistors in bulk-CMOS technology and copper TSVs interconnects, and device simulations to characterize the current-voltage characteristics of the transistors, accounting for the stress using appropriate physical models, analyzing the results obtained, and comparing them with changes caused by the electrical coupling between TSVs and transistors, to put them in perspective.

LITERATURE STUDY

With 3D ICs becoming an increasingly attractive solution, and TSVs heralded as the interconnect technology to enable them, researchers have been looking at various aspects of TSV technology, right from their manufacturing, to the issues that might prove to be a hindrance in realizing 3D ICs with TSVs.

Lu et al [3] used finite element analysis (FEA) to study the thermal stress distribution due to a single TSV, and investigated three different TSV structures. The authors concluded that using a hybrid TSV structure (using a layer between silicon and copper designed to reduce the impact of the CTE mismatch between the two) results in lower values of stress along the direction of propagation. A hybrid structure would also avoid current leaking into the silicon from the copper (due to ineffective side-wall passivation).

McDonough et al performed thermal and spatial profiling of TSV-induced stress in 3D ICs using experimental methods and simulation [4] [5]. The authors found that the stress in silicon is caused during the thermal annealing process, and that in the case of an array of Cu-TSVs, morphological modification of the copper due to thermal annealing is correlated to substantial changes in the intra-array stress profiles.

Athikulwongse et al [6] analyzed the impact of the choice of KOZ distance from TSVs on mechanical stress, carrier mobility, area, wirelength, and performance of 3D ICs. They found that the use of a large KOZ could successfully counteract the impact of TSV induced stress on carrier mobility, but at a significant area and wirelength penalty. They proposed a solution that takes into account TSV-induced stress mobility variation to do more aggressive placement, which results in an area saving when compared to traditional wirelength driven placement, while extracting best circuit performance.

Okoro et al [7] analyzed the induced stresses in silicon during thermo-compression Cu-Cu bonding of copper TSVs, and found that the temperature during the thermo-compression process is the main cause of induced stress, and not the bonding force used. They also found that the residual stress observed post-bonding is a result of the heat treatment employed in sintering back-end-of-line (BEOL) copper. They established that a PMOS is more sensitive to changes in stress caused by the TSV compared to an NMOS, and hence would be the one to influence the keep-out zone (KOZ). They also found that the extent to which stress propagates from a copper via depends on its diameter.

Chang et al [8] found that the diameter of the TSV is a key factor in determining not only the distance to which the stress propagates from the TSV, but also the amount of stress. The greater the diameter of the TSV, the higher the stress, and the greater the distance to which the stress propagates from the TSV. They also studied the impact of an array of TSVs, and found that the impact of an array of TSVs is more than that of a single TSV. The key finding of this work was that using smaller diameter TSVs would reduce both the stress caused by the TSVs, as well as the KOZ.

Mercha et al [9] modeled the effect of stress due to a single TSV and an array of TSVs on neighboring NMOS and PMOS transistors for analog and digital applications. They compared the results of their model with measurement data, and found that the impact of TSV-induced stress on performance is much greater for analog circuits than for digital ones. They also found that this holds true in the case of a TSV array as well, except that the effect is more pronounced. They concluded that the keep-out zone (KOZ) would have to be greater when designing an analog circuit compared to a digital circuit, and it would also have to be greater for a TSV array compared to a single TSV.

Finally, West et al [10] measured electrical characteristics for a 28 nm high-k metal gate NMOS/PMOS device located in the proximity of a single TSV and an array of TSVs. They performed the experiments for three different orientations of the TSV with respect to the transistor channel: lateral, longitudinal, diagonal. They also varied the distance between the transistor and TSV. They found that the change in on and off currents is negligible (small enough to be tolerated) even at fairly small distances (> 4 μm), and that CMOS circuits could be placed at distances much closer to TSVs than previously thought, depending on the application.

Apart from the mechanical stress caused by TSVs affecting transistor performance, electric field coupling between a TSV and transistor can introduce noise and affect performance of the transistor.

Khan et al [11] characterized the TSV-induced noise as a function of several crucial design and process parameters, including signal slew rate, TSV height, ILD thickness, and distance between TSV and device and between TSVs. They found that the noise can be quite significant, especially in a high resistance substrate, and that aggressive shielding is required in order to counteract the effect. Techniques for doing so were proposed, and include using a backside ground plane, using coaxial TSVs, and using EPI substrates.

Cho et al [12] also studied noise coupling between active circuits and TSVs, and found that noise coupling is significant (because of low immunity to substrate noise coupling) and adversely impacts analog and RF performance. They proposed a model for the coupling noise, using which they investigated the effect of substrate coupling noise and the effectiveness of using a guard ring structure as a solution for noise isolation.

Chuan Xu et al [13] studied EM coupling noise from TSVs to active regions in various 3D IC technologies, and developed compact models for bulk-CMOS technology, ratifying it against simulation results, so that they can be used to calculate KOZ for 3D ICs.

Trivedi et al [14] analyzed the through-oxide via (TOV) induced back-gate effect on the characteristics of FDSOI devices, and found that the change in potential modulates the threshold voltage of the devices, thereby affecting the current, especially leakage current. Leakage current and hence power were found to be a function of TOV potential, as well as distance between TOV and the device. This conclusion was that this effect must also be considered when designing and laying out circuits.

Motivation

While several works have studied the effect of TSV-induced mechanical stress on transistor performance, and several others have studied the effect of TSV-device electric field coupling on transistor performance, and each of them recommend or provide models to set an appropriate keep-out zone (KOZ), there was a need for a detailed and combined study of these two effects, so that their relative importance could be gauged, and calculation of KOZ based on which effect produces greater variation in performance. With this in mind, we developed a 3D TCAD process flow and device characteristics simulation framework to quantify and analyze the impact both of these effects for bulk-CMOS technology.

SIMULATION SETUP

Three dimensional Technology CAD (TCAD) simulations are performed to quantify the effect of TSV induced stress on bulk-CMOS transistors. To understand the impact of strain/stress on the performance of NMOS and PMOS transistors, we simulated three different orientations between a TSV and a 28nm NMOS and PMOS device (figure 1), with the distance between the TSV and transistor fixed at 2.5 µm in each case. Using this setup, first a single TSV and transistor is simulated. Next, simulations are performed to quantify the change in currents of an NMOS/PMOS transistor when placed inside a grid of TSVs [8] [10]. These multi-TSV grid simulations are performed for two different cases: 4-TSV grid i.e. a transistor is surrounded by four TSVs, each TSV oriented diagonally with respect to the transistor, and 8-TSV grid i.e. a transistor is surrounded by eight TSVs (Fig. 1b), with four TSVs oriented diagonally, two perpendicularly, and two laterally with respect to the transistor.

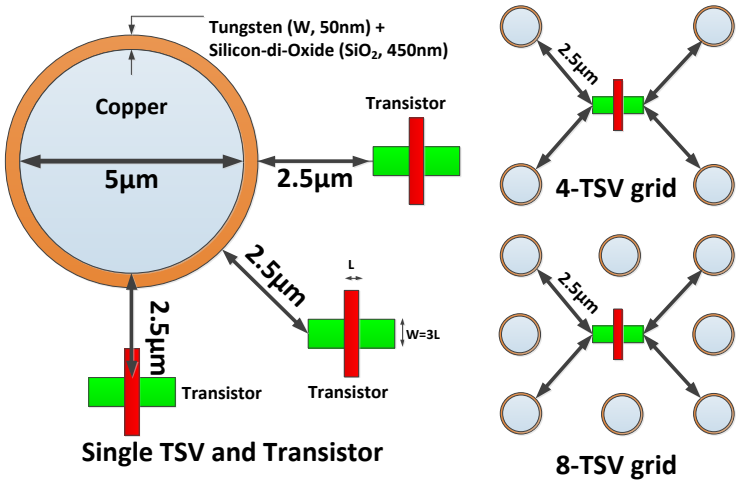

Figure 1: The 3D TCAD simulation framework for TSV-to-device coupling for the 28 nm transistor

Simulations are also carried out to understand the effect of increasing the separation between the transistor and TSV, by performing a set of simulations with the distance between the transistor and TSV increased to 4 µm, and comparing the results with those obtained when the TSV and transistor are only 2.5 µm away from each other.

Lastly, considering that a 3D package may consist of dies employing different technologies depending on the application, simulations are carried out to understand how the impact of stress/strain changes as the transistor has been scaled down. Simulations have been performed for transistors fabricated at 180 nm and 40 nm, and the results compared to those obtained with the 28 nm transistor.

Process Simulation

Sentaurus Process [15] is used to simulate the process steps for fabricating the NMOS/PMOS transistor, and the TSVs.

The transistors are fabricated to match the specifications required by ITRS for a low operating power (LOP) transistor [16]. Low operating power transistors are employed in applications that require the circuitry to be always on, such as in image sensors which capture images continuously, or proximity sensors employed in vehicles.

Figure 2 illustrates the process flow for fabricating a 28 nm n- or p-type bulk-CMOS transistor. The same process flow is simulated for the 40 nm NMOS and PMOS transistors as well. For the 180 nm transistors, a traditional poly-silicon gate is employed instead of a metal gate, and high-k oxide isn't used as it is unnecessary in that technology.

The transistors have been grown on <100> silicon, with the channel oriented in the <110> direction. Hafnium Oxide is used as the high-k dielectric, with a thin layer of SiO_2 used as

sacrificial oxide layer. The use of a metal gate in conjunction with a high-K dielectric has been shown to improve the electron/hole mobility by effectively screening surface phonons. For the NMOS transistor, TiN, which is a mid-gap metal, is used as the gate metal.

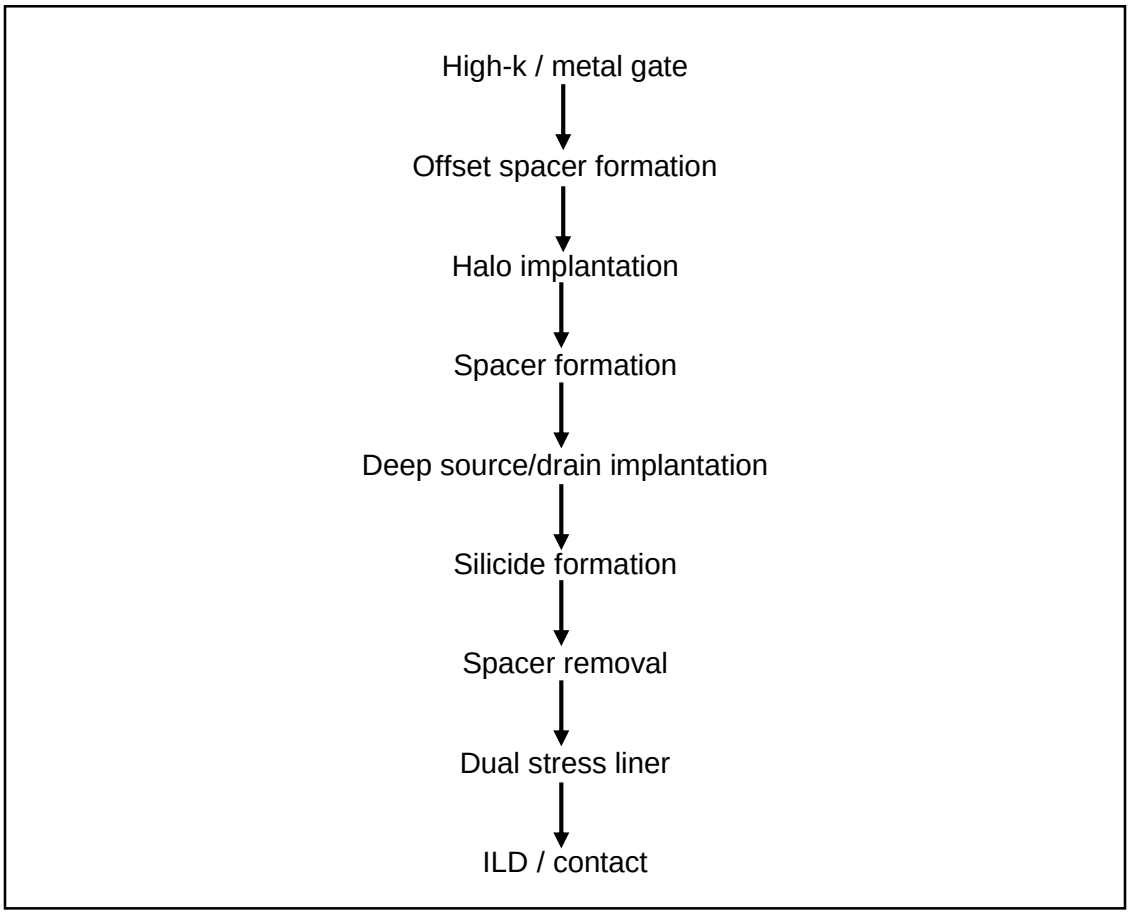

Figure 2: Process flow for fabricating a 28 nm high-k metal gate transistor

Doping concentration for the source and drain regions is ~ 1E20, while both halo doping and a retrograde doping profile are used to adjust the threshold voltage of the device and account for the short-channel effect.

Dual stress liners are utilized to introduce tensile stress in the NMOS transistor and compressive stress in the PMOS transistor to improve performance. To maximize the benefit of stress, the nitride spacer is removed following the source and drain implantation step and before the deposition of the dual stress liners [17]. The thickness of the nitride layers used is ~75 nm. The stress relaxation time is 100 ps at a temperature of 600 °C.

Via-middle process is used to simulate fabrication of TSV and transistor. Figure 3 illustrates the via-middle process flow, in which the FEOL features are fabricated before TSV filling and metallization.

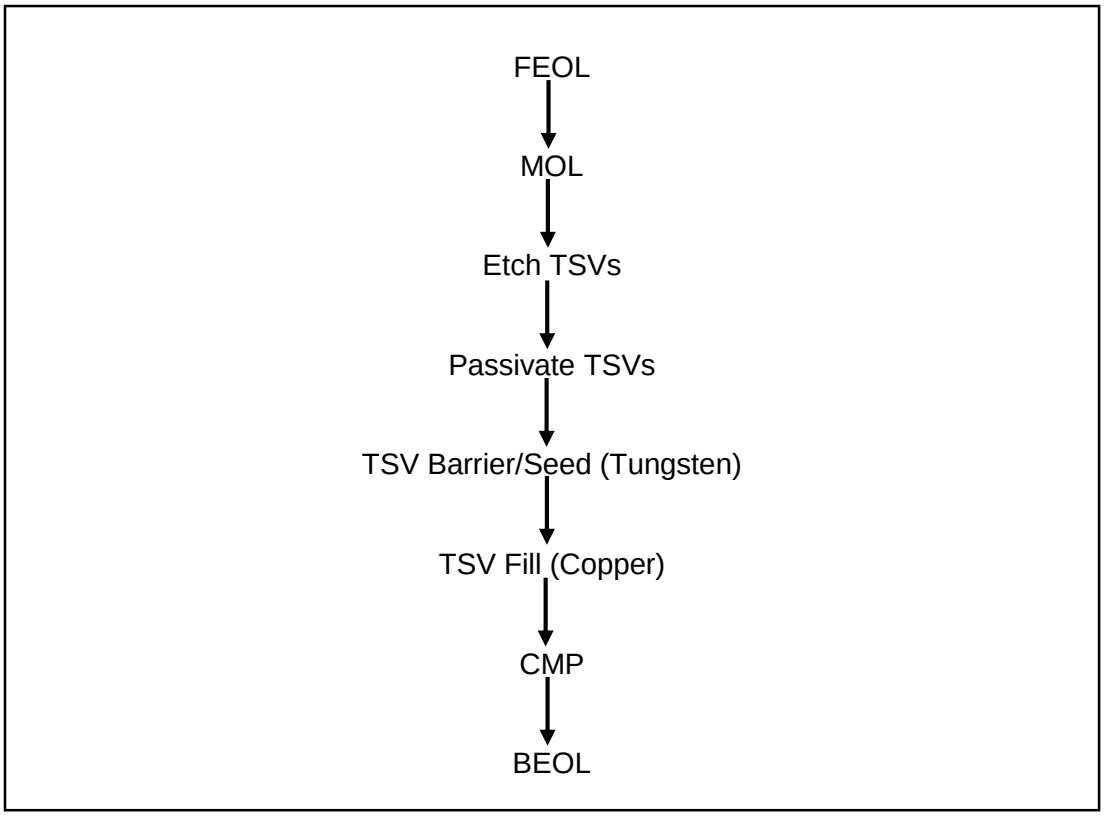

Figure 3: Via middle process flow

The trench for the TSV interconnect is created using the Bosch DRIE process, alternating between SF_6 etching and C_4F_8 passivation. The trench is coated with 450 nm of silicon dioxide and 50 nm of tungsten before filling it with copper, which is the interconnect metal of choice. The SiO_2 and Tungsten layers are used to lower the CTE mismatch between bulk silicon and copper interconnect in order to reduce stress, which is beneficial from the standpoints of transistor performance and mechanical reliability.

Device Simulation

Electrical characteristics of the transistors are simulated using Sentaurus Device [18]. TSVs are biased at logic '0' or logic '1' to account for the electrical field coupling between TSV and device. For an NMOS device, when the TSV is biased at V_{DD}, the field originating from the TSV can cause a marginal forward body-bias, resulting in reduced threshold voltage (V_{th}). Similarly for a PMOS device, a TSV biased at 0V (grounded) results in a marginal forward body bias. Hence, the threshold voltages of NMOS and PMOS are expected to reduce with TSV = 1V and 0V, respectively.

For all simulations, the following options/models were enabled:

- SRH recombination
- Band-to-band tunneling
- Enhanced Lombardi model
- Bandgap narrowing
- High-field saturation

Stress induced electron and hole mobility modification is simulated through models in [18]. A description of the models used for electron and hole mobility changes follows. The effect

of stress on the threshold voltage is accounted for in the simulation, with an increase in stress resulting in a reduction in threshold voltage.

Strain-Si Mobility Model for Electrons

For electron transport, the strain-Si mobility model [18] accounts for the lowering of the two perpendicular valleys (Δ_2, in the z-direction) with respect to the four in-plane valleys (Δ_4, in the x- and y-directions) as a result of the applied tensile strain. This in turn results in more electrons occupying the Δ_2 valleys, where the effective mass of electrons is much lower compared to that in the Δ_4 valleys, which are now more sparsely populated by electrons as a result of the redistribution. Lower electron density in the Δ_4 valleys also results in lower inter-valley scattering. These two effects combine to enhance electron mobility. The model accounts for modification of deformation potentials, which also result in a change in mobility. Electron mobility in the presence of strain is calculated using the following equation:

$$\mu_{n,ii} = \mu_{n0}\left[1 + \frac{1 - \mu_{nl}/\mu_{nt}}{1 + 2\,(\mu_{nl}/\mu_{nt})}\left(\exp\left(\frac{\Delta E_c - \Delta E_{c,i}}{kT}\right) - 1\right)\right]$$

where:

- μ_{n0} is the electron mobility in the absence of any strain.
- μ_{nl} and μ_{nt} are respectively the electron longitudinal and transverse electron masses in the subvalley.
- subscript i indicates a direction ($\mu_{n,11}$ is the electron mobility in the direction of the x-axis, i.e., the direction of the channel for the transistors in this work).
- ΔE_c is the average of the conduction band shifts of the three Δ_2 valleys in the direction of the x-, y- and z-axis.

- $\Delta E_{c,i}$ is the conduction band shift taking place in the Δ_2 valley in the i^{th} direction ($\Delta E_{c,i}$ is the shift in the Δ_2 valley in the direction of the x-axis).

Within this electron strain-mobility model, the following options were enabled so that the model is consistent and physically correct:

- Calculation of the strained electron effective mass in order to account for a change in effective mass of electrons due to strain.
- Calculation of quasi-Fermi levels for the electrons which impacts electron redistribution between bands.
- Inter-valley scattering of electrons.

Intel Stress-induced Hole Mobility Model

For hole transport, Intel's stress-induced hole mobility model [18] [19] was enabled, which models modification of band structure of the topmost valence band under stress (from the fourfold symmetry of the two ellipsoidal bands in the unstressed condition). Under stress, the symmetry is broken by virtue of splitting of the maximum energy associated with these bands, with holes partial to occupying the upper valley. The applied stress also changes the transverse and longitudinal hole effective masses of the two ellipsoidal bands. These two effects contribute to a change in hole mobility.

As with the electron strain-mobility model, the option to calculate quasi-Fermi levels for holes in the valence band, and then apply those values to carrier redistribution, was activated.

RESULTS

Table 1 below contains the key electrical characteristics of the baseline 28 nm NMOS/PMOS, which is simply a transistor without a TSV in its vicinity. Figure 4 shows a transistor surrounded by four TSVs, with the various dimensions of the transistor and TSVs not drawn to scale, but proportioned correctly. The figure also shows a magnified version of the transistor showing the source and drain regions, gate, and nitride stress liner. The figure also shows the point of observation of stress in the channel.

Table 1: Characteristics of the 28 nm NMOS and PMOS transistor obtained from TCAD simulations

	28 nm NMOS	**28 nm PMOS**
I_{on}	749.7 µA/µm	464.8 µA/µm
I_{off}	2.994 nA/µm	3.008 nA/µm
I_{lin}	123.9 µA/µm	76.9 µA/µm
Sub V_T Slope	85 mV/decade	88 mV/decade

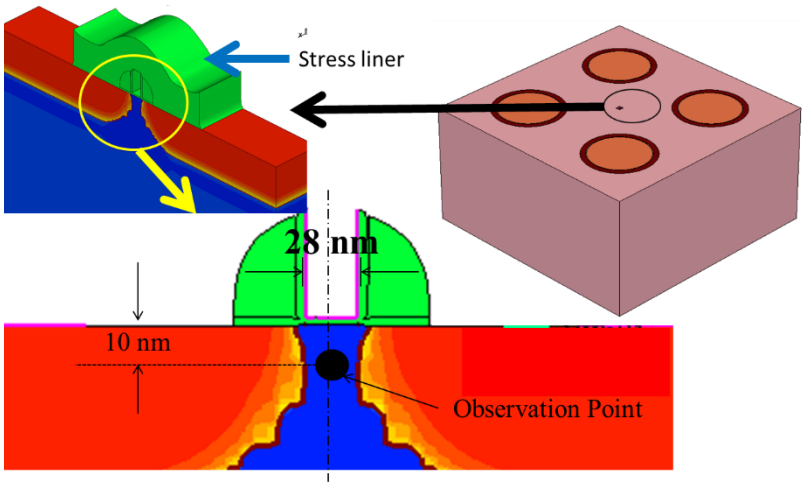

Figure 4: 3D simulation structure showing the TSVs and the transistors, and the point in the channel for measuring stress

Figure 5 shows the strain/stress distribution for the baseline 28 nm NMOS transistor. The strain is greater at the edges of the channel, where the nitride liner is very close to the source and drain regions, separated only by the oxide. The strain is comparatively lower in the center, where the thickness of the gate results in greater separation between nitride liner and channel.

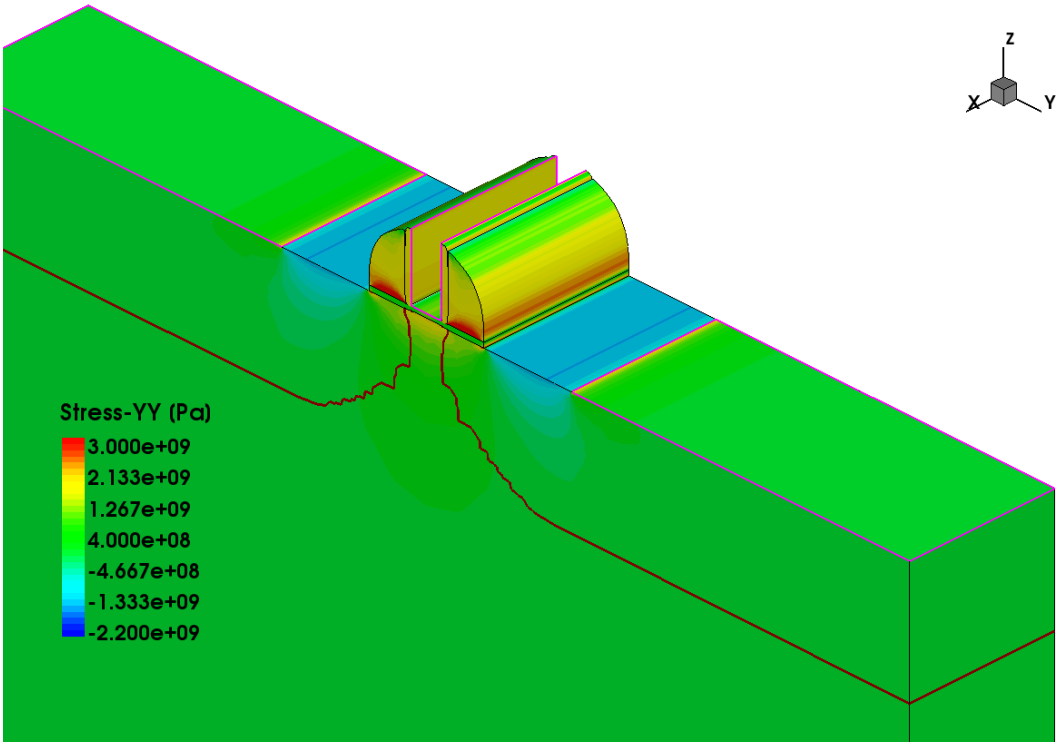

Figure 5: Stress distribution in and around the channel of 28 nm NMOS without a TSV present

Figure 6 shows the stress/strain pattern for the 28 nm NMOS transistor with a 5 µm diameter TSV at a distance of 2.5 µm to its left (figure 1). The stress/strain pattern is similar to the one before, except for a marginal increase in tensile strain (100 – 200 MPa) in and around the channel. The analysis of the electrostatic potential at the center of the

channel shows that with the TSV at 1V, the substrate potential close to the channel increases marginally, resulting in a reduced threshold voltage.

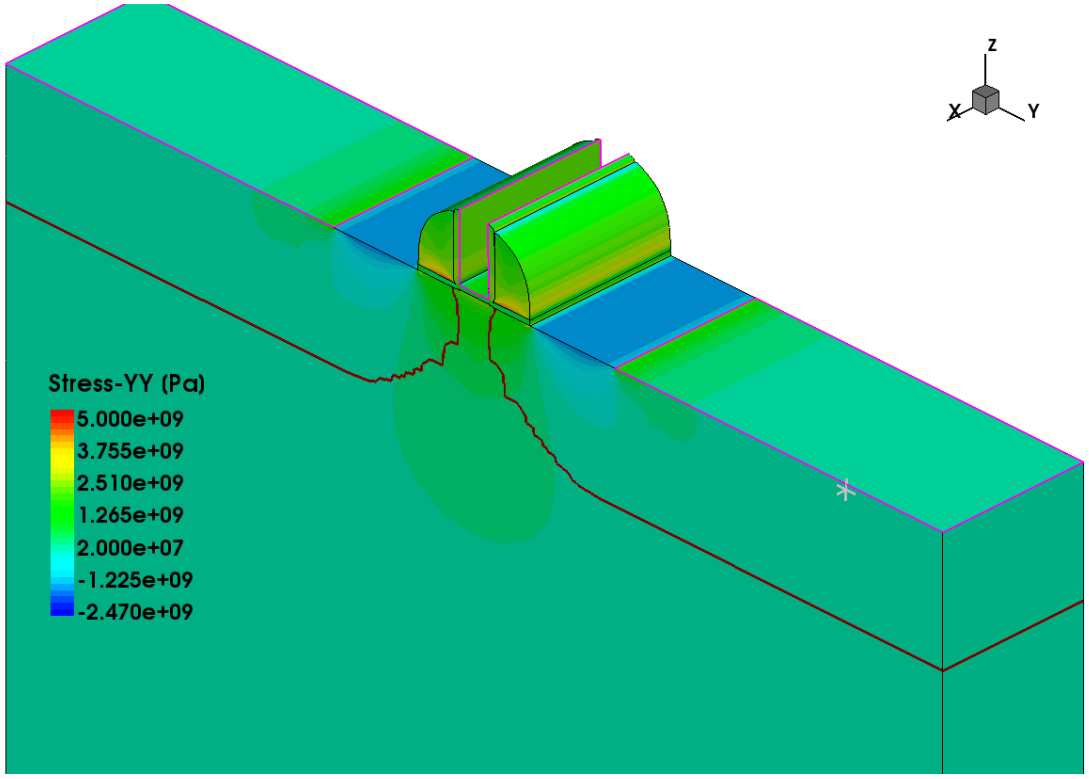

Figure 6: Stress distribution in and around the channel of 28 nm NMOS with a TSV 2.5 µm to its left

Coupling Between a Transistor and a Single TSV

Table 2 provides a summary of the TSV-to-device coupling for the 28nm NMOS as a result of the device simulations, while table 3 does so for the 28 nm PMOS transistor. The percentage changes obtained using the simulation framework are similar to recent experimental results [8][9][10][17].

Table 2: Percentage changes in I_{on}, I_{off} and I_{lin} for a 28 nm NMOS transistor due to stress from a neighboring TSV

	ΔI_{on} (%)	**ΔI_{off} (%)**	**ΔI_{lin} (%)**
TSV at 0° w.r.t. the NMOS channel			
TSV at 0V	1.42	3.73	2.62
TSV at 1V	2.42	5.37	3.74
TSV at 45° w.r.t. the NMOS channel			
TSV at 0V	2.11	4.64	3.31
TSV at 1V	3.05	6.37	4.40
TSV at 90° w.r.t. the NMOS channel			
TSV at 0V	0.93	2.86	1.77
TSV at 1V	1.37	4.18	2.69

Table 3: Percentage changes in Ion, Ioff and Ilin for a 28 nm PMOS transistor due to stress from a neighboring TSV

	ΔI_{on} (%)	**ΔI_{off} (%)**	**ΔI_{lin} (%)**
TSV at 0° w.r.t. the PMOS channel			
TSV at 0V	1.76	5.28	3.34
TSV at 1V	1.24	3.51	2.35
TSV at 45° w.r.t. the PMOS channel			
TSV at 0V	2.96	8.41	5.71
TSV at 1V	2.42	6.26	4.68
TSV at 90° w.r.t. the PMOS channel			
TSV at 0V	2.00	5.81	3.82
TSV at 1V	1.46	4.05	3.01

Effect of TSV-induced Stress

To begin with, consider the effect of stress on the NMOS with the TSV at 0V (i.e. no electric field coupling). With the TSV at 0V, the change in I_{on} is found to be within 2% for all orientations of the TSV with respect to the transistor. This tallies with the observed increase (~150 MPa) in tensile strain at the center of the channel. The changes in I_{off} and I_{lin} are similar in nature. The effect of additional TSV induced strain is higher in the linear operating region of the NMOS, as a change in mobility has a greater impact on the linear

current than saturation current. The change in I_{off} is even higher and can be attributed to its exponential dependence on the threshold voltage. As mentioned previously, an increase in tensile strain results in a decrease in threshold voltage of an NMOS.

The change in current is highest when the TSV is diagonal with respect to the transistor, and least when the TSV is perpendicular to the transistor channel, which is in agreement with results obtained by West et al [10]. The difference in changes in NMOS current from when the TSV is at 0° to when it is at 90° can be explained using empirical non-local pseudopotential theory [20], which predicts a greater change in electron effective mass when uniaxial strain is applied along the <110> direction (same as the channel).

For the 28 nm PMOS transistor with the TSV at 1V, the results show a trend similar to those obtained for the NMOS. I_{off} changes the most (4-6%), I_{on} changes the least (1-2%), with changes in I_{lin} (3-4%) sandwiched in between the two. For the PMOS transistor, the TSV at 90° results in the largest change in current, because it causes the largest change in the hole effective mass for the same change in the stress.

Effect of TSV-induced Stress and TSV-transistor Electrical Coupling

The combined effect of TSV-induced stress and field coupling between the TSV and transistor can be easily understood from the results corresponding to the TSV at 1V for the NMOS (table 2), and the TSV at 0V for the PMOS (table 3).

For the NMOS transistor, when the TSV is at 1V, the field coupling results in a marginal increases in its body voltage. This in turn results in a higher change in current. The change in current due to TSV potential is clear from the difference between the changes in current when the TSV is at 0V and at 1V. This difference caused by the TSV potential is comparable to the difference caused by the additional stress introduced by the TSV.

A similar observation can be made for the PMOS device as well with the TSV at 0V. We assume that the TSV is placed inside the same n-well as the PMOS for this study.

From these results, we can see that electrical coupling between the TSV and transistor is as important as TSV-induced stress in the transistor channel.

Transistor Placed Inside a TSV Grid

A scenario worth studying via simulation is the effect of placing a transistor inside an array of TSVs arranged as a grid (figure 1). This scenario is important from the point of view of placing inverters or transistors comprising an inverter buffer chain in the spaces between power (or signal) TSVs, typically located next to each other, forming a grid.

To evaluate this scenario, four cases are simulated, two involving a transistor surrounded by 4 TSVs, each of which is diagonal to the transistor channel, and two more cases involving a transistor placed at the center of a square grid of 8 TSVs, four of them occupying the vertices of the square, and the other four lying on the mid-points of the four sides. In each case, change in current (on, off, and linear current) is computed with respect to the values obtained for the baseline 28 nm NMOS/PMOS transistor. The results are presented in Table 4.

Table 4: Changes in I_{on}, I_{off} and I_{lin} for a 28 nm NMOS/PMOS transistor surrounded by 4 and 8 TSV grids

	TSV Grid	ΔI_{on}	ΔI_{off}	ΔI_{lin}
NMOS	4 TSVs @ 0V	2.8%	7.11%	4.88%
	8 TSVs @ 0V	3.77%	8.82%	5.14%
PMOS	4 TSVs @ 1V	-2.24%	-6.93%	-4.14%
	8 TSVs @ 1V	-2.63%	-8.02%	-4.81%

Simulations were run assuming all TSVs in the grid to be at 0V for the NMOS and at 1V for the PMOS transistor. For the NMOS, the worst changes in on and off currents are ~ 4% and 9% respectively, which are not significantly different when compared to the changes caused due to the stress induced by a single TSV. The same can be observed for the PMOS, for which the worst on and off current changes are ~ 3% and 8% respectively.

The addition of 3 and 7 TSVs respectively to form 4- and 8-TSV grids results in the stresses caused by the TSVs to combine both constructively and destructively [9], so that their combined effect is less than the sum of the effects of individual TSVs. The result of this interaction is that the change in stress, and hence currents, is also lower than the sum of changes caused by the individual TSVs.

Effect of Distance Between TSV and Transistor

Simulations were performed to understand the effect of TSV-to-device distance for the 28 nm NMOS and PMOS transistors.

Figure 6 illustrates the effect of increasing the TSV-to-transistor distance from 2.5 µm to 4 µm for the NMOS, and figure 7 does the same for the PMOS. For both NMOS and PMOS, it is observed that the current changes less at both voltage levels of the TSV at the greater distance. This is expected as the stress decreases as the distance from the TSV increases, as does the field coupling.

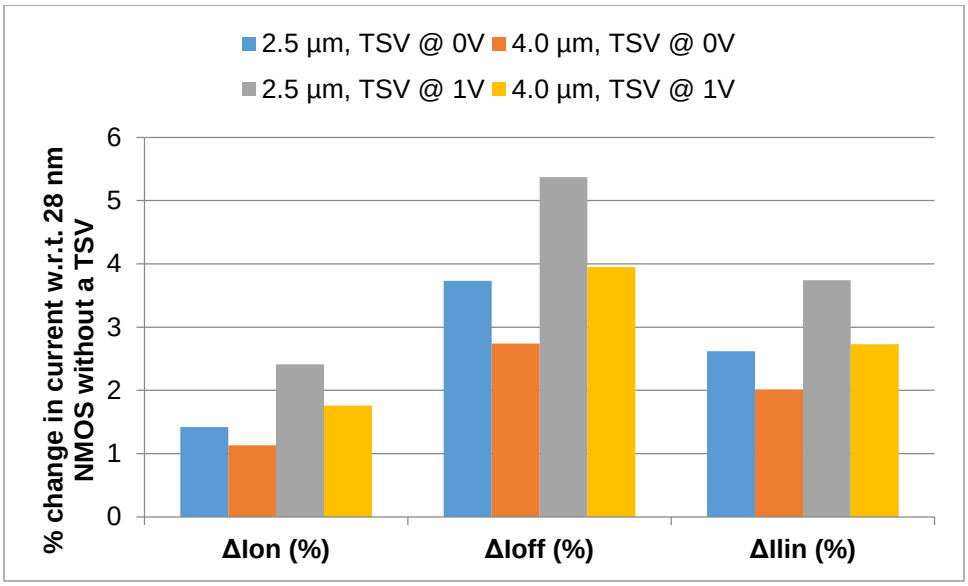

Figure 7: Changes in I_{on}, I_{off} and I_{lin} as a function of the TSV-to-device distance for a 28nm NMOS

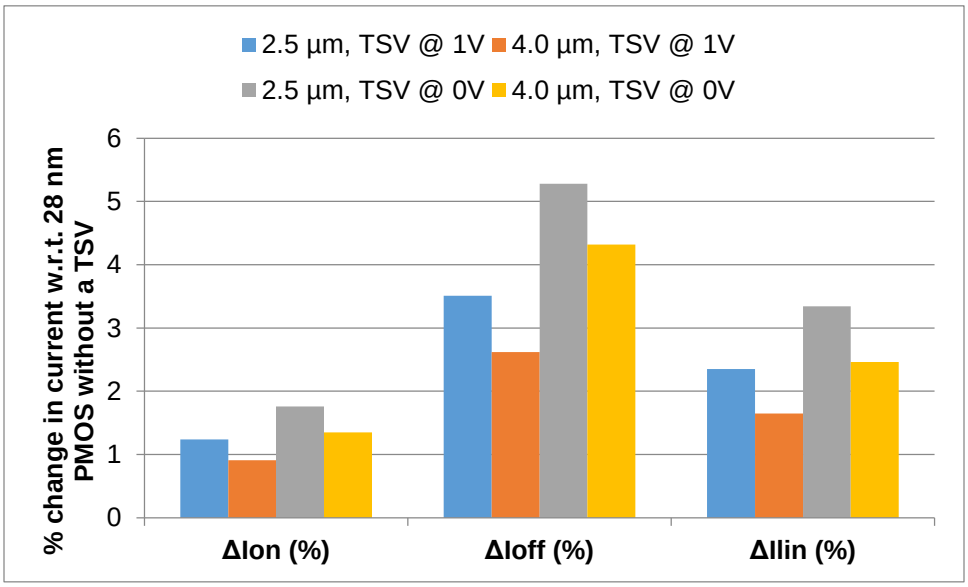

Figure 8: Changes in I_{on}, I_{off} and I_{lin} as a function of the TSV-to-device distance for a 28nm PMOS

Impact of TSV-to-Device Coupling at Various Technology Nodes

Simulations were performed to understand the effect of technology scaling on TSV-to-device coupling. 3D TCAD simulations are performed considering 40nm and 180nm NMOS/PMOS devices, and the results are compared with the 28nm device presented in the first section.

For all the simulations, the TSV diameter is kept constant at 5.5 µm, and the TSV-to-device distance is also kept constant at 2.5 µm. This helps in understanding the effect of scaling the transistor technology only, isolating it from scaling trends in TSVs, and the effect of changing the TSV-to-device distance, explored in the previous section with the 28 nm transistors.

Table 5: Characteristics of the 180 nm, 40 nm, and 28 nm NMOS and PMOS transistors obtained from TCAD simulations

	180 nm		**40 nm**		**28 nm**	
	NMOS	**PMOS**	**NMOS**	**PMOS**	**NMOS**	**PMOS**
I_{on} (µA/µm)	647.3	343.4	679.7	230.4	749.7	464.8
I_{off} (pA/µm)	16.3	16.9	118.6	118.3	2994	3008
I_{lin} (µA/µm)	90.3	41.9	85.2	29.4	123.9	76.9
Sub V_T Slope (mV/decade)	81	85	82	84	85	88

Table 5 shows the characteristics of the baseline 180 nm and 40 nm NMOS and PMOS, alongside the 28 nm devices. Changes in currents due to TSV-induced stress and TSV-device field coupling are calculated with respect to these transistors.

Figure 9 shows the changes in the I_{on}, I_{off} and I_{lin} for the 180 nm, 40 nm and 28 nm NMOS transistors with the TSV at 0°, 45° and 90°, at the TSV potential of 0V. The figure clearly

shows that the effect of current change caused by TSV-induced stress reduces appreciably with technology scaling. For instance, the 28nm device sees the maximum change in I_{on} reduced to 2%, compared to 4% for the 40nm device. The primary factor is the higher engineered stress in the channel of the 28 nm device due to the thickness and extent of the nitride layer used to introduce tensile strain or compressive stress. The doping concentration and profile, and the lower channel depth also contribute to the higher initial channel strain/stress. Since the device with the stress liner serves as the baseline for our calculations, and the TSV introduces the same stress in both the 28 nm and 40 nm transistors, this result makes sense. The effect of scaling is strongest in the change in I_{off}.

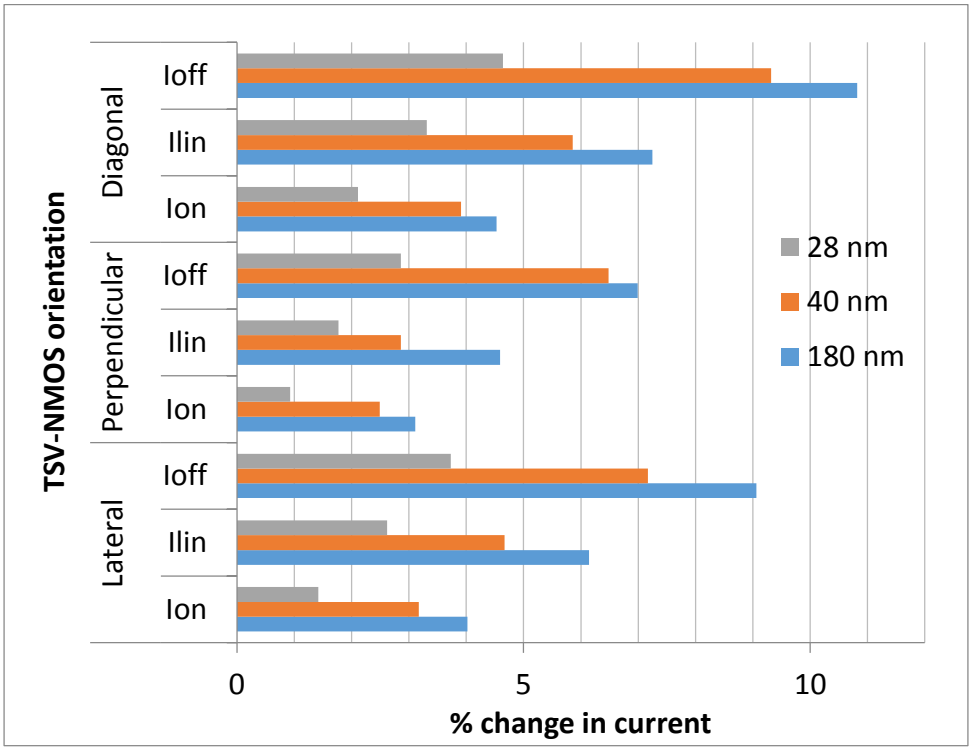

Figure 9: Effect of technology scaling on TSV-to-device coupling: NMOS with TSV at 0V

Figure 10 shows the effect of scaling including the field coupling, i.e. with the TSV at 1V for the NMOS. The generic trend of figure 8 is repeated here as well.

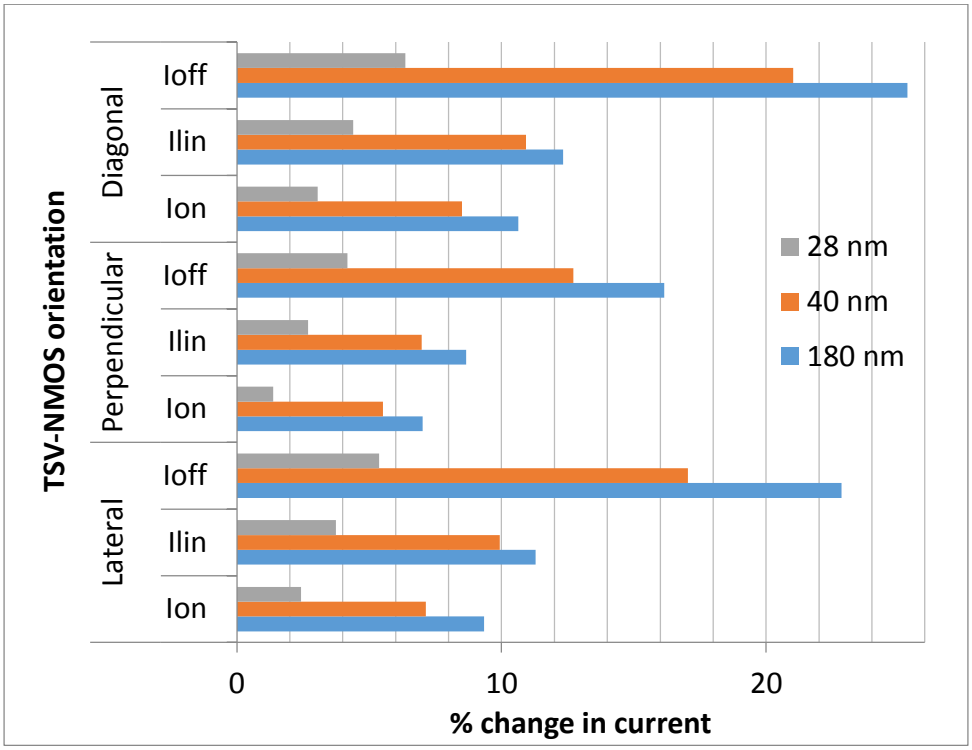

Figure 10: Effect of technology scaling on TSV-to-device coupling: NMOS with TSV at 1V

Figure 11 shows the effect of scaling on the additional changes in the current between TSV=1V and TSV=0V conditions, i.e. the changes due to the field coupling. The results point to the trend that the effect of field coupling also reduces with technology scaling. This can be attributed to the fact that the electric field inside the transistor channel (gate induced vertical field and source/drain induced lateral field) is higher at scaled technologies. Hence, perturbation due to additional TSV induced electric field is much smaller.

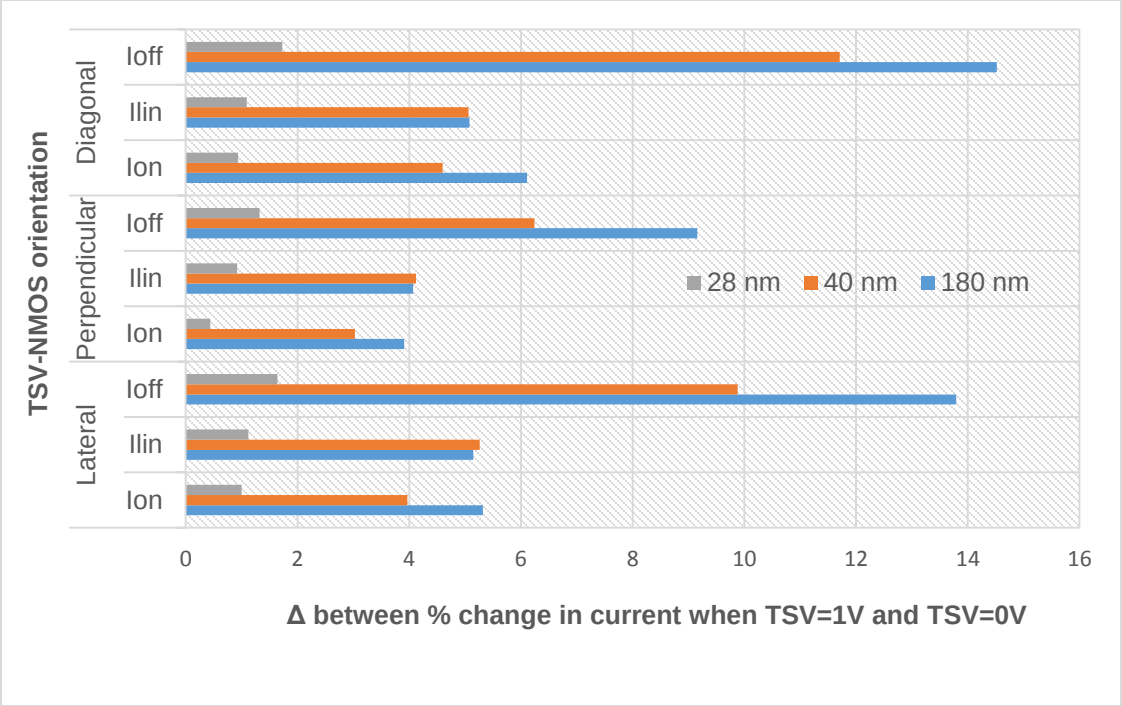

Figure 11: The difference in percentage change in current for NMOS transistors between TSV at 1V and TSV at 0V

Figures 12 and 13 illustrate the effect of scaling on TSV-to-PMOS coupling for all three orientations, as before. As with the NMOS, the changes in I_{on}, I_{off} and I_{lin} reduce with scaling for PMOS transistors too. Further, as in the case of the NMOS, the difference between the changes when the TSV is at 0V and when the TSV is at 1V reduces as well.

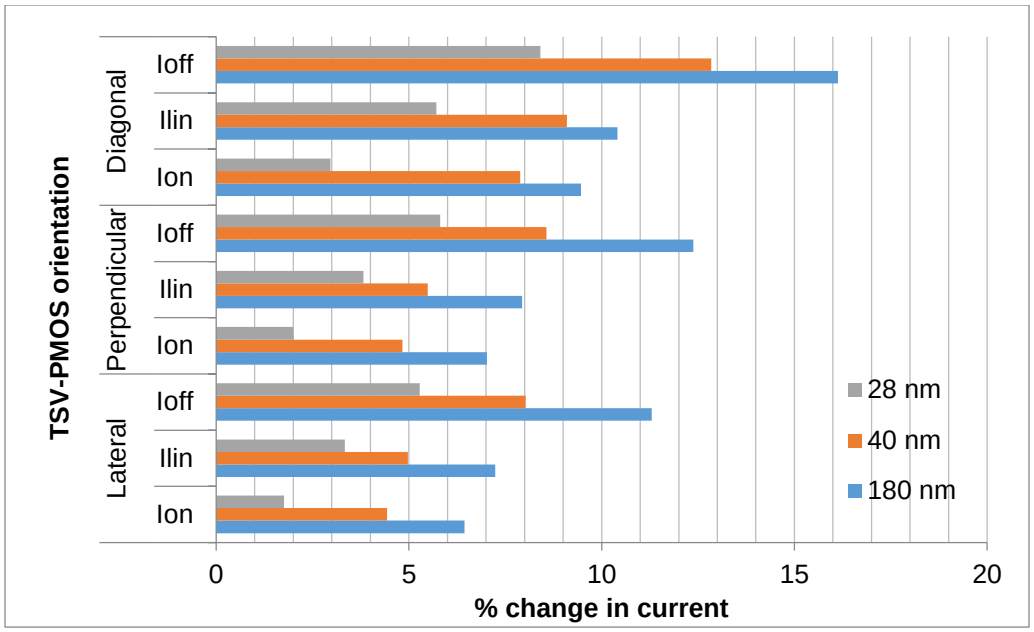

Figure 12: Effect of technology scaling on TSV-to-device coupling: PMOS with TSV at 0V

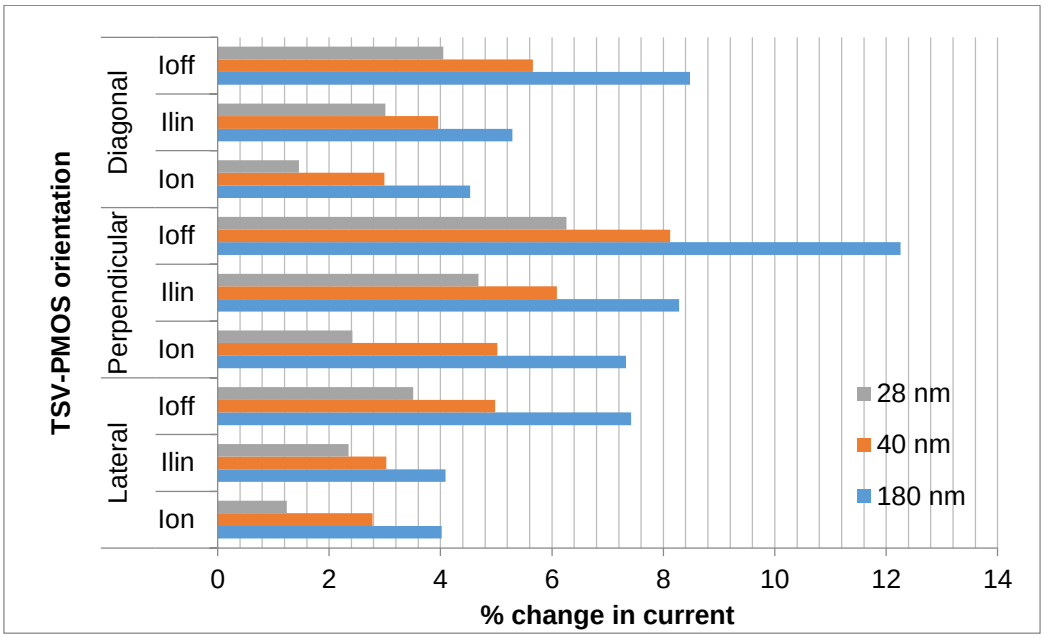

Figure 13: Effect of technology scaling on TSV-to-device coupling: PMOS with TSV at 1V

CONCLUSION AND FUTURE WORK

This work studies the effect of mechanical stress and electrical field coupling between through-silicon vias (TSVs) and bulk-CMOS devices through 3D TCAD process-device co-simulation. TSVs introduce additional tensile strain in the transistor channel (at normal operating temperatures). However, the magnitude of the induced strain is much smaller compared to the strain (stress) engineered using tensile (compressive) nitride liner (or other strain/stress engineering techniques) used to improve NMOS (PMOS) performance in nanometer technologies. Likewise the TSV induced electric field also modifies the electrostatics inside the transistor channel and modifies its electrical characteristics. However, the TSV induced field is much smaller than the internal electric field in the channel, particularly in the nanometer technologies. Hence, both TSV-to-device coupling mechanisms have only a marginal impact on the electrical characteristics of neighboring transistors in scaled technologies. The analysis suggests that at current and future technology nodes, the keep-out zone (KOZ) can be defined more aggressively, so that transistors may be placed closer to TSVs, and also inside a TSV grid, which would help reduce circuit/system footprint, and thus reduce cost by increasing the efficiency of silicon utilization.

While this work studies TSV-device coupling for bulk-CMOS transistors, a similar study and analysis can be performed for alternative transistor technologies, including FinFET, FDSOI, and PDSOI transistors. For instance, in case of FinFETs, the effect of stress alone would be interesting, given that stress and its impact on mobility in FinFETs is a function of many factors [21], including fin length, fin pitch, number of fins, size of STI, method of stress engineering, and distribution of stress along the fin. These factors will decide how much of an impact the TSV-induced stress has on transistor performance. Some of these

factors, such as fin pitch, also have an effect on parasitics and AC performance [21], so the effect of electrical coupling between TSV and transistor would also be interesting to study. It would also be interesting to determine the extent of electrical coupling given that a double- or tri-gate transistor allows for stronger control by the gate on transistor performance.

Further, this study could be extended to understand the impact of TSV-device interaction on circuits like inverters, logic gates, and ring oscillators. For instance, tensile strain improves mobility of n-type devices, and degrades mobility of p-type devices, and depending on how large the changes are, the p-to-n mobility ratio may change significantly. This would need to be taken in account when sizing transistors in an inverter or logic gate to ensure that the circuit performs as expected.

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