CMOS INDUCTIVELY COUPLED POWER RECEIVER FOR

WIRELESS MICROSENSORS

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Presented to
The Academic Faculty

by

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CMOS INDUCTIVELY COUPLED POWER RECEIVER FOR
WIRELESS MICROSENSORS

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To my family
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Modern-day wireless microsystems (WMS) include an assortment of sensors, transceivers, analog and digital signal processors, memory, and many additional components to facilitate the advanced functional requirements of wireless sensor networks (WSN) and biomedical implants. All of this functionality comes at the cost of increased power consumption. The microscale dimensions of these systems limit the energy capacity of miniaturized energy reservoirs, such as thin-film Li-ions and super capacitors. The combination of reduced internal energy and increased power consumption limit operational lifetimes for WMS. Harvesting energy from thermal gradients, vibrations, light, and/or radiation is appealing, but not yet a reality for many applications, because miniaturized state-of-the-art transducers do not generate sufficient power. Wireless power transfer (WPT) via inductive coupling can supply the additional power required to extend the operational lifetimes of WMS. WPT can also recharge the battery of a WMS, so that the system can continue to operate between interrogations (i.e., recharge cycles). Unfortunately, the WMS’s volumetric constraints limit the size of the receiving coil, which results in a loosely coupled link that induces a low electromotive force (EMF). With low EMF voltages, power extraction from the induced coil voltage amounts to low-threshold rectification, or equivalently low AC voltage to DC voltage conversion.

The purpose of this research is to investigate how to transfer power wirelessly using a loosely-coupled inductive link and to develop, design, simulate, build, test, and evaluate CMOS charger integrated circuits (IC) that wirelessly charge the battery of a
microsystem. A fundamental challenge here is that small receiver coils only produce millivolts of AC voltage, which is difficult to convert into DC form. Although LC-boosted diode-bridge rectifiers in the literature today extract energy from similar AC sources, they can only do so with the addition of a precisely tuned off-chip resonant capacitor, which counters the aim of integration. Therefore, rather than rectify the AC voltage, this research rectified the current that the AC voltage induces in the coil. This way, the system can still draw power from voltages that fall below the inherent threshold limit of diode-bridge rectifiers. Still, output power was low because, with these low currents, small coils can only extract a diminutive fraction of the magnetic energy available, which is why investing battery energy into the coil to build larger coil currents generated higher output power. Lastly, as this current-mode rectification scheme was implemented using a switching converter, a novel self-synchronization method was developed that automatically synchronizes the switching frequency of the converter to the incoming EMF signal for autonomy.

This dissertation begins with background motivation and fundamentals of inductively coupled power transfer and then proceeds by discussing the findings of this research. Specifically, Chapter 1 reviews state-of-the-art wireless microsystems within the context of power requirements and discusses the energy and power sources available for powering them. Chapter 2 provides background in wireless power transfer and details electromagnetic induction and inductively coupled power transfer with discussion on receiver coil miniaturization. Chapter 3 surveys and compares low-voltage rectifiers, which can be grouped into resonant receivers, voltage multipliers, and inductive rectifiers. Chapter 4 introduces a novel inductive rectifier that reduces the input-referred
threshold of inductive rectifiers to unprecedented values and details the design and the experimental results of the IC prototype. Chapter 5 explores the requirements for the higher power transfer, which motivates the introduction of a novel energy-investment receiver and concludes with experimental validation of an IC prototype. Chapter 6 details a novel self-synchronization scheme that records the incoming EMF frequency and adaptively adjusts the receivers switching frequency for synchronization and concludes with the experimental results of an IC prototype. Finally, Chapter 7 summarizes the findings of this research by highlighting the contributions of this work, the technical limitations of this work, and future research directions.
CHAPTER 1

POWERING MICROSYSTEMS

1.1 Applications

Advances in microfabrication techniques have enabled the miniaturization of microelectronics and have made it possible to integrate more electronic functionality onto a single integrated circuit (IC). With the advent of microelectromechanical systems (MEMS), ICs can be packaged together with numerous MEMS sensors and/or actuators to form an ultra-compact, all-inclusive wireless microsystem (WMS). The small size of WMSs allows them to be unobtrusive, often a requirement for biomedical implants [1, 2], and economical, which motivates their use in industrial, smart home, agricultural, and environmental monitoring applications [3, 4].

WMS have already been employed in many biomedical applications, including implantable biosensors, as shown in Figure 1.1, that continuously monitor blood glucose and intraocular pressure to improve treatment regiments of diabetes and glaucoma patients, respectively [5-8]. Biosensors have also been used in detecting bio-molecules (e.g., nucleotides and proteins) in point-of-care diagnostic devices [9-11]. In another example, a patient’s vitals can also be examined by allowing them to wear a body sensor network (BSN) that records electrocardiograms (ECG) [12-14] and by using implanted blood pressure monitors [15]. Muscle and neural tissue stimulators are yet another WMS, which have been used for acupuncture, cochlear prosthesis, retinal implants, and deep-brain stimulation in managing Parkinson’s disease and epilepsy [16-18]. Furthermore, wireless miniaturized drug delivery systems have been used to release higher-concentration doses of a drug at a local target site and therefore avoid the negative side effects of systemic medication [19-21]. To name one more biomedical application,
Wireless endoscopes (or capsule endoscopes) have been used to examine areas of the small intestines that cannot be reached with conventional types of endoscopy [22].

![Figure 1.1. Implantable continuous intraocular pressure monitor for managing glaucoma [5] © 2011 IEEE.](image)

Other than biomedical applications, WMS are also becoming widespread in industrial applications. Examples of which, include structural health monitoring for aircrafts [23, 24], space satellites [25], concrete bridges [26], and automobile tires [27, 28]. Additional examples include wireless sensor networks (WSN), where distributed sensor nodes can monitor environmental conditions like pressure, temperature, and humidity for air/water quality monitoring and natural disaster prevention [29-31]. In more futuristic applications, researchers have utilized the compact nature of WMS for the development of the microrobots used in swarm robotics (as shown in Figure 1.2) [32] and wireless motion control of cyborg hawk moths [33]. The wireless nature of these WMS, which allows them to be so useful, also imposes the challenge of how to power them. However, before considering different powering methods, an examination of power requirements...
for various WMS is necessary and will guide in the selection of an appropriate powering method.

Figure 1.2. Autonomous mm³-sized microrobot used in swarm robotics [32] © 2011 IEEE.

1.2 Power Requirements

1.2.1 Inside a Microsystem

For a better understanding of the power requirements, a look at the power-consuming circuit blocks within a typical WMS proves insightful. As such, Figure 1.3 displays an example. Here, ambient information is sensed with any of the micro-scale sensors and is sent via the sensor interface to the digital microprocessor. The analog front-end begins by amplifying the low-level outputs of the sensor (e.g., capacitive changes in an accelerometer) with a low noise amplifier (LNA); the LNA commonly employs auto-zeroing and chopper stabilization to reduce offset and flicker noise [34]. Next, the amplified signal is digitized with an analog to digital converter (ADC) that commonly uses successive approximation (SAR) techniques for their superior energy per conversion-step [35, 36]. While there have been many circuit design advances in low-power sensor front-end LNAs [13, 37, 38] and ADCs [39, 40] the power savings of the sensor interface block is limited by the bandwidth and signal-to-noise ratio (SNR) requirements for the given application. As such, the power consumption of the sensor interface is mostly dictated by the system requirements specific to an application [41].
Within the digital block, sensor data is typically pre-processed, compressed, and sent to random-access memory (RAM) for storage. The digital block employs numerous power conserving techniques including: dynamic voltage scaling (DVS) to minimize energy consumption for a given timing requirement, clock gating to reduce dynamic power, and multiple threshold CMOS (also referred to as footer/header power gating) to reduce leakage power when in deep-sleep mode [14, 41, 42]. Furthermore, as the microprocessor frequently executes similar application specific tasks (e.g., fast Fourier transform (FFT), digital filtering, encryption, data encoding/decoding), those tasks can be delegated to specialized hardware modules that consume less power than a general reduced instruction set computing (RISC) architecture [43].

With regard to the transceiver, it wirelessly transmits the encoded data from the digital block to a base station that listens to and archives the data. The transceiver also receives data, which is typically used to acknowledge sent data, but can also be used to update firmware [32] or prompt an asynchronous sensing/actuation event [21]. Without power-conscious design of the transceiver, it can easily dominate the WMS’s power budget [41, 44]. Conventional far-field or radio frequency (RF) communication is power intensive [45], which is why other less power-costly methods, such as optical, near-field (or backscattering), infrared, and even sound are sometimes used [3, 32, 41, 46, 47]. The alternatives, however, either require line of sight communication or have a more limited
communication range. As such, techniques to reduce power consumption of the RF transceiver have been investigated; namely, the use of ultrawideband (UWB) transmitters for RF communication has proven energy efficient because they do not require a power-costly high precision local oscillator [48, 49]. Ultimately, for RF communications, reducing the maximum transmission distance gives the largest power savings, as it substantially reduces the required radiated (or transmitted) power [4]. Regardless of the communication method, the most straightforward approach to reduce transceiver power losses is to transmit less data, which is why raw sensor data input to the digital block is usually filtered, pre-processed, and compressed prior to transmission. Another commonly used system-level technique includes disabling the transceiver (often referred to as sleep or deep-sleep mode) for prolonged periods until required to transmit. The percentage of time that the transceiver, or more generally, the complete microsystem is enabled is referred to as the duty-cycle. While some applications allow for an ultra-low duty-cycle (e.g., a slow-varying measurand like a tire-pressure reading [28]), others require more continuous monitoring and more frequent transmission (e.g., a neural stimulator [17]) that increase the duty-cycle to consume more power.

1.2.2 Average Power Consumption

Table 1.1 illustrates the average power requirements for the numerous applications discussed in the last subsection. As can be seen from Table 1.1, WMS consume a wide range of power levels (5.3 nW – 300 mW) depending on the application in question. The variations in power consumption arise from different applications necessitating different system requirements, as some functions are more power-intensive than others. That is to say, that even with the power saving of the numerous power-conscious techniques previously discussed, the system requirements for an application ultimately defines the WMS’s power requirement and WMSs with higher functionality or more stringent system requirements consume the most power.
<table>
<thead>
<tr>
<th>Application</th>
<th>Average Power Consumption</th>
<th>Size</th>
<th>Author</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Environmental Monitoring</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Humidity Sensor</td>
<td>1.38 mW</td>
<td>16 × 16 mm²</td>
<td>Cirmirakis</td>
<td>[29]</td>
</tr>
<tr>
<td>Pressure, Temperature, and</td>
<td>341 μW</td>
<td>32 mm³</td>
<td>DeHennis</td>
<td>[30]</td>
</tr>
<tr>
<td>Humidity Sensor Suite</td>
<td>48.6 μW</td>
<td>0.5 cm³</td>
<td>Lemmerhirt</td>
<td>[31]</td>
</tr>
<tr>
<td><strong>Microrobots</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Swarm Microrobotics</td>
<td>692 μW</td>
<td>3 × 3 × 3 mm³</td>
<td>Casanova</td>
<td>[32]</td>
</tr>
<tr>
<td>Cyborg Moth</td>
<td>2.5 mW</td>
<td>15 × 26 × 0.025 mm³</td>
<td>Daly</td>
<td>[33]</td>
</tr>
<tr>
<td><strong>Structural Health Monitoring</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Aircraft Fuselage</td>
<td>2.9 mW</td>
<td>80 × 35 mm²</td>
<td>Becker</td>
<td>[24]</td>
</tr>
<tr>
<td>Aircraft Propeller</td>
<td>120 mW</td>
<td>63 × 32 × 8 mm³</td>
<td>Escriba</td>
<td>[23]</td>
</tr>
<tr>
<td>Space Satellite</td>
<td>5.3 mW</td>
<td>2 mm²</td>
<td>Shamim</td>
<td>[25]</td>
</tr>
<tr>
<td>Tire Pressure</td>
<td>4 μW</td>
<td>1 cm³</td>
<td>Flatscher</td>
<td>[28]</td>
</tr>
<tr>
<td><strong>Patient Vital Monitoring</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Blood Pressure Monitor</td>
<td>300 μW</td>
<td>12.6 × 3.2 × 3.2 mm³</td>
<td>Cong</td>
<td>[15]</td>
</tr>
<tr>
<td>Electrocardiogram (ECG or EKG)</td>
<td>12 μW</td>
<td>25 × 68 mm²</td>
<td>Yoo</td>
<td>[12]</td>
</tr>
<tr>
<td></td>
<td>60 μW</td>
<td>4 mm × 1.5 mm²</td>
<td>Yazicioglu</td>
<td>[13]</td>
</tr>
<tr>
<td><strong>Disease Management</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Glucose Sensor</td>
<td>286 μW</td>
<td>4 × 8 × 1 mm³</td>
<td>Ahmadi</td>
<td>[8]</td>
</tr>
<tr>
<td>Intraocular Pressure Monitor</td>
<td>240 nW</td>
<td>8.75mm³</td>
<td>Chen</td>
<td>[6]</td>
</tr>
<tr>
<td>(Tonometer)</td>
<td>5.3 nW</td>
<td>1.5 mm³</td>
<td>Chen</td>
<td>[5]</td>
</tr>
<tr>
<td>Implant Delivery</td>
<td>7.2 mW</td>
<td>32 mm³</td>
<td>Yang</td>
<td>[20]</td>
</tr>
<tr>
<td></td>
<td>370 μW</td>
<td>5 × 5 × 5 mm³</td>
<td>Smith</td>
<td>[19]</td>
</tr>
<tr>
<td><strong>Bio-molecule Detectors</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Point-of-care (PoC) Diagnostics</td>
<td>165 mW</td>
<td>2.1 × 1.4 mm³</td>
<td>Wang</td>
<td>[9]</td>
</tr>
<tr>
<td></td>
<td>300 mW</td>
<td>0.6 mm²</td>
<td>Gambini</td>
<td>[10]</td>
</tr>
<tr>
<td></td>
<td>2.3 mW</td>
<td>2.54 × 7.62 × 1 mm³</td>
<td>Singh</td>
<td>[11]</td>
</tr>
<tr>
<td><strong>Muscle and Neural Tissue</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Stimulation</td>
<td>8.25 mW</td>
<td>4.5 × 4.5 mm²</td>
<td>Ghovanloo</td>
<td>[18]</td>
</tr>
<tr>
<td>Acupuncture</td>
<td>6.8 mW</td>
<td>12.5 mm²</td>
<td>Song</td>
<td>[16]</td>
</tr>
<tr>
<td>Pacemaker</td>
<td>8 μW</td>
<td>35 × 35 mm²</td>
<td>Wong</td>
<td>[2]</td>
</tr>
</tbody>
</table>
1.2.3 Profile of Power Consumption

As mentioned previously, duty-cycling provides substantial energy savings, however, enabling and disabling power to the system also induces a large peak-to-average power consumption profile. To illustrate the large peak-to-average ratio (PAR), data from [14] was used to reproduce an example power profile, as shown in Figure 1.4. In the example shown, power consumption peaks during a transmission event. For the remainder of the time the microsystem senses and records ECG signals, while the transmitter is in a deep-sleep mode to conserve power. This kind of power profile requires an energy source that can both provide high instantaneous power (during data transmission) and still have a large enough energy reservoir to supply the device throughout its lifetime. As described in the next section, both power density and energy density trade-off with one another for various powering methods.

![Figure 1.4. Example of the instantaneous power consumption of a wireless microsystem (values reported in [14]).](image)

1.3 Power and Energy Sources

Numerous energy and power sources have been employed to supply microsystems throughout the literature [50]. The Ragone plot, shown in Figure 1.5, displays how power and energy density trade-off between the common sources [51]. Here, power sources refer to sources that have relatively high power densities and low energy densities. Conversely, energy sources have relatively high energy densities, but low power
densities. Power sources have been traditionally used to supply devices with high peak power requirements that otherwise could not be supplied by the low-power energy sources. However, energy sources are preferred because they have a larger energy capacity that can prolong the operational lifetime of the microsystem, as highlighted by contours of constant lifetime in the Ragone plot (represented by dashed lines). However, energy sources can only be used when the peak power requirement is low enough for the energy source to supply it. As discussed in the previous section, Microsystems can have a high peak-to-average power ratio that would require a power source to supply the high peak power requirement. Instead, hybrid solutions incorporate a power source to deliver the high power transients required of the load and an energy source to deliver the average power requirements. This way, the hybrid source has the drive of a power source with the energy capacity of an energy source to yield the best lifetime for the microsystem.

Figure 1.5. Volumetric Ragone plot for various energy and power sources, with the dashed lines representing contours of constant lifetime (plot constructed using method from [51] and using values reported in [52-55]).
1.3.1 Electrochemical Batteries

Electrochemical batteries are the most commercially used power sources for small mobile electronics. Of these, lithium-ion (Li-ion) batteries are the most predominant due to their superior power density (1000-4000 W/kg) and energy density (60-240 Wh/kg) [52]. Additionally, they are rechargeable with a respectable number of recharge cycles (1000-3000) and have low self-discharge rates of 5% per month [52, 56]. Furthermore, all-solid-state thin-film Li-ion technology facilitates their integration into microsystems with a film thickness of only 10 – 15 μm and active areas less than 25 cm² to yield capacities of 0.1 to 5 mAh [57-59]. With a power density sufficient to deliver the peak power requirements of most microsystems, thin-film Li-ions are good candidates for powering them. However, given their relatively lower energy densities, they cannot sustain powering the microsystems for very long. As an example, given the average power requirement of 19 μW (as in Figure 1.4) and a 5 mAh capacity thin-film Li-ion, the lifetime of the device is about 35 days. The Li-ion battery additionally has the disadvantage of requiring specialized charging circuitry, to avoid under and over charging the cell [60]; the former of which can dramatically reduce the capacity of the battery (9% reduction in capacity from a 1.2% undercharge), while the later can lead to thermal runaway and venting [56, 61]. It is also worth mentioning that non-rechargeable batteries have also been used to power microsystems. Most notably, Zinc-Air batteries have been used in hearing aids because of their very low self-discharge rate of 0.5% per month and high energy density of 300 – 500 Wh/kg, which arises from using oxygen in the air for its cathodic half reaction [52, 56].

1.3.2 Supercapacitors

Supercapacitors are yet another useful power source that distinguishes themselves from traditional dielectric or electrolytic capacitors by their much higher capacitance of 35 – 1300 F/cm³ [52]. The higher capacitance allows the supercapacitor to have energy
densities that are $100 - 1000\times$ larger than electrolytic capacitors, but still $10 - 100\times$ smaller than a Li-ion [52, 62]. Combined with $10\times$ more power density than the Li-ion, but a tenth of that of electrolytic capacitors, they fit in-between the Li-ion and conventional capacitors in the Ragone plot [51]. An appealing aspect of the supercapacitor is its cycle life, with some supercapacitors boasting 500,000 to 1,000,000 recharge cycles [52]. Furthermore, supercapacitors have the additional benefit of rapid recharge times of 1 – 10 seconds compared to the 15 minutes to 2 hours for rechargeable electrochemical batteries [52]. Also, thin-film micro-supercapacitors technology facilitates integration into microsystems [63, 64]. Unfortunately, their high self-discharge rate of 38 – 50% per month limits lifetime to a few months. As a result of both the high self-discharge rate and the relatively low energy density, the lifetime of these devices are quite limited and therefore require a frequent resupply of energy. As such, these devices are commonly used in tandem with energy sources such as energy harvesters [65, 66].

### 1.3.3 Fuel Cells

Fuel cells fall into the category of energy sources and are appealing as they offer higher specific energy densities than that of Li-ions. Although fuel cells convert chemical energy into electrical energy just as conventional electrochemical batteries do, they instead use gaseous or liquid reactants that store significantly higher chemical energy compared to the solid reactants found in electrochemical batteries. Unlike some electrochemical batteries, fuel cells are not recharged, but are refueled for a rough maximum of 3000 times [53]. Of the various fuel cell technologies, direct methanol fuel cells (DMFCs) are the most preferred for microscale applications as they offer both an operating range that includes ambient temperature and a reduction in peripheral components (balance-of-plant components: fuel reformers, heaters, pumps, and humidifiers) that allow for miniaturization [55]. While DMFCs have a theoretical specific density of 6088 Wh/kg, conversion efficiency and scaling limit the specific density in
current state-of-the-art microscale designs to 805 Wh/kg [52]. However, this density is still about 5 times greater than Li-ion technology. Because DMFCs have lower power density and a slower transient response than batteries, they are often used in tandem with Li-ions or supercapacitors, where the power sources provide the high-frequency peak power demanded by the load and the fuel cell provides the low-frequency average power [67].

1.3.4 Nuclear Batteries

With an even larger improvement in energy density over Li-ions, nuclear batteries have been employed in applications where lifetime is of upmost importance and volume is extremely restricted, such as space travel [68]. Of the various nuclear batteries, betavoltaics are the most commonly used for microscale applications as they can be fabricated using silicon-based microfabrication techniques [54]. Betavoltaics convert the high kinetic energy of beta particles ejected from decaying radioactive isotopes, such as tritium $^3$H, promethium-147 $^{147}$Pr, and nickel-63 $^{63}$Ni (as shown in Figure 1.5), into electrical energy. The lifetime of nuclear batteries corresponds to the half-life of their radioactive isotopes, which are generally quite long. Of these radioactive isotopes, $^{63}$Ni has the longest half-life of 100.3 years, while $^3$H and $^{147}$Pr have shorter half-lives of 12.4 and 2.6 years, respectively. However, with regard to power density, $^{147}$Pr has the highest power density (5 μW/mm$^3$), followed by $^3$H (20 nW/mm$^3$), and finally by $^{63}$Ni (0.5 nW/mm$^3$) [54]. As these power densities are low to begin with, power-conditioning circuits that employ maximum-power-point tracking (MPPT) are required to extract all of the available power from the betavoltaic cells. A major deterrent in using nuclear batteries in microsystems is their prohibitively high cost [69]. Finally, it is worth noting, that $^{147}$Pr, which has by far the greatest energy density of the above-mentioned radioactive isotopes (as visible in Figure 1.5), is unavailable for purchase in the United States [70].
1.3.5 Energy Harvesters

Energy harvesters convert available energy from the environment in the form of light [5, 71], motion [72-77], RF radiation [78-80] and heat [58, 81] into electrical energy. Because their energy reservoir is not confined by the miniature dimensions of microsystems, but instead encompasses their ambient surroundings, their energy capacity can be considered quasi-infinite [82]. However, the ambient energy sources do have limited available power, which depend on the ambient energy source and the transduction mechanism (summarized in Table 1.2). To highlight differences between the energy-constrained sources and energy harvesters, Figure 1.6 shows a retrofitted Ragone plot with the addition of energy harvesters (top axis). The plot suggests that if the average power requirement of a microsystem is less than that available from an ambient energy source, then energy harvesting has the potential to supply all the required energy to the microsystem and extend its lifetime indefinitely (sometimes referred to as “perpetual” in the literature) [6].

<table>
<thead>
<tr>
<th>Energy Source</th>
<th>Transduction Mechanism</th>
<th>Estimated Power† (in 1 cm³ or 1 cm²)</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Light</td>
<td>Photovoltaic Effect</td>
<td>Outdoor: 150 μW - 10 mW</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Indoor: &lt;10 μW</td>
<td></td>
</tr>
<tr>
<td>Kinetic</td>
<td>Electrostatic</td>
<td>1 - 400 μW</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Electromagnetic</td>
<td>1 - 100 μW</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Piezoelectric</td>
<td>1 - 100 μW</td>
<td></td>
</tr>
<tr>
<td>RF Radiation</td>
<td>Antenna</td>
<td>0.01 - 0.1 μW (25 - 100 m from GSM station)</td>
<td></td>
</tr>
<tr>
<td>Heat</td>
<td>Seebeck Effect</td>
<td>15 μW (10 °C gradient)</td>
<td></td>
</tr>
</tbody>
</table>

†Estimated power values reported in [83]
Selection of an energy harvester to support a microsystem is not solely dependent on power density, but also depends on whether the application allows access to a particular environmental stimulus (e.g., outdoor light has the highest power density, but is inaccessible for biomedical implants). Furthermore, even if the microsystem has access to an ambient energy source, availability of incoming power from that source may be sporadic (e.g., vibrations of a bridge). As such, energy harvesters are usually accompanied with an energy buffer in the form of a Li-ion battery or a supercapacitor to supply power during an energy drought and as a means of delivering the high peak powers characteristic of microsystems. Finally, microscale integration has proven feasible for light, heat, RF radiation, and kinetic energy harvesters [84], although
electromagnetic transduction does not scale nearly as favorably as piezoelectric and electrostatic transduction for kinetic or vibration energy harvesters [85].

1.3.6 Wireless Power Transmission

In an inductively coupled system, as shown in Figure 1.7, an externally located wireless power transmitter generates a time-varying magnetic field from which an in-package wireless power receiver harnesses energy. In a similar fashion to an energy harvester, the energy reservoir is not confined by the microsystem, but is instead confined by the power transmitter’s housing, which can be made much larger as it does not need to adhere to the strict volumetric requirements of a microsystem. The idea is to shift the energy capacity from the on-board energy source to a much larger externally located battery in an effort to extend lifetime of the microsystem. Furthermore, as the intensity of the magnetic field located at the wireless power receiver dictates the available power, the wireless power transmitter may increase or decrease its externally generated magnetic field to fulfill the power requirements of the microsystem. For reference, power densities up to 8.3 W/cm$^3$ have been reported in the literature [86].

![Figure 1.7. Wireless power transfer used to power a microsensor and recharge its on-board battery.](image)

The near-field electromagnetic link established between the receiver and transmitter can also sustain data transmission via near-field communication (i.e., backscattering) [87]. Not only can the link energize the microsystem, but it can also
recharge its battery during data transmission so that the system can continue to operate between communications [88-90]. As an example, Figure 1.7 shows a potential application of how a microsensor on a carton of milk can track and report temperature history collected during transport and storage to ensure that a cashier does not sell spoiled milk. Other applications include direct powering of biomedical implants, where the wireless power transmitter sits just outside the body [91-93]. The main disadvantage of inductively coupled power is the requirement that the wireless power transmitter be near the microsystem, which means that wireless powering is inappropriate in remote applications where near-field communication is unlikely. Furthermore, microscale magnetic transducers or pickup coils induce small voltages, which create challenges for power extraction.

1.3.7 Comparison

Table 1.3 summarizes the various energy and power sources with regard to peak power capability, peak energy storage, self-discharge rate, recharge time, cycle life, and remarks for each of the sources. To showcase how energy and power sources are used in real microsystems, Figure 1.8 displays a Ragone plot appended with how microsystems (shown as Δ and found in Table 1.1) might be powered. Each microsystem is plotted with an average power density (i.e., equal allocation of on-board source or battery to the remainder of the microsystem) and is assumed to be powered by the highest energy dense on-board source that can support its average power consumption. As can be seen from the figure, ultra-low average power microsystems ([5, 6, 15, 19, 31, 33]) can be powered by nuclear batteries to find long lifetimes from a couple of years to greater than a quarter century. However, the higher average power microsystems ([8, 11, 23, 30, 32]) cannot be powered by nuclear batteries, but instead must use Zinc-Air as an energy source, which cannot sustain powering the microsystems for very long (11.8 hours – 7.8 days). For applications that have access to ambient energy, energy harvester may be used to increase
lifetime semi-indefinitely (or at least until device or transducer failure). However, without the use of outdoor sunlight, energy harvesters can only support three of the microsystems. To support the higher average power microsystems for longer than the week that Zinc-Air can sustain, solar energy harvesting or wireless power transfer must be employed. This work is directed to applications that necessitate the higher average power delivered by inductive coupling.

**Table 1.3 Comparison of energy and power sources for microsystems.**

<table>
<thead>
<tr>
<th>Source</th>
<th>Peak Power Density</th>
<th>Peak Energy Density</th>
<th>Self-discharge Half Life</th>
<th>Cycle Life</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Supercapacitor</strong></td>
<td>14.6 - 86 mW/mm³</td>
<td>0.15 - 68 mJ/mm³</td>
<td>30 - 40 Days</td>
<td>&gt;1,000,000</td>
<td>● Ultra-fast recharging (1 – 10 sec)</td>
</tr>
<tr>
<td><strong>Li-Ion</strong></td>
<td>2.0 - 10 mW/mm³</td>
<td>0.43 - 2.3 J/mm³</td>
<td>0.55 - 1.9 Years</td>
<td>1,000 - 3,000</td>
<td>● Slow recharging (10 – 60 min)</td>
</tr>
<tr>
<td><strong>Zinc-Air</strong></td>
<td>0.8 - 1.5 mW/mm³</td>
<td>4.6 - 5 J/mm³</td>
<td>11.5 - 13.5 Years</td>
<td>Non-rechargeable</td>
<td>● Requires access to Air</td>
</tr>
<tr>
<td><strong>Micro-Fuel Cell</strong></td>
<td>4.6 - 66.8 μW/mm³</td>
<td>2.7 - 4.1 J/mm³</td>
<td>Limited by Methanol Crossover</td>
<td>3,000 refuelings</td>
<td>● Requires access to Air</td>
</tr>
<tr>
<td><strong>Nuclear Battery</strong></td>
<td>³H 20 nW/mm³</td>
<td>4.5 J/mm³</td>
<td>12.3 Years</td>
<td>Non-rechargeable</td>
<td>● Costly</td>
</tr>
<tr>
<td></td>
<td>⁶³Ni 0.5 nW/mm³</td>
<td>0.9 J/mm³</td>
<td>100.3 Years</td>
<td></td>
<td>● ¹⁴⁷Pr unavailable in United States</td>
</tr>
<tr>
<td></td>
<td>¹⁴⁷Pr 5 μW/mm³</td>
<td>2.4 J/mm³</td>
<td>2.6 Years</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Energy Harvester</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Light: Outdoor</strong></td>
<td>0.15 - 10 μW/mm³</td>
<td></td>
<td></td>
<td>N/A</td>
<td>● Availability of power is stochastic</td>
</tr>
<tr>
<td><strong>Light: Indoor</strong></td>
<td>10 nW/mm³</td>
<td></td>
<td></td>
<td>N/A</td>
<td></td>
</tr>
<tr>
<td><strong>Kinetic</strong></td>
<td>1 - 400 nW/mm³</td>
<td></td>
<td></td>
<td>N/A</td>
<td></td>
</tr>
<tr>
<td><strong>Thermal</strong></td>
<td>15 nW/mm³</td>
<td></td>
<td></td>
<td>N/A</td>
<td></td>
</tr>
<tr>
<td><strong>Radio Frequency</strong></td>
<td>0.01 - 0.1 nW/mm³</td>
<td></td>
<td></td>
<td>N/A</td>
<td>● Requires proximity to magnetic source</td>
</tr>
<tr>
<td><strong>Wireless Power Transfer</strong></td>
<td>8.3 mW/mm³</td>
<td></td>
<td></td>
<td>N/A</td>
<td></td>
</tr>
</tbody>
</table>

Table generated with values reported in [52-55, 83, 86].
Figure 1.8. Ragone plot appended with microsystems (Δ) from the literature. Each microsystem is displayed as an average power density on the plot (i.e., equal allocation of on-board source or battery to the remainder of microsystem). Plot constructed using method from [51] and using values reported in [52-55, 83, 86].
CHAPTER 2
WIRELESS POWER TRANSFER

Fundamentally, wireless power transfer uses the mutual magnetic field between a wireless power transmitter and a wireless power receiver to couple power from transmitter to receiver, as was shown in Figure 1.7. Therefore, Section 2.1 discusses generation of magnetic fields and the voltages they induce, along with their corresponding circuit models. Furthermore, Section 2.2 discusses power transfer between transmitter and receiver, focusing on maximal power transfer, efficiency, and operational regimes. As the target application to be powered is a microsystem, the chapter concludes with Section 2.3, which examines the effects of miniaturizing the wireless receiver.

2.1 Inductive Coupling

2.1.1 Magnetic Field Generation

According to Ampère’s circuital law, a current flowing through a transmitting coil generates an external magnetic field. The Biot-Savart law is a general method for determining the generated magnetic field and is pictorially shown in Figure 2.1a and analytically described by

\[
\vec{B} = \frac{\mu I}{4\pi} \int_s \frac{d\vec{s} \times \hat{R}}{\|\hat{R}\|},
\]  

(2.1)

where \(\mu\) is the permeability of the medium, \(I\) is the current flowing in the coil, \(s\) is the line describing the coil, and \(\hat{R}\) is the vector from the coil to the point in space where the magnetic field, \(\vec{B}\), is being evaluated. As an example of how a current-carrying coil generates a magnetic field, Figure 2.1b shows the simple case of a circular transmitter coil with \(r_T\) radius and \(N_T\) turns. The Biot-Savart law may then be used to calculate the on-axis magnetic field to be [94]:

18
\[ \vec{B}_T(z = d_C) \approx \frac{\mu_0 N_T}{2} \frac{r_T^2}{(r_T^2 + d_C^2)^{3/2}} z. \]  

(2.2)

First, note that the magnetic field on the \( z = d_C \) plane is approximately constant if the \( x \) or \( y \) displacement is much less than the coil’s radius \([94]\). Secondly, as distance from the coil increases and becomes much greater than the coil’s radius (i.e., \( d_C >> r_T \)), the magnetic field decays by \( d_C^3 \), which is characteristic of how near-field intensities decay with distance.

![Diagram](image)

Figure 2.1(a) Using current in a wire to generate a magnetic field given by the Biot-Savart law and (b) an example case of a circular loop generating a magnetic field.

### 2.1.2 Electromagnetic Induction

When the generated magnetic field is time-varying it can then be combined with Faraday’s law to induce an electromotive force (EMF) onto a receiver or pickup coil. The law states that the induced voltage (\( v_{\text{EMF}} \)) in a closed circuit is equal to the rate-of-change of the magnetic flux through the circuit, and this law is formally written as

\[
v_{\text{EMF}} = \frac{\partial \Phi_{\text{FLUX}}}{\partial t} = \frac{\partial}{\partial t} \oint_{A_{\text{ENC}}} \vec{B} \cdot d\vec{A}_{\text{ENC}}.
\]

(2.3)

where \( \vec{B} \) is the magnetic field, \( A_{\text{ENC}} \) is a surface that is bounded by the closed circuit, and \( \Phi_{\text{FLUX}} \) corresponds to the magnetic flux (here, \( \Phi_{\text{FLUX}} \) absorbs the number of turns); all of which is shown pictorially in Figure 2.2a \([95]\). For the simple case of circular coaxial
transmitting and receiving coils, as shown in Figure 2.2b, the magnetic flux in the receiving coil reduces to

\[
\Phi_{\text{FLUX}, R} \bigg|_{r_R << r_T} = \bar{B}_T \bar{A}_{\text{ENC}, R} = \bar{B}_T N_R \pi r_R^2, \tag{2.4}
\]
as \bar{B}_T is constant on the x-y plane for a receiving coil radius, \( r_R \), much smaller than a transmitting coil radius, \( r_T \), and as \( \bar{B}_T \) is aligned with \( \bar{A}_{\text{ENC}, R} \). Then, substituting Equation (2.2) into Equation (2.4) results in

\[
\Phi_{\text{FLUX}, R} \bigg|_{r_R << r_T} = i_T \frac{\mu \pi}{2} \frac{N_T N_R r_T^2 r_R^2}{\left(r_T^2 + d_c^2\right)^{3/2}}. \tag{2.5}
\]

When the transmitting current is time-varying, so is the magnetic flux through the receiving coil, which induces a voltage equal to

\[
v_{\text{EMF}, R} \bigg|_{r_R << r_T} = \frac{\partial \Phi_{\text{FLUX}, R}}{\partial t} \bigg|_{r_R << r_T} = \frac{di_T}{dt} \frac{\mu \pi}{2} \frac{N_T N_R r_T^2 r_R^2}{\left(r_T^2 + d_c^2\right)^{3/2}}. \tag{2.6}
\]

![Figure 2.2(a) Faraday’s electromagnetic induction law and (b) an example of electromagnetic induction for the case of two circular coaxial coils.](image-url)
2.1.3 Mutual Inductance

The above-mentioned example illustrates how a transmitting coil can induce a voltage onto a receiving coil. In general, the relationship between the magnetic flux through the receiving coil, $\Phi_{FLUX.R}$, and the transmitting current, $i_T$, can be expressed as

$$\Phi_{FLUX.R} = M_{RT} i_T,$$  \hspace{1cm} (2.7)

where $M_{RT}$ is defined as the mutual inductance from the transmitting coil to the receiving coil. For the case of the aligned circular coils, the mutual inductance is

$$M_{RT} \bigg|_{r_R << r_T} = \frac{\mu \pi}{2} \frac{N_T N_R r_T^2 r_R^2}{(r_T^2 + d_c^2)^{3/2}}.$$  \hspace{1cm} (2.8)

In general, the mutual inductance can be calculated using the Neumann formula, which is equal to

$$M_{RT} = \frac{\mu}{4\pi} \oint_{s_{T}, s_{R}} \oint_{\tilde{R}_{d}} d\tilde{s}_T \cdot d\tilde{s}_R,$$  \hspace{1cm} (2.9)

where $\tilde{s}_T$ and $\tilde{s}_R$ are the curves that describe the transmitting and receiving coils, respectively, and $\tilde{R}_{d}$ is the vector from $d\tilde{s}_T$ to $d\tilde{s}_R$. Equation (2.9) is the same if the transmitting coil is relabeled to the receiving coil and vice-versa, which means that the mutual inductance from transmitter to receiver is the same as the mutual inductance from receiver to transmitter or

$$M_{RT} = M_{TR}.$$  \hspace{1cm} (2.10)

From this point forward, $M_{RT}$ and $M_{TR}$ will simply be referred to as $M_C$, as there is no need to distinguish between the two mutual inductances.

In addition to mutual inductances, both the coils have their own self-inductance, defined as

21
$$\Phi_{\text{FLUX},R} = L_R i_R$$

(2.11)

and

$$\Phi_{\text{FLUX},T} = L_T i_T,$$

(2.12)

where $L_R$ and $L_T$ are the self-inductances of the receiving and transmitting coil, respectively. The total flux of the transmitting and receiving coils can be combined as the linear combination of self- and mutually-generated magnetic fields,

$$\begin{bmatrix} \Phi_{\text{FLUX},R} \\ \Phi_{\text{FLUX},T} \end{bmatrix} = \begin{bmatrix} L_R & M_C \\ M_C & L_T \end{bmatrix} \begin{bmatrix} i_R \\ i_T \end{bmatrix},$$

(2.13)

which when combined with Faraday’s law yields

$$\begin{bmatrix} v_{\text{COIL},R} \\ v_{\text{COIL},T} \end{bmatrix} = \frac{\partial}{\partial t} \begin{bmatrix} \Phi_{\text{FLUX},R} \\ \Phi_{\text{FLUX},T} \end{bmatrix} = \begin{bmatrix} L_R & M_C \\ M_C & L_T \end{bmatrix} \begin{bmatrix} \frac{di_R}{dt} \\ \frac{di_T}{dt} \end{bmatrix}.$$  

(2.14)

Equation (2.13) is more commonly represented by its equivalent circuit representation as shown in Figure 2.3. Each coil in the equivalent circuit contains an inductor (i.e., $L_T$ or $L_R$) that represents the self-induced EMF and a dependent voltage source that models the externally-induced EMF. When the mutual inductance between the coils goes to zero, each coil reduces to an isolated inductor of value equal to its self-inductance.

![Figure 2.3](image-url)

**Figure 2.3.** (a) Two inductively coupled coils represented with their (b) equivalent circuit model.
Energy is stored in the magnetic field generated by the inductively coupled system. To determine that potential energy, the work done on the coils is investigated having first assumed no magnetic field (i.e., $i_R$ and $i_T$ are initially zero). The work done to increase the magnetic field is then equal to the energy stored in the coils or

$$E_{STORED} = \int_0^T v_{COIL,R}i_R dt + \int_0^T v_{COIL,T}i_T dt,$$

which when combined with Equation (2.14) reduces to

$$E_{STORED} = \int_0^T \left( L_R \frac{di_R}{dt} + M_C \frac{di_R}{dt} \right) i_R dt + \int_0^T \left( L_T \frac{di_T}{dt} + M_C \frac{di_T}{dt} \right) i_T dt.$$

Further simplification gives

$$E_{STORED} = L_R \int_0^T i_R \frac{di_R}{dt} dt + L_T \int_0^T i_T \frac{di_T}{dt} dt + M_C \int_0^T \left( \frac{di_R}{dt} + \frac{di_T}{dt} \right) i_R dt$$

and finally equals

$$E_{STORED} = \frac{1}{2} L_R i_R^2 + \frac{1}{2} L_T i_T^2 + M_C i_R i_T,$$

where $I_R$ and $I_T$ are the receiver and transmitter currents some $T$ time later, respectively. Notice that the first two terms in $E_{STORED}$ correspond to the energy stored in both coils if they were not coupled. However, when the coils are coupled an additional term appears, which represents the amount of additional work required to generate a magnetic field in the presence of an existent magnetic field. Furthermore, the energy stored in the coils must be strictly positive for energy conservation to hold, which implies

$$\frac{1}{2} L_R i_R^2 + \frac{1}{2} L_T i_T^2 + M_C i_R i_T \geq 0.$$

For the above equation to be true for all $I_R$ and $I_T$, the mutual inductance is constrained by

$$\sqrt{L_T L_R} \geq M_C.$$

As such, the mutual inductance is often described by
\[ M_C = k_C \sqrt{L_T L_R}, \quad 0 \leq k_C \leq 1, \]  

(2.21)

where \( k_C \) is the coupling factor and is indicative of the fraction of flux that reaches the other coil. When \( k_C \) is equal to one, the inductive link simplifies to a transformer. For the opposite extreme of zero coupling (i.e., \( k_C = 0 \)), the inductive link reduces to two isolated inductors.

### 2.1.4 Circuit Model

The equivalent circuit of Figure 2.3 captures the dynamics of magnetic induction, however, the inclusion of parasitic resistances and capacitances of the coils improves model accuracy and also allows for assessment of dissipative power losses. A lumped model of inductively coupled coils with parasitic elements is shown in Figure 2.4. The model includes the addition of equivalent series resistances (ESR) \( R_L \) and \( R_T \) as well as the addition of parasitic winding capacitances \( C_{PAR,R} \) and \( C_{PAR,T} \) that result from closely spaced coils [96]. It should be noted, that these lumped models do not accurately forecast the frequency response of the coils for frequencies above their self-resonance. While more accurate distributed models capture the frequency response [22], the frequency content of power transfer is well contained within the frequency limits of the lumped model, which explains why the vast majority of wireless power receivers use the lumped model, [22, 80, 88-93].

![Figure 2.4. Inductively coupled coil model with inclusion of parasitic equivalent series resistance and winding capacitance.](image)
2.2 Power Transfer

In inductively coupled systems, the wireless power transmitter generates a time-varying magnetic field that changes the receiver coil’s flux to induce a $v_{EMF,R}$ coil voltage. The power receiver then derives power from the induced $v_{EMF,R}$ voltage using a power converter as shown in Figure 2.5. Generating the time-varying magnetic field corresponds to driving the transmitter coil with a time-varying transmitter current, $i_T$. The majority of wireless powering topologies drive the transmitter winding using a signal-tone sinusoidal current waveform, although more exotic waveforms, such as Gaussian pulses, have also been used [97]. To produce a single-tone AC current, a sinusoidal voltage source, $v_T$, is used to drive the transmitter coil along with a series resonant capacitor, $C_T$. The resonant capacitor’s impedance is chosen to cancel the impedance of $L_T$ at the operating frequency of the voltage source, $f_O$, so that a larger transmitter coil current and a correspondingly larger external magnetic field are generated. This larger magnetic field is used to induce a larger $v_{EMF,R}$ voltage from which more power can be extracted.

![Figure 2.5. Typical example of inductively coupled power transfer being used to power a load.](image)

For power and efficiency analysis of inductively coupled systems, it is helpful to model the power converter as an impedance, $Z_L$, as shown in Figure 2.6a. Although this modeling might seem like a limiting case, circuit analysis with $Z_L$ yields equivalent solutions for the more general maximum power transfer and efficiency solutions found in
Appendix A. Therefore, the $Z_L$ model highlights many useful characteristics of the power transfer, namely, maximum power transfer and efficiency, which will prove useful as a comparative benchmark. Furthermore, the parasitic winding capacitances, $C_{PAR.T}$ and $C_{PAR.R}$, can be neglected for transient analysis, given that their self-resonating frequencies are much greater than the operation frequency and that their $R-L$ time constants are greater than their respective $R-C$ time constants (see Appendix B for details), which is assumed to be the case.

\[ V_{emf,t} = j\omega_0 M_C I_t \]

Figure 2.6. (a) Simplified circuit for wireless power transfer using $Z_L$ to model the power converter and (b) translation of that circuit into the frequency domain for analysis.

Figure 2.6a displays the simplified model for the wireless power transfer. Given that the primary driving voltage is sinusoidal, it is constructive to analyze the circuit in the frequency domain, as shown in Figure 2.6b. As mentioned previously, the impedances of $C_T$ and $L_T$ are chosen such that they cancel at the operating frequency. The circuit in Figure 2.6b can be further reduced by reflecting the receiver onto the transmitter circuit. To do so, the $V_{emf,t}$ voltage is expressed as

\[ Z_L = R_L + jX_L \]
\[ V_{\text{emf},r} = j\omega_0 M_c I_r, \]  
\[ \text{(2.22)} \]

which when combined with the receiver current,

\[ I_r = \frac{-V_{\text{emf},r}}{R_R + j\omega_0 L_R + Z_L} = \frac{-j\omega_0 M_c I_t}{R_R + j\omega_0 L_R + Z_L}, \]  
\[ \text{(2.23)} \]

becomes

\[ V_{\text{emf},r} = j\omega_0 M_c I_r = \frac{\omega_0^2 M_c^2}{R_R + j\omega_0 L_R + Z_L} I_t = Z_{EQ,T} I_t. \]  
\[ \text{(2.24)} \]

As such, the loading from the receiver onto the transmitter can be represented as a reflected impedance onto the transmitter of value

\[ Z_{EQ,T} = \frac{\omega_0^2 M_c^2}{R_R + j\omega_0 L_R + Z_L}, \]  
\[ \text{(2.25)} \]

as is shown in Figure 2.7a. In a similar fashion, the transmitter can be reflected onto the receiver circuit, by expressing the \( V_{\text{emf},r} \) voltage as

\[ V_{\text{emf},r} = j\omega_0 M_c I_t, \]  
\[ \text{(2.26)} \]

and combing with the transmitter current,

\[ I_t = \frac{V_t - V_{\text{emf},r}}{R_T} = \frac{V_t - j\omega_0 M_c I_r}{R_T}, \]  
\[ \text{(2.27)} \]

yields

\[ V_{\text{emf},r} = j\omega_0 M_c I_t = \frac{j\omega_0 M_c V_t}{R_T} + \frac{\omega_0^2 M_c^2}{R_T} I_r = V_{eq,r} + R_{EQ,R} I_r, \]  
\[ \text{(2.28)} \]

The resulting transmitter reflection onto the receiver results in an equivalent source voltage and resistance of values

\[ V_{eq,r} = \frac{j\omega_0 M_c V_t}{R_T} \]  
\[ \text{(2.29)} \]

and
\[ R_{EQ,R} = \frac{\omega_a^2 M_C^2}{R_T}, \]  

which are shown in Figure 2.7b.

![Equivalent circuit with (a) receiver reflected to transmitter and (b) transmitter reflected to receiver.](image)

**Figure 2.7.** Equivalent circuit with (a) receiver reflected to transmitter and (b) transmitter reflected to receiver.

The reflection-reduced circuits prove insightful as they decouple the more complicated coupled circuit of Figure 2.6b into two simpler to understand circuits. For example, the receiver reflected circuit (i.e, Figure 2.7a) shows that the load seen by the transmitter \( Z_{EQ,T} \) becomes larger with higher coupling (i.e, increased \( k_C \)) and with heavier receiver current draw (i.e., decreased \( Z_L \)). However, the current draw is limited by the pickup coil’s impedance (i.e, \( R_R \) and \( j\omega_OL_R \)), so that further reductions in \( Z_L \) constitute diminishing returns in \( Z_{EQ,T} \). From the receiver’s perspective, Figure 2.7b, the unloaded \( V_{emf,r} \) source or equivalently the \( V_{eq,r} \) voltage increases with higher coupling and unloaded transmitter current (i.e., \( V_t / R_T \)). When loaded, however, the \( V_{emf,r} \) voltage decreases from \( V_{eq,r} \) because of the equivalent source resistance \( R_{EQ,R} \). This source resistance also increases with higher coupling, but does not play a significant role until the coupling factor is high enough to overcome pickup coil’s series impedance (i.e., \( R_R \) and \( j\omega_OL_R \)).
2.2.1 Maximal Power Transfer

For the purposes of power transfer to the load, it is fitting to use the transmitter-reflected-to-the-receiver circuit, shown in Figure 2.7b. From inspection, the power transmitted to the load is

\[ P_{LOAD} = \frac{1}{2} I_r I_r^* R_L, \]  

(2.31)

where

\[ I_r = \frac{-V_{eq,r}}{R_{eq,r} + R_L + j(\omega_L L_R + X_L)} \]  

(2.32)

and \( Z_L \) has been expressed as the sum of its real component, \( R_L \), and its reactive component, \( X_L \) (i.e., \( Z_L = R_L + jX_L \)). Using Equation (2.21) and some algebraic manipulation, \( P_{LOAD} \) can be expressed as

\[ P_{LOAD} = \frac{k_c^2 Q_T Q_R \left( \frac{|V_i|^2}{2R_T} \frac{R_L}{R_T} \right) \left( \frac{R_L}{R_R} \right) \left( \frac{\omega_L L_R + X_L}{R_R} \right)^2}{\left( k_c^2 Q_T Q_R + 1 + \frac{R_L}{R_R} \right)^2 \left( \frac{\omega_L L_R + X_L}{R_R} \right)^2}, \]  

(2.33)

where \( Q_T \) and \( Q_R \) are the quality factors of the transmitter and receiver coils, respectively. The quality factors are explicitly written as

\[ Q_T = \frac{\omega_L L_T}{R_T} \]  

(2.34)

and

\[ Q_R = \frac{\omega_L L_R}{R_R}. \]  

(2.35)

Equation (2.33) suggests that the reactive component of the load (i.e., \( jX_L \)) should be set to cancel the reactive component of the pickup coil (i.e., \( j\omega_L L_R \)) as a requirement for maximum \( P_{LOAD} \); as any other \( X_L \) would reduce \( P_{LOAD} \). This is in accord with the conjugate matching requirement for maximum power transfer. In fact, maximum power
transfer takes place when \( Z_L \) equals the conjugate of the source impedance shown in Figure 2.7b. As such, the maximum power delivered to \( Z_L \) occurs when

\[
Z_{L(MAX)} = \left( R_{BQ,R} + R_R + j\omega_0 L_R \right) = \frac{\omega_0^2 M_c^2}{R_T} + R_R - j\omega_0 L_R
\]  

(2.36)
or separated into its real and reactive components gives

\[
R_{L(MAX)} = \frac{\omega_0^2 M_c^2}{R_T} + R_R = R_R \left( 1 + k_c^2 Q_T Q_R \right)
\]  

(2.37)
and

\[
jX_{L(MAX)} = - j\omega_0 L_R.
\]  

(2.38)

The expressions show that the requirement for the reactive component of \( Z_{L(MAX)} \) does not change with coupling and only depends on the receiver’s self-inductance. However, the requirement for the real component of \( Z_{L(MAX)} \) does change with coupling, especially when \( k_c^2 Q_T Q_R \) is greater than one. This suggests that \( Z_L \), and in particular \( R_L \), would have to be adaptive across coupling factor for maximal power transfer. Figure 2.8a displays this requirement for \( R_L \) across coupling factor as an annotated line on a contour plot of normalized \( P_{LOAD} \) (the entire plot assumes reactive matching i.e., \( X_L = X_{L(MAX)} \)). This \( R_L \) equal to \( R_{L(MAX)} \) line traces out the maximum \( P_{LOAD} \) across coupling. Alternatively, inserting \( Z_{L(MAX)} \) into the general \( P_{LOAD} \) Equation (2.33) explicitly yields the maximal power delivery to the load across coupling factors, that is

\[
P_{LOAD(MAX)} = \frac{k_c^2 Q_T Q_R V_t^2}{1 + k_c^2 Q_T Q_R} \frac{V_t^2}{8R_T}
\]  

(2.39)
which is plotted in Figure 2.8b.
The plots in Figure 2.8 highlight that larger $k_c^2 Q_T Q_R$ factors are preferred as they result in a higher possible power transfer (having assumed conjugate matching). Furthermore, the $k_c^2 Q_T Q_R$ factor can also be used to identify two coupling regimes, namely, the high and low coupling regimes. Table 2.1 displays how expressions for $P_{LOAD(MAX)}$ and $Z_{L(MAX)}$ simplify for each coupling regime. For the low coupling regime, defined by the $k_c^2 Q_T Q_R$ factor being much smaller than one, $P_{LOAD(MAX)}$ increases linearly with $k_c^2 Q_T Q_R$, which suggests that increasing the quality factor for each of the coils is critical for increasing power transfer. Moreover, as the conjugate matching requirement in this regime is constant across coupling factor it is relatively easier to implement $Z_{L(MAX)}$. On the other hand, conjugate matching for the high coupling regime ($k_c^2 Q_T Q_R >> 1$) is more difficult as $Z_{L(MAX)}$ varies with $k_c$ and would require a $Z_L$ that is adaptive. However, given the conjugate matching, $P_{LOAD(MAX)}$ remains constant across $k_c$ in the high coupling regime and equals the overall maximal power point. Finally, notice that the
high coupling regime corresponds to the case when \( Z_{EQ,T} \) in Figure 2.7a becomes comparable to \( R_T \). Given that case, maximal power transfer to \( Z_{EQ,T} \) occurs when \( Z_{EQ,T} \) equals \( R_T \), which is why \( R_{L(MAX)} \) increases to satisfy this condition.

**Table 2.1 Simplification of Power Transfer Expressions in the Low and High Coupling Regime**

<table>
<thead>
<tr>
<th></th>
<th>Valid For All Regimes: ( k_c^2 Q_T Q_R \ll 1 )</th>
<th>Low Coupling Regime: ( k_c^2 Q_T Q_R \ll 1 )</th>
<th>High Coupling Regime: ( k_c^2 Q_T Q_R \gg 1 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( P_{LOAD(MAX)} )</td>
<td>( \frac{k_c^2 Q_T Q_R</td>
<td>V_i</td>
<td>^2}{1 + k_c^2 Q_T Q_R 8R_T} )</td>
</tr>
<tr>
<td>( Z_{L(MAX)} )</td>
<td>( R_R(1+k_c^2 Q_T Q_R) - j\omega O_L R )</td>
<td>( R_R - j\omega O_L R )</td>
<td>( R_R k_c^2 Q_T Q_R - j\omega O_L R )</td>
</tr>
</tbody>
</table>

### 2.2.2 System Efficiency

The requirements for maximal power transfer do not correspond to those for maximal system efficiency and in some applications (e.g., battery powered transmitters) it may be more important to conserve energy than to supply maximum power. As such, this subsection discusses system efficiency. For simplicity, system efficiency, \( \eta_{SYS} \), can be split up into the product of transmitter and receiver efficiency, \( \eta_T \) and \( \eta_R \), respectively. System efficiency can then be written as

\[
\eta_{SYS} = \eta_T \eta_R = \left( \frac{P_R}{P_T} \right) \left( \frac{P_{LOAD}}{P_R} \right),
\]

where \( \eta_T \) is the fraction of power sourced by \( V_t \) (i.e., \( P_T \)) that transfers over to the receiver and \( \eta_R \) is the fraction of power in the receiver that is delivered to the load (i.e., \( Z_L \)). For further simplification, the reactive component of \( Z_L \) is assumed to cancel the self-inductance of the pickup coil (i.e., \( jX_L = - j\omega O_L R \)) throughout the efficiency analysis, such that, the reflection-reduced circuits simplify to those shown in Figure 2.9.
Figure 2.9. Equivalent reflected circuits with cancelled reactive components (i.e., $jX_L = -j\omega_0L_L$) for the (a) receiver reflected to transmitter and (b) transmitter reflected to receiver.

To begin with, the transmitter efficiency is considered, which lends itself for analysis using the receiver reflected to transmitter circuit of Figure 2.9a. From the circuit, the fraction of power that flows into $V_{emf,t}$ is

$$\eta_T = \frac{P_R}{P_T} = \frac{\frac{|I_t|^2}{2} R_{EQ,T}}{\frac{|I_t|^2}{2} R_T + \frac{|I_t|^2}{2} R_{EQ,T}} = \frac{R_{EQ,T}}{R_T + R_{EQ,T}}. \quad (2.41)$$

Further reduction is possible by using the definition of $R_{EQ,T}$ (shown in Figure 2.9a) and the expression for the quality factors (Equations 2.34 and 2.35) to yield

$$\eta_T = \frac{k_T^2 Q_T Q_R}{k_T^2 Q_T Q_R + 1 + \frac{R_L}{R_T}}. \quad (2.42)$$

Similarly, the receiver efficiency may be calculated using the transmitter reflected to the receiver circuit of Figure 2.9b. In this case, $\eta_R$ is the fraction of power in the receiver that is delivered to $R_L$ or

$$\eta_R = \frac{P_{LOAD}}{P_R} = \frac{\frac{|I_r|^2}{2} R_L}{\frac{|I_r|^2}{2} R_T + \frac{|I_r|^2}{2} R_L} = \frac{R_L}{R_T + R_L}. \quad (2.43)$$
Note that $R_{EQ,R}$ is a fictitious resistance that simply models how $V_{emf,r}$ decreases when loaded. As such, power dissipation across $R_{EQ,R}$ simply reduces the total power sourced from the $V_{emf,r}$ voltage, but does not affect receiver efficiency. Finally, combining transmitter and receiver efficiencies yield the overall system efficiency to be

$$
\eta_{SYS} = \eta_T \eta_R = \frac{k_C^2 Q_T Q_R}{k_C^2 Q_T Q_R + 1 + \frac{R_L}{R_R} \left(1 + \frac{R_R}{R_L}\right)}. 
$$

(2.44)

The system efficiency expression given by Equation (2.44) highlights the recurring importance of the $k_C^2 Q_T Q_R$ factor. In addition, the expression has two competing $R_L$ terms within its denominator that suggests that there is an optimal $R_L$ value that maximizes system efficiency. This optimal value of $R_L$ is found by solving

$$
\frac{\partial \eta_{SYS}}{\partial R_L} = 0,
$$

(2.45)

which yields the required $R_L$ for maximal system efficiency, that is

$$
R_{L(OPT)} = R_R \sqrt{1 + k_C^2 Q_T Q_R}. 
$$

(2.46)

Note, that the $R_L$ that yields optimal system efficiency is annotated with subscript “(OPT)”, which should not be confused with the $R_{L(MAX)}$ variable that corresponds to maximum power transfer. Furthermore, notice that the requirement for $R_{L(OPT)}$ varies with coupling factor, especially when $k_C^2 Q_T Q_R$ is greater than one, such that an adaptive $R_L$ would be required to track $R_{L(OPT)}$. Figure 2.10a displays this requirement for $R_L$ across coupling factor as an annotated line on a contour plot of system efficiency. This $R_L$ equal to $R_{L(OPT)}$ line traces out the maximum $\eta_{SYS}$ across coupling. Alternatively, inserting $R_{L(OPT)}$ into the global $\eta_{SYS}$ Equation (2.44) explicitly yields the maximal system efficiency across coupling factors, that is

$$
\eta_{SYS(OPT)} = \frac{k_C^2 Q_T Q_R}{\left(1 + \sqrt{1 + k_C^2 Q_T Q_R}\right)^2}, 
$$

(2.47)
which is plotted in Figure 2.10b.

\[
R_L = (\text{OPT}) \quad \text{with} \quad Z_L(\text{OPT}) \quad \text{Load Requirement}
\]

\[
\text{Maximum System Efficiency} \quad \eta_{\text{SYS}}(\text{OPT}) \quad \%\n\]

\[
\text{Maximum System Efficiency with } Z_L(\text{OPT}) \quad \text{Load Requirement}
\]

Figure 2.10. (a) Contour plot of system efficiency with the dashed line corresponding to the \( R_L \) that maximizes the system efficiency for a given \( k_C^2QLQR \) and (b) the corresponding traced out maximum system efficiency across coupling.

In a similar fashion to the maximal power expressions, the system efficiency expressions can also be separated into low and high coupling regimes, as shown in Table 2.2. For the case of the low coupling regime, \( \eta_{\text{SYS(OPT)}} \) increases linearly with the \( k_C^2QLQR \) factor and \( Z_L(\text{OPT}) \) is constant across coupling factor \( k_C \). Notice, that in the low coupling regime, \( Z_L(\text{OPT}) \) equals \( Z_L(\text{MAX}) \), which means that both maximum efficiency and maximum power transfer conditions can be simultaneously satisfied in the low coupling regime. However, \( Z_L(\text{OPT}) \) takes a different form in the high coupling regime, but still requires the same reactive component (viz., \(-j\omega_OL_R\)). Ideally, \( \eta_{\text{SYS(OPT)}} \) asymptotically approaches an efficiency of 100% as the \( k_C^2QLQR \) grows to infinity. However, as \( k_C \) is bounded to a maximum value of one, the largest efficiency achievable is still limited by the quality factors of the coils.
### Table 2.2 Simplification of Efficiency Expressions in the Low and High Coupling Regime

<table>
<thead>
<tr>
<th></th>
<th>Valid For All Regimes:</th>
<th>Low Coupling Regime: $k_C^2 Q_T Q_R &lt;&lt; 1$</th>
<th>High Coupling Regime: $k_C^2 Q_T Q_R &gt;&gt; 1$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\eta_{SYS(OPT)}$</td>
<td>$\frac{k_C^2 Q_T Q_R}{\left(1 + \sqrt{1 + k_C^2 Q_T Q_R}\right)^2}$</td>
<td>$\frac{k_C^2 Q_T Q_R}{4}$</td>
<td>$\frac{\sqrt{k_C^2 Q_T Q_R}}{2 + \sqrt{k_C^2 Q_T Q_R}}$</td>
</tr>
<tr>
<td>$Z_{L(OPT)}$</td>
<td>$R_R \sqrt{1 + k_C^2 Q_T Q_R - j\omega_0 L_R}$</td>
<td>$R_R - j\omega_0 L_R$</td>
<td>$R_R \sqrt{k_C^2 Q_T Q_R - j\omega_0 L_R}$</td>
</tr>
</tbody>
</table>

#### 2.2.3 Discussion

Thus far power transfer and system efficiency have been treated separately, with emphasis on maximizing each individually. However, their maximizing conditions differ and as a result maximizing power transfer may lead to plummeting system efficiencies and vice versa. Therefore, to gain insight into this dilemma Figure 2.11a displays how $P_{LOAD}$ varies along the optimal system efficiency condition (i.e., $Z_{L(OPT)}$) and Figure 2.11b displays how $\eta_{SYS}$ varies along the maximum power condition (i.e., $Z_{L(MAX)}$). Within the low coupling regime, $Z_{L(OPT)}$ approaches $Z_{L(MAX)}$ such that their respective $P_{LOAD}$ and $\eta_{SYS}$ traces lie on top of one another, which means both maximal power transfer and maximal system efficiency are achievable in this regime. As the coupling transitions into the high coupling regime, however, the traces separate and their differences become apparent. In particular, the load power along the $Z_L = Z_{L(OPT)}$ trace sharply decreases to about an order of magnitude less than the peak power. Furthermore, the system efficiency along the $Z_L = Z_{L(MAX)}$ trace asymptotically approaches 50% with an increasing $k_C^2 Q_T Q_R$ factor. Therefore, designing for maximum power transfer or maximum efficiency gives suboptimal results for the other and the best results usually come in the form of a compromise between the two.
Figure 2.11. Gray and black traces indicating load requirements for maximum power transfer and maximum system efficiency, respectively, appended on (a) power transfer and (b) system efficiency plots.
Finally, it is important to realize that the analyses for power transfer and system efficiency are highly idealized. In particular, the analyses do not account for the conduction losses associated with harmonic transmitter and receiver current components. Furthermore, power converters typically have other power losses, such as switching or quiescent losses, that were not accounted for during the analyses. However, the analyses do offer the fundamental limits of power transfer and system efficiency from which a comparative benchmark may be established.

2.3 Receiver Miniaturization

Hitherto, the discussion on wireless power transfer has been very general; however, when considering micro-scale applications, it is important to consider the effects of miniaturization of the receiver coil. For one, miniaturization tends to reduce the quality factor of the receiver coil \([98]\), which matters, as discussed in the previous subsection, because the product \(k_C^2Q_TQ_R\) ultimately determines the maximal system efficiency for an inductive link and also determines the coupling regime. Furthermore, miniaturization also reduces the coupling coefficient (i.e., \(k_C\)) associated with the inductive link. To highlight the reduction in \(k_C\), a didactic example of two coaxial circular coils is presented below.

![Figure 2.12. Example case of two coaxial circular coils with transmitter radius \((r_T)\), receiver radius \((r_R)\), and distance \((d_C)\) between them.](image)

Figure 2.12 displays the example of two coaxial circular transmitter and receiver coils. Note, that this is the same example for which the mutual inductance was solved for earlier this chapter. However, that derivation utilized the small coil approximation (viz., $r_R \ll r_T$); in general though, the mutual inductance and the coupling factor can be found in [99]. Using the general results, Figure 2.13 displays how $k_C$ is affected by the scaling of the receiver coil. First, notice that the coupling factor decreases with a smaller $r_R / r_T$ ratio, which can be thought of intuitively as the receiver coil seeing less magnetic flux due to its shrinking flux area. Second, the coupling factor remains relatively independent of coil separation so long as the coils are within a transmitter’s radius of one another ($r_T > d_C$). Otherwise, the coupling factor decreases rapidly (by the cubed power) with coil separation. As such, the transmitter radius should be selected to be at least the distance between the coils (with the optimal value being $r_T = \sqrt{2} d_C$ [94]). Given the constraint on $r_T$, miniaturization of the receiver coil (i.e., $r_R$) results in smaller coupling factors.

![Coupling factor between two circular coaxial coils](image)

**Figure 2.13.** Coupling factor between two circular coaxial coils with transmitter radius ($r_T$), receiver radius ($r_R$), and distance ($d_C$) between them.
Miniaturization of the receiver coil then reduces both the receiver quality factor and the coupling factor (i.e., $Q_R$ and $k_C$) to cause an overall reduction of the $k_C^2 Q_T Q_R$ product, which suggests that with enough scaling the inductive power transfer will operate in the low coupling regime. Given that the system operates in this low coupling regime, the transmitter reflected to the receiver circuit simplifies from that of Figure 2.14a to that shown in Figure 2.14b. The simplified circuit removes $R_{EQ,R}$, as it is much smaller than $R_R$ in the low coupling regime (from $k_C^2 Q_T Q_R << 1$). The elimination of $R_{EQ,R}$ signifies that the $V_{emf,r}$ voltage is independent of loading and therefore only depends on $V_{eq,r}$, which is the induced open circuit voltage. With regard to the transmitter, the low coupling regime corresponds to insignificant loading (i.e., $R_{EQ,T} << R_T$ in Figure 2.9), which means that transmitter current and the corresponding generated magnetic field are unaltered with receiver loading so that the induced receiver voltage of Figure 2.14b is also independent of receiver loading.

For considering how the induced open circuit voltage scales with receiver coil miniaturization, Figure 2.15 displays a shrinking receiver coil in a time-varying magnetic field. As can be seen from the figure, the magnetic flux of the shrinking coil reduces as its area decreases (for a fixed geometry). This reduction in magnetic flux ultimately results in low induced voltages (small $v_{EMF,R}$). These low voltages present a challenge,
because although the power converter shown in Figure 2.5 was modeled as an impedance throughout this chapter (i.e., $Z_L$), real power converters require a minimum input voltage to deliver power. Furthermore, as the microsystem ultimately requires DC power (in the form of a supply or battery voltage), the converter needs to rectify low amplitude $v_{EMF,R}$ voltages. Therefore, the following chapter discusses low voltage rectifiers and their application in inductively coupled power transfer for microsystems.

Figure 2.15. Reduced magnetic flux and corresponding induced voltage ($v_{EMF,R}$) with shrinking of receiver coil from (a) to (b).
CHAPTER 3
LOW VOLTAGE RECTIFIERS

There are three categories of wireless power receivers, all of which aim to rectify low induced voltages (i.e. small $v_{EMF,R}$): the resonant receiver ($LC$-boosted), the voltage multiplier, and the inductive rectifier. The resonant receiver uses a high-$Q$ filter to boost low induced voltages to conventional rectifiable voltages. The voltage multiplier, also known as Dickson charge pump, Villard cascade, and Cockcroft-Walton generator, uses capacitors as energy storage elements to pump charge to higher voltages. Finally, the inductive rectifier uses an inductor as an energy storage device to build current and then direct that current to a battery. All of these techniques use energy storage elements to build sufficient energy for rectification, with the voltage multiplier and resonant receiver building voltages above the voltage threshold of standard rectifiers (e.g., diode-bridge) and with the inductive rectifier building sufficient current to overcome the losses associated with controlling the inductor.

3.1 Resonant Receivers

3.1.1 High-$Q$ Filter

Induced coil voltages (i.e., $v_{EMF,R}$) are usually too low for standard voltage rectification (e.g., diode-bridge and voltage doubler). As such, a high-$Q$ filter inserted after the coil, as illustrated in Figure 3.1a, allows for a boosted voltage, $v_{BOOST}$, to be generated that is more appropriate for rectifying. The filter most frequently used is shown in Figure 3.1b and is comprised of the coil inductance and a parallel capacitor, $C_R$ [92, 100-102]. The transfer function of the $L_R$-$C_R$ filter highlights how the filter generates the boosted voltage, which is analytically described by
\[
\frac{V_{\text{boost}}}{V_{\text{emf},r}} = \frac{1/sC_R}{sL_R + R_L + 1/sC_R} = \frac{\omega_R^2}{s^2 + s \frac{\omega_R}{Q_R} + \omega_R^2},
\]

(3.1)

where \(\omega_R\) corresponds to the natural frequency (i.e., \(\omega_R^2 = 1/L_RC_R\)) and \(Q_R\) corresponds to the quality factor \((Q_R = \omega_R L_R / R_L)\), and is graphically depicted by Figure 3.2. When the natural frequency of the \(L_R-C_R\) filter matches that of the driving \(v_{\text{EMF},R}\) frequency, \(f_o\), the filter amplifies \(v_{\text{EMF},R}\) by a factor of \(Q_R\), or

\[
\left| \frac{V_{\text{boost}}}{V_{\text{emf},r}} \right|_{s = j\omega_R} = Q_R,
\]

(3.2)

to effectively reduce the input-referred threshold of the combined rectifier and \(L_R-C_R\) filter by a factor of \(Q_R\).

![Figure 3.1. (a) Resonant receiver system with (b) an \(L_R-C_R\) filter implementation.](image)

![Figure 3.2. \(L_R-C_R\) filter frequency response.](image)
While the \( L_R-C_R \) filter boosts the \( v_{EMF,R} \) voltage, it only does so for frequencies near the natural frequency. Figure 3.2 highlights how small deviations away from \( \omega_R \) result in drastic reductions in gain, such that tuning becomes a necessity to lessen the effects of gain sensitivity with respect to frequency. Although frequency sensitive, when the resonant filter is driven at resonance, it builds a large inductor current, \( i_L \), which flows through the \( v_{EMF,R} \) voltage source. In other words, power extraction from \( v_{EMF,R} \) (i.e., \( P_{EMF,R} \)) is relatively high and found in Appendix C to be

\[
P_{EMF,R} \bigg|_{2\pi f_o} = \frac{V_{emf,r} V_{C(MAX)}}{2\omega_R L_R},
\]

where \( V_{C(MAX)} \) corresponds to the maximum \( C_R \) voltage, typically limited by the voltage rectifier.

To account for frequency sensitivity, a couple of schemes tune the receiver \( C_R \) by either (i) selecting additional capacitance from a capacitor bank (shown in Figure 3.3a) [103] or (ii) adding a variable inductance (from duty-cycling an inductor) in parallel with \( C_R \) (shown in Figure 3.3b) [104]. However, both tuning schemes require additional off-chip components (the capacitive bank or the additional inductor), countering the aim of micro-system integration. Additionally, resolution for the capacitive bank and tuning range for both schemes limit the extent to which the resonant frequency of the filter matches that of the \( v_{EMF,R} \) drive frequency.

Figure 3.3. Self-tuning schemes for resonant receiver: (a) capacitive bank and (b) variable inductance.
3.1.2 Resonant Voltage Rectifiers

Once boosted by the high-$Q$ filter, a voltage-mode rectifier transfers power to $C_{RECT}$ when $v_{BOOST}$ surpasses the rectifier’s threshold, $V_{TR}$. The diode-implemented half-wave voltage rectifier in Figure 3.4a, transfers power through the diode, $D_R$, into $C_{RECT}$ only when $v_{BOOST}$ is larger than $V_{RECT} + V_D$, where $V_D$ is the diode voltage. Additionally, as the current sent to $C_{RECT}$ flows through $D_R$, the efficiency of the rectifier reduces to

$$\eta_{HW} = \frac{i_{RECT}V_{RECT}}{i_{RECT}V_{RECT} + i_{RECT}V_D} = \frac{V_{RECT}}{V_{RECT} + V_D},$$

so that reducing $V_D$ is crucial for efficiency. Full-wave rectifiers are more frequently used in the literature [89, 105-110], as shown in Figure 3.4b, as they transfer energy to $C_{RECT}$ twice as often as the half-wave rectifier. They send power to the $C_{RECT}$ during the positive half of $v_{BOOST}$ through diodes $D_T^+$ and $D_B^+$ and during the negative half of $v_{BOOST}$ through $D_T^-$ and $D_B^-$. The voltage threshold of the full-wave rectifier is

$$V_{TR(FW)} = V_{RECT} + 2V_D.$$  \hspace{1cm} (3.5)

Similar to the half-wave rectifier, the efficiency is

$$\eta_{FW} = \frac{i_{RECT}V_{RECT}}{i_{RECT}V_{RECT} + i_{RECT}2V_D} = \frac{V_{RECT}}{V_{RECT} + 2V_D},$$

so that again, reducing $V_D$ is crucial for efficiency. The Delon voltage doubler or bridge voltage doubler, shown in Figure 3.4c, uses both halves of $v_{BOOST}$ to develop double the voltage at $C_{RECT}$. During the positive phase $D_T^+$ conducts through $C_{RECT}^+$, similar to the half-wave rectifier, and during the negative phase $D_T^-$ and $C_{RECT}^-$ conduct to develop a $V_{RECT}$ that is double that of the half-wave rectifier and has a threshold of

$$V_{TR(VD)} = \frac{V_{RECT}}{2} + V_D.$$  \hspace{1cm} (3.7)
The efficiency for the doubler is the same as that of the half-bridge (as the doubler is really just a negative extension of the half-wave rectifier); both of which have higher efficiencies than that of the full-wave rectifier.

![Diagrams](image)

**Figure 3.4.** (a) Half-wave, (b) full-wave, and (c) voltage-doubler rectifiers.

To increase efficiency, Schottky diodes can replace P-N diodes to reduce the diode voltage drop from roughly 0.7 V to 0.3 V as in [89], although for a standard N-well CMOS process, Schottky diodes are not available. Also, while the P-substrate to N⁺-diffusion diode and the P⁺-diffusion to N-well to P-substrate (PNP) are available, their use as power diodes is seldom as both introduce current into the substrate, which could potentially produce latch-up and debiasing issues. As such, diode connected MOSFETs have been used to rectify, as in Figure 3.5a [87, 111-114]. The top pair of PMOS, \(MP_T^+\) and \(MP_T^-\), represent the top pair of diodes, \(DT^+\) and \(DT^-\), in the full-wave rectifier. They begin conducting when their source-gate voltage exceeds the MOS threshold voltage, \(V_{TH}\) (\(V_{TH}\) corresponds to the voltage required to invert the channel of a MOSFET and is not related to \(V_{TR}\), which is the threshold voltage for a particular rectifier). Their MOSFET voltage drop, \(V_{MOS}\), is equal to \(V_{TH} + V_{DS(SAT)}\), where \(V_{DS(SAT)}\) is the overdrive voltage required to conduct the current. To reduce \(V_{DS(SAT)}\) their width-to-length ratios are usually made as large as area permits. Additionally, the gate-coupled or latch NMOS pair on the bottom act as \(DB^+\) and \(DB^-\), although their operation is more similar to a switch. Unfortunately for the top pair of PMOS, if their source-drain voltage exceeds the emitter-base turn-on voltage of the parasitic vertical PNP, then the substrate BJT will steer...
current away and sink it into the substrate. As such, Figure 3.5b has a PMOS bulk-picking circuit [111, 113] in which the bulk of the PMOS is isolated and MP\textsubscript{P1} and MP\textsubscript{P2} pick the higher of the two voltages. Although using additional PMOS seems counterproductive, because the bulk connection is isolated, even if neither MP\textsubscript{P1} nor MP\textsubscript{P2} turn on and the parasitic BJT does conduct, the BJT’s base current will charge the bulk capacitance to turn itself off. Besides protection from the parasitic BJT, the bulk picker also reduces the body effect of the power PMOS (MP\textsubscript{T+} or MP\textsubscript{T−}).

Figure 3.5. Full-wave rectifier using (a) diode-connected PMOS and a latch NMOS pair, along with the (b) bulk-picking implementation.

Both diodes and diode-connected MOSFETs can be used as rectifying elements, but both have turn-on voltages (V\textsubscript{D} and V\textsubscript{MOS}) that increase losses and reduce efficiency. The use of a self-synchronized switch allows the MOSFET to act as a switch during conduction, as shown in Figure 3.6a. The self-synchronizing switch reduces the V\textsubscript{MOS} turn-on voltage to the ohmic voltage drop associated with the MOSFET’s triode resistance, which is considerably less than V\textsubscript{MOS}. The comparator, CP\textsubscript{R}, compares V\textsubscript{RECT} with v\textsubscript{BOOST}. When v\textsubscript{BOOST} is greater than V\textsubscript{RECT} the switch engages to conduct current to C\textsubscript{RECT}, otherwise the switch is off. The self-synchronizing switch has the following non-
idealities: (i) $CP_R$’s delay and offset can lead to the missed opportunity of rectifying when $v_{BOOST}$ just exceeds $V_{RECT}$ and (ii) the delay and offset can lead to reverse discharging of $C_{RECT}$ when $v_{BOOST}$ falls below $V_{RECT}$. From the design prospective, $CP_R$’s input common mode range (ICMR) must be wide enough to encompass $V_{RECT}$’s voltage range and the quiescent power losses should not negate the power benefits of using the self-synchronized switch. Besides comparator implementation, a transformer-based implementation can be used to drive the switches [115], as shown in Figure 3.6b. Here, the transformer’s secondary winding has been separated, one for power transmission and the other for switch synchronization. Note, that $R_{DAMP}$ ensures an overdamped response of the $RLC$ circuit comprising of $R_{DAMP}$, $L_{SYNC}$, and gate-source capacitance of $M_R$ to remove any ringing from $M_R$’s gate. While this technique avoids the quiescent power requirement, the scheme is sensitive to the amplitude of the $v_{BOOST}$ voltage. As such, the transformer’s turn ratios must be chosen to synchronize MOSFET turn-on with conduction to the output, otherwise the MOSFET may preemptively turn on to discharge the output or the MOSFET may not turn on at all in which case the body diode would need to conduct the current.

Figure 3.6 (a) Half-wave rectifier using a self-synchronizing switch and (b) voltage doubler using a transformer to synchronize diode-switch.

### 3.1.3 Resonant Current Rectifier

Figure 3.7 shows a resonant receiver utilizing current rectification [90], where the $L_{R}-C_R$ tank is tuned to resonate with $v_{EMF,R}$. When $S_{RES}$ is closed, inductor current, $i_L$, resonantly...
builds. Power transfer occurs by steering positive $i_L$ current into $C_{RECT}$. Specifically, $S_{RES}$ opens during a negative-to-positive $i_L$ transition, directing $i_L$ through $D_R^+$ and into $C_{RECT}$ during de-energizing time $\tau_{DE}$. Once the de-energizing event completes, $S_{RES}$ closes again in preparation for the next cycle. During the energizing time, the circuit again resonantly builds, extracting energy from $v_{EMF,R}$ equal to that of the energy transferred to $C_{RECT}$ in the last cycle (during steady-state). Current rectification circumvents threshold limitations of conventional voltage-mode rectifiers, so that the resonant current rectifier’s minimum threshold is dependent on the power losses (i.e., $P_{EMF,R} = P_{LOSS}$). Additionally, as is the case for all resonant receivers, input-referred threshold and power extraction from $P_{EMF,R}$ are drastically sensitive to frequency variation and therefore require tuning to preserve these benefits.

![Resonant Current Rectifier](image)

Figure 3.7. Resonant current rectifier (a) schematic and (b) corresponding time-domain waveforms.

### 3.2 Voltage Multipliers

Instead of using $L_R$-$C_R$ resonance to boost $v_{EMF,R}$, voltage multipliers use a cascade of voltage rectifiers that build upon each other. Each stage builds a quasi-dc voltage onto its capacitor, which acts as a stepping-stone for the consecutive stage to build its own voltage. The single-stage voltage multiplier (or Greinacher circuit), shown in Figure 3.8a, deposits charge onto $C_D$ during the negative-half cycle of $v_{AC}$ and then transfers that charge to $C_{RECT}$ during the positive-half cycle (during steady-state). During the negative-half cycle, $C_D$ charges to $|V_{ac}| - V_D$, where $|V_{ac}|$ is the amplitude of $v_{AC}$. As such, $C_D$ acts
as a temporary battery during the positive-half cycle, in which $v_{AC}$ plus this $C_D$ battery can charge $C_{RECT}$ to

$$V_{RECT} = 2|v_{ac}| - 2V_D.$$  \hfill (3.8)

The charge pump feature allows $V_{RECT}$ to be potentially boosted above $|v_{ac}|$ (given that $|v_{ac}|$ is larger than a diode voltage). A CMOS implementation is shown in Figure 3.8b, where the diodes are replaced with diode-connected MOSFETs.

By cascading the single-stage cells, the $N$-stage multiplier shown in Figure 3.8c increases $V_{RECT}$ to

$$V_{RECT} = 2N\left[\frac{C_R}{C_R + C_P} |v_{ac}| - V_D - \frac{I_O}{f(C_R + C_P)} \right],$$  \hfill (3.9)

where the $I_O$ term accounts for the output loading current and $C_P$ is the parasitic capacitance on each pumping node [116]. Alternatively, the input-referred threshold for a given $V_{RECT}$ is

$$V_{TR(VM)} = \left(1 + \frac{C_P}{C_R} \right) \left( \frac{V_{RECT}}{2N} + V_D \right),$$  \hfill (3.10)

and while increasing the number of stages decreases $V_{TR(VM)}$, $V_D$ fundamentally limits the input-referred threshold. Maximum power extraction takes place when all of the pumping
capacitors draw half of their maximum allowed charge or equivalently when product $I_0 V_{RECT}$ is maximized, namely,

$$P_{EMF,R(MAX)} = I_0 V_{RECT} \left. \frac{\partial (I_0 V_{RECT})}{\partial I_0} \right|_{I_0=0} = \frac{N}{2} \left( C_R + C_P \right) \left( \frac{C_R}{C_P + C_R} |V_{ac}| - V_D \right)^2 f_o. \quad (3.11)$$

To extract more energy per cycle, larger pumping capacitors or more pumping capacitors (i.e., number of stages) are required. While use of off-chip capacitors aid in power extraction, they counter the goal of micro-system integration.

As $V_{RECT}$ is limited by the $V_D$ and $V_{MOS}$ for the diode and diode-connected MOSFET case, respectively, technology options such as Schottky diodes and zero-$V_{TH}$ transistors have been exploited [117, 118]. Additionally, the following circuit techniques, shown in Figure 3.9, also reduce the turn-on voltage: (i) $V_{TH}$ distributer [119, 120], (ii) mirrored threshold [116, 121], (iii) pseudo-floating-gate transistors [122], and (iv) threshold self-compensation [80].

![Circuit diagrams](image)

Figure 3.9. Threshold reduction techniques: (a) $V_{TH}$ distributer, (b) mirrored threshold, (c) pseudo-floating-gate transistors, and (d) threshold self-compensation.
Techniques (i)-(iii) effectively place a $V_{TH}$ voltage between the gate-drain terminals to reduce the turn-on voltage of the diode-connected MOSFETs and the dissipated losses through them. The (i) $V_{TH}$ distributer places a $V_{TH}$ voltage onto a flying capacitor that charges another capacitor connected between the gate-drain terminals, $C_{TH}$, to a voltage of $V_{TH}$. Similarly, the (ii) mirrored threshold technique uses the gate-source voltage of bias MOSFETs ($MN_B^-$ and $MP_B^+$) and places that voltage over the gate-drain terminals of the power MOSFET devices ($MN_R^-$ and $MP_R^+$). In (iii) floating gates are used to program a threshold voltage across a MOSFET-capacitor, this technique requires an initialization time to program the voltages. In (iv) the gate is biased with higher stage output voltages. While all these techniques reduce the effective threshold of the MOSFET diode, reverse leakage current limits the number of stages to 5–16 [80, 116, 118, 120], as higher stages lead to plummeting efficiencies.

### 3.3 Inductive Rectifying

Hitherto, the previous rectifiers have had input-referred voltage thresholds defined by their voltage-mode rectifiers (except, the resonant current rectifier). Instead, by building current in an inductor from the low induced voltage (i.e., $v_{EMF.R}$) and then directing it to a battery, inductive rectifiers circumvent threshold limitations of conventional voltage-mode rectifiers by current-mode rectification. The discontinuous-conduction-mode (DCM) boost converter in Figure 3.10 acts as a didactic example for the current rectification. When $S_{EN}$ is closed, $v_{EMF.R}$ falls over $L_{EXT}$ and $L_R$ to build current $i_{EN}$ in the inductors. As the inductors current, $i_L$, must continue flowing when $S_{EN}$ opens, the diode $D_R^+$ conducts $i_L$ so that the current redirects or rectifies into $C_{RECT}$. $L_{EXT}$ and $L_R$ act as intermediaries of power transfer and they build current during the energizing phase ($S_{EN}$ closed) and rectify it during the de-energizing phase ($S_{EN}$ open). As the inductors guide current into $C_{RECT}$, the inductive rectification circumvents conventional voltage
thresholds. However, if the power drawn from $v_{EMF,R} (P_{EMF,R})$ is negated by the converter losses ($P_{LOSS}$), then no additional power transfers to $C_{RECT}$. As such,

$$P_{EMF,R} > P_{LOSS} = P_Q + P_C + P_{SW}$$  \hspace{1cm} (3.12)

must be overcome for power transfer, where the power losses are comprised of quiescent losses ($P_Q$), conduction losses ($P_C$), and switching losses ($P_{SW}$). Overcoming Equation (3.12) and reducing the equivalent input-referred threshold amounts to minimizing the power losses.

![Figure 3.10. Inductive rectifying implemented by the (a) boost converter circuit with (b) the corresponding time-domain waveforms.](image)

The DCM boost converter in Figure 3.10 only delivers power when $v_{EMF,R}$ is positive, Figure 3.11a illustrates an example in which both halves of $v_{EMF,R}$ deliver power [123]. Here, $L_{EXT}^+, MN_B^+, D_T^+$, and $C_{RECT}^+$ construct the boost converter when $v_{EMF,R}$ is positive and $L_{EXT}^-, MN_B^-, D_T^-$, and $C_{RECT}^-$ construct the boost converter when $v_{EMF,R}$ is negative, so that from symmetry, a positive ($V_{RECT}^+$) and a negative ($V_{RECT}^-$) voltage form. This embodiment energizes $L_{EXT}$ and $L_R$ during a fixed on-time, $\tau_{EN}$, followed by full de-energizing of $L_{EXT}$ and $L_R$, at which point a zero current detect restarts the energizing phase so that the converter operates at the boundary of continuous conduction mode (CCM) and discontinuous conduction mode (DCM), shown in Figure 3.11b.
Additionally, this converter operates at a switching frequency that is much faster than the \( v_{\text{EMF},R} \) operating frequency (i.e., \( \tau_{\text{EN}} + \tau_{\text{DE}} \ll T_O \)), so that the \( v_{\text{EMF},R} \) voltage appears quasi-dc across a switching cycle. As such, \( i_{\text{AC}} \) in Figure 3.11b has a triangular waveform with peaks that are proportional to the instantaneous \( v_{\text{EMF},R} \) voltage. These triangular peaks trace out \( i_{\text{AC}}'s \) envelope, \( I_{\text{ac(env)}} \), which equals

\[
I_{\text{ac(env)}} = \frac{V_{\text{emf},R} \tau_{\text{EN}}}{(L_{\text{EXT}} + L_R)}.
\]  

(3.13)

\( i_{\text{AC}}'s \) fundamental component, \( I_{\text{ac(1)}} \), is also proportional to the instantaneous \( v_{\text{EMF},R} \) voltage, because \( I_{\text{ac(1)}} \) simply equals half of \( I_{\text{ac(env)}} \). Then, as \( I_{\text{ac(1)}} \) and \( V_{\text{emf},R} \) are completely in-phase and have amplitudes that track with one another, this converter emulates resistive loading of \( v_{\text{EMF},R} \). Furthermore, the power extracted from \( v_{\text{EMF},R} \) for this case is

\[
P_{\text{EMF},R} = \frac{1}{2} V_{\text{emf},R} I_{\text{ac(1)}} = \frac{1}{2} V_{\text{emf},R} \left[ \frac{V_{\text{emf},R} \tau_{\text{EN}}}{2(L_{\text{EXT}} + L_R)} \right] = \frac{1}{4} \left( \frac{V_{\text{emf},R}^2 \tau_{\text{EN}}}{L_{\text{EXT}} + L_R} \right),
\]

(3.14)

and is independent of \( v_{\text{EMF},R} \)'s frequency (given a fast enough switching frequency, viz., \( \tau_{\text{EN}} + \tau_{\text{DE}} \ll T_O \)). Unfortunately, this technique requires two additional inductors and Schottky diodes.

Figure 3.11. Dual-polarity boost converter (a) schematic and (b) corresponding time-domain waveforms.

In another inductive rectifier topology, the pickup coil’s self-inductance is re-utilized as the main power inductor, shown in Figure 3.12a [124, 125]. The converter is driven with a constant pulse width modulated (PWM) signal, \( S_{\text{EN}} \) in Figure 3.12b, so that
during the energizing time switches $MN_B^-$ and $MN_B^+$ short the transformer’s secondary allowing $v_{EMF,R}$ to fall over $L_R$ while building inductor current, $i_L$. When the MOSFETs open, $i_L$ must continue flowing and reroutes to conduct through the diodes and into $C_{RECT}$. Depending on the polarity of $i_L$ (i.e., the polarity of $v_{EMF,R}$) either positive conducting diodes $D_T^+$ and $D_B^+$ or negative conducting diodes $D_T^-$ and $D_B^-$ channel energy into $C_{RECT}$. If the de-energizing time is small, or equivalently $|V_{emf,R}| << V_{RECT}$, then $i_L$’s fundamental component is in phase and corresponds with resistive loading. While resistive emulation is ideal for removing reactive loading, the switching frequency of the converter must be higher than that of the operating frequency (i.e., $\tau_{EN} << T_O$). The higher switching frequency comes with increased switching losses ($P_{SW}$) and decreased power extraction ($P_{EMF,R}$ from Equation (3.14)), both of which increase the input-referred threshold.

Figure 3.12. Dual-polarity transformer-based boost converter (a) schematic and (b) corresponding time-domain waveforms.

The transformer in Figure 3.12a also aids in start-up. When $V_{RECT}$ is insufficient to drive $MN_B^-$ and $MN_B^+$ (start-up condition), both MOSFETs are off so that $D_T^+, D_T^-$, and the MOSFET body diodes construct a diode-bridge rectifier and the transformer aids in voltage rectifying by boosting $v_{EMF,R}$ by the turns-ratio $n$. Unfortunately, the addition of a transformer is not practical from an integration perspective.
3.4 Comparison

Table 3.1 shows a quantitative summary and comparison of the studied rectifiers based on the following criteria: integration, input-referred threshold, frequency sensitivity, power extraction and battery-less startup. While resonant receivers extract the most power, they are highly sensitive to frequency. Additionally, resonant receivers’ input-referred threshold, while potentially low, critically depends on the quality factor of the pickup coil. Voltage multipliers on the other hand, exhibit low frequency sensitivity, but lack in efficiency and input-referred threshold. Voltage multipliers are most typically used in RF harvesting (far-field) or in the GHz arena, as their power extraction is proportional to frequency, as found in Equation (3.11). Inductive charging has the lowest frequency sensitivity as well as low input-referred threshold, but suffers from low to moderate power extraction. However, with the reuse of the coil inductor as the power inductor, power extraction is higher and system integration is highest.
### Table 3.1 Comparison of Low Voltage Rectifiers

<table>
<thead>
<tr>
<th>Integration</th>
<th>Input-Reflected Threshold</th>
<th>Frequency Sensitivity</th>
<th>Power Extraction $P_{EMF,R}$</th>
<th>Battery-less Start-up</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Voltage Rectifier</strong></td>
<td>$V_{TR} \over Q_R$</td>
<td>Limited by LC-filter bandwidth: $\Delta \omega_{MAX} = \frac{\omega_R}{Q_R}$</td>
<td>$V_{conf,r} \over V_{C(MAX)}$</td>
<td>Yes</td>
</tr>
<tr>
<td><strong>Resonant Receivers</strong></td>
<td></td>
<td></td>
<td>$\over 2\omega_L R$</td>
<td></td>
</tr>
<tr>
<td><strong>Voltage Rectifier</strong></td>
<td>$V_{TR} \over Q_R$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Resonant Rectifier and tuning</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>With Self-Tuning</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Current Rectifier</strong></td>
<td>$V_{RECT} + V_D \sin \left( \frac{2\pi \tau_{EN}}{T_0} \right)$</td>
<td>Limited by LC-filter bandwidth: $\Delta \omega_{MAX} = \frac{\omega_R}{Q_R}$</td>
<td>$\over 2\pi R$</td>
<td>No</td>
</tr>
<tr>
<td><strong>Voltage Rectifier</strong></td>
<td>$V_{TR} \over Q_R$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>With Self-Tuning</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>On-Chip Pumping Capacitors</strong></td>
<td>$1 + C_P \over C_R \left( V_{RECT} + V_D \right)$</td>
<td>$P_{EMF,R} \propto f_O$</td>
<td>$N \over 2 \left( C_R + C_P \left( \frac{C_R}{C_P} - V_{conf,r} - V_D \right) \right)^2 f_O$</td>
<td>Yes</td>
</tr>
<tr>
<td><strong>Off-Chip Pumping Capacitors</strong></td>
<td>$1 + C_P \over C_R \left( V_{RECT} + V_D \right)$</td>
<td>$P_{EMF,R} \propto f_O$</td>
<td>$N \over 2 \left( C_R + C_P \left( \frac{C_R}{C_P} - V_{conf,r} - V_D \right) \right)^2 f_O$</td>
<td>Yes</td>
</tr>
<tr>
<td><strong>Inductive Charging</strong></td>
<td>$4P_{LOSS}(L_R + L_{EXT}) \over \tau_{EN}$</td>
<td>Only $P_{LOSS}$ is frequency sensitive, with $P_{SW} \propto f_O$</td>
<td>$\over 4(L_{EXT} + L_R)$</td>
<td>No</td>
</tr>
<tr>
<td><strong>Using External Inductor</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Reusing Pickup Coil’s Self-Inductance</strong></td>
<td>None</td>
<td>Only $P_{LOSS}$ is frequency sensitive, with $P_{SW} \propto f_O$</td>
<td>$\over 4L_R$</td>
<td>No</td>
</tr>
</tbody>
</table>

1 $V_{TR}$ refers to the voltage threshold of the voltage rectifier placed after the high-Q filter.

2 $V_{C(MAX)}$ corresponds to the maximum $C_R$ voltage, typically limited by the voltage rectifier.
CHAPTER 4

PROPOSED LOW-EMF INDUCTIVELY-COUPLED POWER RECEIVER

Although all the low voltage rectifiers have their respective benefits, inductive rectifiers offer a low input-referred threshold, the least sensitivity to frequency, and a high efficiency. In the proposed wireless power receiver–battery charger system, an inductive rectifying scheme that increases extracted power from the induced $v_{EMF,R}$ source, while decreasing converter losses is introduced. The combination of increased power extraction and decreased losses reduces the input-referred threshold to unprecedented values for inductive rectifiers. Furthermore, as the pickup coil’s self-inductance is used as the power inductor in the rectifying scheme, micro-scale system implementation is achievable.

4.1 Proposed Inductive Rectifying Scheme

The proposed inductive rectifying scheme for a wireless power receiver–battery charger system draws more power from the $v_{EMF,R}$ source than that of prior art inductive rectifiers. The scheme achieves this by extending the energizing time to allow more current to build onto the inductor prior to de-energizing it into $V_{RECT}$. As shown in Figure 4.1 the energizing time extends to cover most of $v_{EMF,R}$’s half cycle, so that there is only one energizing and de-energizing event for both the positive-half and negative-half cycle of $v_{EMF,R}$. During the positive energizing time, $\tau_{EN}^+$, which corresponds to the vast majority of the positive-half cycle of $v_{EMF,R}$ (i.e., $\tau_{EN}^+ \approx T_o/2$), switches $S_N^+$ and $S_N^-$ are closed so that the $v_{EMF,R}$ source energizes the coil’s self-inductance, $L_R$, by building its peak current to

$$\Delta i_L = \int_0^{\tau_{EN}^+} \frac{\left| V_{emf,r} \right| \sin(2\pi f_o t)}{L_R} dt \approx \int_0^{T_o/2} \frac{\left| V_{emf,r} \right| \sin(2\pi f_o t)}{L_R} dt = \frac{V_{emf,r}}{\pi f_o L_R},$$

(4.1)
graphically shown in Figure 4.1a. The energy in $L_R$ at the end of the positive energizing time (assuming no losses) is then

$$E_L = \frac{1}{2} L_R \Delta i_L^2 = \frac{|V_{emf,R}|^2}{2\pi^2 f_0^2 L_R}. \quad (4.2)$$

![Diagram of proposed inductive rectifying scheme through positive energizing, positive de-energizing, negative energizing, and negative de-energizing times.](image)

Figure 4.1. Proposed inductive rectifying scheme through the (a) positive energizing, (b) positive de-energizing, (c) negative energizing, and (d) negative de-energizing times.

At the end of the positive energizing time, switch $S_N^+$ opens so that positive half-cycle inductor current, $i_L^+$, redirects through the diode $S_D^+$ and into $V_{RECT}$ during the positive de-energizing time, $\tau_{DE}^+$, shown in Figure 4.1b. The diode remains conducting until all of $L_R$'s current and energy transfers into $V_{RECT}$. Subsequently, the negative
energizing time, $\tau_{EN^-}$, begins by closing $S_N^+$ so that now a negative valued $v_{EMF,R}$ energizes $L_R$, as shown in Figure 4.1c. The direction of current during the negative half-cycle, $i_L^-$, is the reverse of that during the positive half-cycle, as $v_{EMF,R}$ is now negative and naturally arises from the symmetry of the circuit. Again, the inductor builds current (and energy) throughout the cycle, until $i_L^-$ reaches its peak value of $\Delta i_L$. Finally, $S_N^-$ opens, beginning the negative de-energizing time, $\tau_{DE^-}$, and directing $i_L^-$ through diode $S_D^-$ and into $V_{RECT}$, as illustrated in Figure 4.1d. The de-energizing time and full-cycle complete when $L_R$’s current and energy transfer into $V_{RECT}$. After completing the full-cycle, the operation begins anew with the start of another cycle. Figure 4.2 displays the inductor waveform as it energizes and de-energizes throughout the full-cycle as well as the rectified current, $i_{RECT}$, flowing into $V_{RECT}$.

![Figure 4.2](image_url)

**Figure 4.2.** (a) Inductive rectifying circuit with (b) corresponding time-domain waveforms.

The proposed rectifier draws energy from $v_{EMF,R}$ and stores it in $L_R$ prior to rectifying the energy into $V_{RECT}$. As the energy is extracted twice during the completion of one cycle (once during the positive-half cycle and once during the negative-half cycle), the power sourced by $v_{EMF,R}$ is then

$$P_{EMF,R} = \frac{2E_L}{T_o} = \frac{1}{T_o} \left( \frac{V_{emf,r}^2}{2\pi^2 f_o^2 L_R} \right) = \frac{V_{emf,r}^2}{\pi^2 f_o L_R}.$$  \hspace{1cm} (4.3)

The energy transferring process from $v_{EMF,R}$ to $L_R$ and from $L_R$ to $V_{RECT}$ incurs losses, $P_{LOSS}$, so that the net power sent to $V_{RECT}$ is then
\[ P_{\text{RECT}} = P_{\text{EMF,R}} - P_{\text{LOSS}}, \quad (4.4) \]

As is the case for inductive rectifiers, there is no conventional voltage threshold to overcome, however, if the power drawn from \( v_{\text{EMF,R}} \) is negated by the converter losses, then no additional power is delivered to \( V_{\text{RECT}} \), so that

\[ P_{\text{LOSS}} < P_{\text{EMF,R}} = \frac{|v_{\text{emf,r}}|^2}{\pi^2 f_0 L_R}, \quad (4.5) \]

ensures power delivery. The proposed scheme eases this condition by extracting more power from the \( v_{\text{EMF,R}} \) source than that of prior art inductive rectifiers. Additionally, Equation (4.5) suggests that there is a minimum \(|V_{\text{emf,r}}|\) required for net power delivery and that \(|V_{\text{emf,r}}|\) value corresponds to the effective threshold of the rectifier, which is

\[ V_{\text{TR}} = \pi \sqrt{P_{\text{LOSS(MIN)}} f_0 L_R}. \quad (4.6) \]

Here, \( P_{\text{LOSS(MIN)}} \) corresponds to the power losses when \(|V_{\text{emf,r}}|\) is just at the threshold (i.e., \(|V_{\text{emf,r}}| = V_{\text{TR}}\)). Specification of \( P_{\text{LOSS(MIN)}} \) is necessary, as \( P_{\text{LOSS}} \) depends on input power levels, \( P_{\text{EMF,R}} \), as is usually the case for switched-inductor converters. The reduction of \( V_{\text{TR}} \), then amounts to decreasing \( P_{\text{LOSS(MIN)}} \), so that decreasing \( P_{\text{LOSS(MIN)}} \) is one of the most fundamental challenges for low-voltage rectification. As such, a low power loss implementation of the proposed scheme is just as central as the scheme itself.

### 4.2 Wireless Power Receiver Circuit

#### 4.2.1 Low Power-loss Implementation

A low power loss implementation of the proposed inductive rectifying scheme reduces the effective threshold (i.e., \( V_{\text{TR}} \)) and increases receiver efficiency. As such, the following circuit techniques aid in achieving low power losses: (i) replacing de-energizing diodes with self-synchronized switches (\( S_{D^+} \) and \( S_{D^-} \)), (ii) enabling and disabling circuit blocks when they are not needed, and (iii) using soft switching techniques to reduce current-
voltage overlap losses incurred during commutations. Figure 4.3 depicts the wireless power receiver circuit implementing the proposed inductive rectifier scheme with the above mentioned low power loss circuit techniques. The wireless power receiver circuit is comprised of energizing CMOS switches $M_N^+$, $M_N^-$, positive de-energizing self-synchronizing switch $M_P^+$ with its corresponding comparator $C_{PD^+}$, and negative de-energizing self-synchronizing switch $M_P^-$ with its corresponding comparator $C_{PD^-}$. The gate-driving voltages of $M_N^+$, $M_N^-$, $M_P^+$, and $M_P^-$ are with respect to $V_{RECT}$ and ground, which is sufficient voltage to drive the switches into triode and produce low channel resistances.

![Diagram](image)

**Figure 4.3. Low power loss implementation of the proposed inductive rectifier scheme.**

The self-synchronizing switch replaces the de-energizing diode with a voltage monitoring comparator and PMOS switch, as shown in Figure 4.3, so that the conventional diode drop of 0.7 V reduces to the ohmic voltage drop of the PMOS’s triode resistance, which is on the order of millivolts. To facilitate operation, comparator $C_{PD}$ monitors $v_{DS}$ of $M_P$ and when $v_{SW}$ rises above $V_{RECT}$, $C_{PD}$ outputs a digital LOW signal to drive $M_P$ on and allow current to flow into $V_{RECT}$; as in the ideal diode case. Similarly, when $v_{SW}$ falls below $V_{RECT}$, $C_{PD}$ outputs a digital HIGH signal to drive $M_P$ off and prevent current from flowing out of $V_{RECT}$. As the comparator only needs to be on during
the de-energizing time, duty cycling the comparator reduces its quiescent power consumption. As such, the comparator is enabled just prior to when the self-synchronizing switch will be part of the conduction path and disabled just after. When disabled, the comparator sets its output HIGH so that $M_P$ is off and the comparator disconnects all its high-power-consuming current branches.

An additional benefit of self-synchronizing switches is how they lend themselves to soft switching. Soft-switching occurs when the current flowing through and/or the voltage across a MOSFET switch is roughly zero to reduce current-voltage overlap losses. To begin with, only the positive half-cycle commutations necessitate investigation, as the negative half-cycle is symmetric. As such, the negative switching node is grounded, as is the case during the positive half-cycle and is shown in Figure 4.4a. In addition, the parasitic capacitance on node $v_{SW}^+$ aids in soft switching and is lumped into $C_{PAR}$. The lumped $C_{PAR}$ consists of the parasitic capacitance of the coil windings, $(C_{PAR,R})$, the gate-drain capacitance of $M_N^+$, and gate-drain capacitance of $M_P^+$. The parasitic capacitance on the node, as the name suggests, would normally drain energy from the system, but when used with soft switching reduces power losses.

Figure 4.4b shows the first commutation in the positive half-cycle when $\tau_{EN}^+$ transitions to $\tau_{DE}^+$. The commutation begins when $M_N^+$ disengages with $v_{SW}^+$ held low by $C_{PAR}$, resulting in a zero voltage switching (ZVS) event. The ZVS implies minimal current-voltage overlap losses incurred in switch $M_N^+$. With $M_N^+$ opened, $i_L$ continues flowing and inductively charges $C_{PAR}$ during the commutation. This inductive charging of the node is almost lossless, as opposed to the conventional hard switching of a node. The inductor continues transferring energy into $C_{PAR}$ until $v_{SW}^+$ rises above $V_{RECT}$ triggering the self-synchronizing switch $S_D^+$. The comparator’s positive-edge trip-point is designed to be slightly above $V_{RECT}$ for an increase in noise immunity. Additionally, the comparator should also respond quickly so that $v_{SW}^+$ does not continue to rise, because the rising voltage of $v_{SW}^+$ could forward bias the parasitic P$^+$ diffusion to N-well to P-
substrate BJT present in the self-synchronizing $M_{p}^+$ PMOS switch. As such, the comparator’s positive-edge delay is designed to be fast enough to avoid allowing the BJT to forward bias and otherwise let current flow into the substrate. After the self-synchronizing switch responds without forward biasing the substrate BJT, the inductor current now flows through $S_{D}^+$ and into $V_{RECT}$ to conclude the $\tau_{EN}^+$ to $\tau_{DE}^+$ commutation.

Figure 4.4. (a) Circuit configuration during the positive-half cycle and (b) soft-switching waveforms during the positive-half cycle commutations.
It is important to note that at the end of the de-energizing cycle $M_P^+$ should only disengage after $L_R$ de-energizes all of $i_L$ into $V_{RECT}$. Instead, if $L_R$ had positive flowing $i_L$ when $M_P^+$ disengaged, then $i_L$ would be re-directed to again flow into the $v_{SW}^+$ node until the voltage on the node grew to re-trigger the self-synchronizing switch’s comparator and re-engage $M_P^+$. This back and forth between engaging and dis-engaging of $M_P^+$, would lead the system into oscillations until $i_L$ finally depleted. During these oscillations, the charging and discharging of the $M_P^+$ gate would lead to undesirable gate charging losses. Therefore, a negative trip-point $V_{TRIP}^-$ is added to $CP_D$ to ensure that even with random offset at the input to the comparator, all of $i_L$ de-energizes into $V_{RECT}$, to altogether avoid the oscillations. However, as the negative trip-point is now slightly below $V_{RECT}$, $i_L$ will marginally reverse its direction before the comparator disengages the de-energizing PMOS switch. Still, as the energy taken from $V_{RECT}$ during this reverse conduction transfers to $L_R$ in preparation for the opposite energizing cycle, the system does not incur a net power loss.

The second commutation in the positive half-cycle occurs when $\tau_{DE}^+$ transitions to $\tau_{EN}^-$. The commutation begins when $M_P^+$ opens with $v_{SW}^+$ held just below $V_{RECT}$ with the help of $C_{PAR}$, resulting in ZVS. With $M_P^+$ open, the now negative inductor current inductively discharges $C_{PAR}$ with minimal losses. That is to say, that although some of the inductor’s energy went into charging $v_{SW}^+$ to $V_{RECT}$ during the $\tau_{EN}^+$ to $\tau_{DE}^+$ commutation, most of that energy returns to the inductor during this inductive discharging event. The inductive discharging continues until a crude zero voltage detect (ZVD) re-engages $M_N^+$ to end the $\tau_{DE}^+$ to $\tau_{EN}^-$ commutation. A logic gate input implements the crude ZVD and roughly senses when $v_{SW}^+$ falls below $V_{RECT}/2$, reducing losses to a fourth of the otherwise hard switching energy loss; the fourth factor comes from the energy in $C_{PAR}$ being proportional to $(V_{SW}^+)^2$. The implemented crude ZVD has minimal control costs compared to an actual zero voltage detect scheme using a comparator, where the power cost of implementing the more accurate scheme would undo the benefit of ZVS.
Figure 4.5a depicts the complete wireless power receiver circuit implementing the proposed inductive rectifier scheme. The system includes the previously mentioned NMOS energizing switches, PMOS de-energizing switches, and self-synchronizing comparators. Additionally, the bias generator provides appropriate bias currents for each of the self-synchronizing comparators. The bias generator’s power consumption should be low, as the generator is always on, unlike the duty-cycled comparators. Furthermore, the $v_{EMF,R}$ polarity detector determines the sign of $v_{EMF,R}$ for the purpose of synchronizing energizing and de-energizing events with $v_{EMF,R}$. The detector’s output signal, $S_{EMF,R}$, feeds the synchronizing information to the control logic. Finally, the control logic provides the appropriate gate-driving signals, $S_{GD}^+$ and $S_{GD}^-$, to the energizing switches and comparator enabling signals, $EN^+$ and $EN^-$, to the self-synchronizing switches.

![Wireless Power Receiver Circuit](image)

**Figure 4.5.** (a) Proposed wireless power receiver with (b) corresponding time-domain waveforms.

Figure 4.5b shows the output signals generated from the control logic as well as the input $v_{EMF,R}$ voltage, inductor current, and rectified current waveforms. The $v_{EMF,R}$ polarity detector feeds the following two critical pieces of information to the control logic: (i) the polarity of $v_{EMF,R}$, which allows the control logic to know in which direction $i_L$ is flowing when being energized and (ii) the transition in polarity, which identifies a
zero crossing or equivalently the end of the energizing time. With that information, the control logic knows which energizing switch to disengage and when to do it. After the switch is disengaged, however, the control logic must know when to re-engage the switch for the following energizing half-cycle. As such, two events help in identifying the end of the de-energizing half-cycle: (i) the self-synchronizing switch finishes de-energizing and (ii) the ZVD NOR gate identifies the end of the soft-switching commutation. Event (i) instructs the control logic to proceed with the next energizing half-cycle, but the ZVD NOR gate stalls the instruction until event (ii) allows the instruction to propagate to the gate of the energizing switch. Additionally, as the self-synchronizing switches only need to be enabled when their respective energizing switch is disengaged, the enable signal is just the inverted gate-driving signal for the respective energizing switch, as shown in Figure 4.5b.

4.2.2 Block-Level Implementation

Figure 4.6 shows the implemented comparator topology for both of the self-synchronizing switches. When the comparator is enabled ($S_{EN}$ is HIGH and $S_{DIS}$ is LOW), the fast start-up current mirror sets the current in $M_{PB}$, which in turn creates the bias voltage, $V_{BIASP}$, onto the gates of the common gate pair $M_{P1}$-$M_{P2}$. When $CPD$’s output is HIGH or equivalently when $M_P$ is off, $M_{H}^{+}$ is also off and currents $i_{P1}$ and $i_{P2}$ compare through mirror network $M_{N1}$-$M_{N2}$. A positive trip-point above $V_{RECT}$ increases noise immunity. As such, a two-to-one mirror ratio is chosen so that $M_{P1}$’s source-gate voltage must be larger than that of $M_{P2}$’s to sink twice the current, leading to a higher-than-$V_{RECT}$ positive trip-point. On the other hand, the negative trip-point should be slightly below $V_{RECT}$ to avoid previously described oscillations. As such, once the comparator trips, $M_{H}^{+}$ shorts and $i_{HYST}$ draws 18/32 of $i_{P2}$ to ensure that the mirrored current onto $M_{P1}$ is less than that flowing in $M_{P2}$ for a lower-than-$V_{RECT}$ trip-point. The trip point is quantified as
\[ V_{\text{TRIP}}^- = V_{SG1} - V_{SG2} = V_{TH1} - V_{TH2} + \left( \sqrt{i_{P1}} - \sqrt{i_{P2}} \right) \left( \frac{2}{k'(W/L)_{P1,P2}} \right) \]

\[ = \left( \sqrt{28I_{\text{REF}}} - \sqrt{32I_{\text{REF}}} \right) \left( \frac{2}{k'(W/L)_{P1,P2}} \right) = V_{SD2(SAT)} \left( \sqrt{\alpha_{\text{EFF}}} - 1 \right), \quad (4.7) \]

where \( \alpha_{\text{EFF}} \) is the effective mirror ratio, in this case \( \alpha_{\text{EFF}} = 7/8 \). Ideally, \( V_{\text{TRIP}}^- \) should be temperature independent to maintain the same margin of noise immunity. Unfortunately, the mobility term, the \( k' \) term in Equation (4.7), has a negative temperature coefficient that varies \( V_{\text{TRIP}}^- \) with temperature. As such, \( I_{\text{REF}} \) is designed to be complementary-to-absolute-temperature (CTAT) in an effort to counteract the temperature variation in \( k' \).

Figure 4.6. Schematic of the self-synchronized switch (transistors are in um and NMOS bulk’s are tied to ground).

Advantages of the comparator topology stem from the common gate input pair \( M_{P1}-M_{P2} \), which offer great input common-mode range for comparing larger-than-rail voltages and fast positive-edge response; i.e., reduction of positive-edge delay, \( \tau_{\text{COMP}^+} \). The reduction of \( \tau_{\text{COMP}^+} \) stems from liberating \( M_{P1} \) of slew rate limitations found in
differential amplifiers. During $\tau_{COMP}^+$, when $v_{SW}$ rises above $V_{RECT}$ the source-gate voltage of $M_P^+$ is overdriven from typical bias to briefly source above-bias current. This current expedites comparison by charging $v_{COMP}$ with a faster-than-conventional slew-rate. The reduction in positive-edge delay allows the comparator to be fast enough to avoid forward biasing the parasitic BJTs of $M_P^+$ and $M_P^-$, which would otherwise let current flow into the substrate.

When the comparator is disabled (i.e., $S_{EN}$ is LOW and $S_{DIS}$ is HIGH), all high current branches in $CP_D$ are shut-off, including the $V_{BIASP}$ reference branch, to conserve power. During the enabling of $CP_D$, capacitive coupling through $C_{GD}$ of $M_B$ perturbs $v_{BIASN}$. To respond, the fast start-up current mirror counteracts the perturbation and properly biases current branches prior to the end of the de-energizing time, ensuring correct judgment from $CP_D$. The bandwidth of the response is limited by the pole of $v_{BIASN}$, which is the effective capacitance at node $v_{BIASN} (C_{BIASN})$ and the output impedance of the $v_{BIASN}$ generator ($Z_{BIASN}$). A conventional current mirror acts too slowly ($\omega_{BIASN} \approx g_{m,FB}/C_{BIASN}$) for $CP_D$ to bias in time. Instead, shunt-shunt feedback through $M_{FB}-M_{SF}$ lowers the output resistance of $Z_{BIASN}$ to push out the output pole from $g_{m,FB}/C_{BIASN}$ to $g_{m,SF}(1+LG_{FB})/C_{BIASN}$, where $LG_{FB}$ is the loop gain of the MOSFET beta-helper current mirror. Although $LG_{FB}$ has its own bandwidth limitations, its unity gain bandwidth is still much higher than $\omega_{BIASN}$, which ultimately stems from the effective capacitance at $v_{FAST}$ being much smaller than $C_{BIASN}$. In addition, the flexibility of adjusting $M_{SF}$’s bias current adds opportunity to further increase $g_{m,SF}$ and therefore the output pole. Therefore, when disabled, minimal current ($I_{REF}/2$) flows through $M_{SF}$ to conserve power and to bias values near their enabled operation. When enabled, current through $M_{FB}$ increases to $32.5I_{REF}$, drastically increasing bandwidth to bias $CP_D$ in time to make a decision. As the enable time corresponds to a small fraction of the period, the average power drawn is low.
The 50 nA current reference shown in Figure 4.7 biases the fast start-up current mirror within $CP_D^+$ and $CP_D^-$. The bias current is low to conserve power, as unlike the duty-cycled comparators, the bias generator is always on. The differential amplifier comprised of $M_{IN-}$, $M_{IN+}$, $M_{M-}$, $M_{M+}$, and $M_{TAIL}$, sets the reference current in $R_{BIAS}$ and $Q_{CTAT}$ such that $V_{DIODE}$ and voltage $I_{REF}R_{BIAS}$ equal. $V_{DIODE}$’s large negative temperature coefficient of $-3.59 \times 10^3$ ppm/°C at 27 °C, combined with the low-temperature coefficient $R_{BIAS}$ produce a reference current that is CTAT. The CTAT current reference reduces temperature variation of $V_{TRIP^-}$ by counteracting the $k'$ temperature coefficient of $-2.77 \times 10^3$ ppm/°C at 27 °C. While $V_{TRIP^-}$’s temperature variation still differs, it is reduced. Additionally, the total quiescent current of the reference is 156.25 nA, which including the disabled biasing current of the fast start-up current mirrors (i.e., 900 nA), the total biasing current of the system with comparators disabled, $I_{BI}$ is 1.056 μA.

![Figure 4.7. Schematic of the bias generator (transistors dimensions are in μm and NMOS bulk's are tied to ground).](image-url)
4.2.3 Power-loss Analysis

The wireless power receiver circuit dissipates conduction losses, $P_c$, across series resistances in $i_L$’s conduction path. The resistances are comprised of the winding resistance or ESR of the receiver coil, $R_R$, as well as the channel impedences of switches: $M_{N^+}$, $M_{N^-}$, $M_{P^+}$, and $M_{P^-}$, which are a function of their size (width-to-length aspect ratios) and gate-source voltages. The conduction losses divide into two different conduction times: energizing and de-energizing, with their respective inductor currents $i_{EN}$ and $i_{DE}$ shown in Figure 4.8c-d. The resistance along the energizing path consists of $R_R$ in series with the two n-type channel resistances, $2R_{MN}$, from $M_{N^+}$ and $M_{N^-}$. The energizing conduction losses are then

$$P_{C,EN} = i_{EN(RMS)}^2(R_R + 2R_{MN}),$$  \hspace{1cm} (4.8)

where $i_{EN(RMS)}$ corresponds to the root mean square (RMS) current of $i_{EN}$. Additionally, as the energizing time spans the vast majority of the period, the conduction time can be considered uninterrupted. As such, the energizing $i_L$ waveform can be approximated as the superposition of a sine wave with amplitude $0.5\Delta i_L$ and an orthogonal (90° out of phase) square wave with amplitude $0.5\Delta i_L$. The superposition is as traced out in Figure 4.8e such that

$$i_{EN(RMS)}^2 \approx i_{SQ(RMS)}^2 + i_{SIN(RMS)}^2 = \left(\frac{\Delta i_L}{2}\right)^2 + \left(\frac{\Delta i_L}{\sqrt{8}}\right)^2,$$  \hspace{1cm} (4.9)

where $i_{SQ(RMS)}$ and $i_{SIN(RMS)}$ are the RMS currents corresponding to $i_{SQ}$ and $i_{SIN}$ shown in Figure 4.8e, respectively.
Figure 4.8. Time-domain waveforms of (a) EMF coil voltage, (b) coil current, (c) energizing current, (d) de-energizing current, and (e) decomposition of energizing current into sinusoidal and squarewave components.

There are two de-energizing paths for this circuit. The resistance along the positive half-cycle’s de-energizing path consists of $R_R$ in series with both $R_{MN}$, from $M_N^-$, and $R_{MP}$, from $M_P^+$, where $R_{MP}$ corresponds to a p-type channel resistance. On the other hand, the resistance along the negative half-cycle’s de-energizing path consists of $R_R$ in series with both $R_{MN}$, from $M_N^+$, and $R_{MP}$, from $M_P^-$. Together, both paths dissipate de-energizing conduction losses, $P_{C,DE}$:

$$P_{C,DE} = i_{DE(RMS)}^2 (R_R + R_{MN} + R_{MP}),$$  \hspace{0.5cm} (4.10)

where $i_{DE(RMS)}$ corresponds to the RMS current of $i_{DE}$. The de-energizing current can be viewed as a double pulsed triangular waveform of amplitude $\Delta i_L$ that conducts only during the $2\tau_{DE}$ time. For the rest of the operational period $i_{DE}$ is zero, so that the triangular current waveform only conducts for a $2\tau_{DE}/T_O$ fraction of time and
\[ i_{DE(RMS)}^2 = i_{TRI(RMS)}^2 \left( \frac{2\tau_{DE}}{T_O} \right) = \left( \frac{\Delta i_{ik}}{\sqrt{3}} \right)^2 \left( \frac{2\tau_{DE}}{T_O} \right), \]  

where \( i_{TRI(RMS)} \) is the RMS current of a triangular current waveform that would span the entire period.

The wireless power receiver circuit also dissipates switching losses, \( P_{SW} \), in charging and discharging MOS and other parasitic capacitances. The switching losses associated with the MOS switches usually consist of gate-driving and current-voltage overlap losses, but as the soft-switching techniques minimize current-voltage overlap losses to insignificant values, only gate-driving losses are considered. The size of the switch determines how much gate capacitance (i.e., \( C_G = C_{GS} + C_{GD} + C_{GB} \approx C_{GS} \)) there is and therefore the required gate-driving power. Throughout a full-cycle, each of the MOS switches (\( M_N^+, M_N^-, M_P^+, M_P^- \)) opens and closes once. The collective gate-load capacitance, \( C_T \), is charged and discharged to \( V_{RECT} \) once per period, with gate-driving loss

\[ P_{SW,GD} = C_T \Delta V_G^2 f_o = \left( 2W_N L_N + 2W_P L_P \right) C_{OX}'' V_{RECT}^2 f_o, \]  

where \( C_T \) is the total gate capacitance for all switches.

To reduce parasitic capacitances of the MOS switches, small gate-oxide area and therefore minimum length transistors are adopted. As the width of the transistor also determines the channel resistance for the MOS switches, their selection amounts to a trade-off between conduction and switching losses. Figure 4.9 depicts the averaged losses incurred in both the n-channel and p-channel MOS switches as a function of channel width over the \( |V_{emf,i}| \) range of 30 mV to 150 mV. The compromise between conduction and switching losses occurs at the minimum of this contour plot. As such, the CMOS switches sizes are \( W_N/L_N \) of 1108/0.18 \( \mu \text{m}/\mu \text{m} \) and \( W_P/L_P \) of 368/0.18 \( \mu \text{m}/\mu \text{m} \).
The charging of stray capacitances on nodes $v_{SW}^+$ and $v_{SW}^-$ also requires energy; the stray capacitance on each node is lumped into $C_{PAR}$. During the soft-switching $\tau_{EN}^+$ to $\tau_{DE}^+$ commutation, $L_R$ inductively charges $C_{PAR}$ almost adiabatically (in resonant fashion), and later during the soft-switching $\tau_{DE}^+$ to $\tau_{EN}^-$ commutation, $L_R$ inductively discharges $C_{PAR}$ to absorb most of that energy back. As previously mentioned, the crude ZVD prematurely senses the zero crossing and instead senses when the switching node falls below $V_{RECT}/2$, with some of the energy in $C_{PAR}$ shunted to ground. The power required to charge and discharge both switching nodes once per full-cycle is then equal to the power shunted to ground or

$$P_{SW,PAR} = \left[ \frac{1}{2} C_{PAR} \left( \frac{V_{RECT}}{2} \right)^2 \right] (2f_o) = \frac{C_{PAR} V_{RECT}^2}{4} f_o.$$  \hspace{1cm} (4.13)

The self-synchronizing comparators and the bias generator require quiescent power to operate and that quiescent power splits into two categories: biasing and duty-cycled. The biasing current, $I_{BI}$, is always flowing during the full cycle and consists of the quiescent current in the bias generator and the disabled bias current of the fast start-up current mirror. The quiescent power required for biasing is
The biasing current was designed to be low, as unlike the duty-cycled comparators, the biasing current is always on. The duty-cycled quiescent power consumption differs from the biasing power as the comparators are enabled only during each of their respective de-energizing times. As such, the quiescent power consumption of the comparators reduces by the fraction of the enabling time or equivalently the de-energizing time, viz.,

\[
P_{Q,CP} = I_{CP}V_{RECT} \frac{2\tau_{DE}}{T_O} = \frac{I_{CP}V_{RECT}}{T_O} \left( \frac{2\Delta i_T L_R}{V_{RECT}} \right) = \frac{2I_{CP} |V_{emf,r}|}{\pi},
\]

where, \( I_{CP} \) is the quiescent current of the comparator when enabled, excluding the disabled bias current of the fast start-up current mirror.

### 4.2.4 Simulation Results

The proposed wireless power receiver circuit was designed for Texas Instruments’ 180-nm CMOS process and simulated using the TIspongeD simulator. The breakdown voltage for the process is 1.8 V and the circuit was designed for a \( V_{RECT} \) voltage of 0.9 V to 1.5 V, so that a Nickel-cadmium (NiCd) battery, Nickel-metal hydride (NiMH) battery, or a supercapacitor (also known as electric double-layer capacitor) are all viable energy storage elements. Additionally, a 400-\( \mu \)H Coilcraft 4513TC receiver coil was chosen as the receiver pickup coil and was modeled using lumped elements. The lumped winding resistance of the coil considered skin effects (i.e., high frequency current distributing to the surface of a conductor) by introducing a frequency-dependent resistor in series with the coil’s DC resistance of 9.66 \( \Omega \). Furthermore, the pickup coil’s parasitic winding capacitance was modeled with a 1.83 pF capacitor. A floating voltage source emulated the induced coil voltage, allowing \( |V_{emf,r}| \) to range from 25 mV to 350 mV with an operational frequency of 125 kHz. Finally, the \( S_{EMF,R} \) signal necessary to synchronize the power receiver to the \( v_{EMF,R} \) voltage originated from an idealized \( v_{EMF,R} \) polarity detector,
where its power consumption was not considered part of the system’s power budget. As such, only the power losses associated with conduction, switching, and quiescent losses from the previous power loss analysis are considered.

Figure 4.10 displays system level functionality for the proposed inductive rectifier. A \(|V_{emf}|\) voltage of 350 mV driven at 125 kHz produces the 4.10 mA peak-to-peak inductor current waveform, with the inductive rectifier sending packets of positive current (i.e., \(i_{RECT}\)) to \(V_{RECT}\) (1.2 V). From simulations, the inductive rectifier extracts 223.6 µW of power from the induced voltage source and transfers 179.7 µW of that power to \(V_{RECT}\) for a receiver efficiency of 80.4 %.

![Image of waveform](image-url)

**Figure 4.10.** Time-domain simulation depicting inductor and rectified current for a \(|V_{emf}|\) of 350 mV at 125kHz and a \(V_{RECT}\) of 1.2 V.

Figure 4.11a-b shows a \(\tau_{EN}^+\) to \(\tau_{DE}^+\) commutation event. Prior to the event, \(M_N^+\) carries all of \(i_L\), but once \(M_N^+\) disengages the current flows into the parasitic capacitance, which is why \(v_{SW}^+\) rises and continues to do so until the soft-synchronizing switch engages and \(M_P^+\) begins carrying the inductor current. It is interesting to note that the currents flowing into the drains of \(M_N^+\) and \(M_P^+\) during the soft-switching event are slightly greater than zero, shown in Figure 4.11a. However, that energy is not dissipated and is instead stored onto the parasitic capacitances of the MOS switches as a fractional component of the lumped \(C_{PAR}\). Figure 4.11c-d displays a full de-energizing event, where the voltage drop across the self-synchronizing switch is on the order of millivolts.
Figure 4.11. Simulated time-domain waveforms for the (a-b) \( \tau_{EN}^+ \) to \( \tau_{DE}^+ \) commutation event and (c-d) de-energizing event.

4.2.5 Discussion

For low \(|V_{emf,r}|\), gate driving losses of the switches and quiescent power losses for control govern \( P_{LOSS} \), as shown in Figure 4.12a, so that the effective threshold, from Equation (4.6), reduces to

\[
V_{TR} = \pi \sqrt{P_{LOSS(MN)} f_o L_R} \approx \pi \sqrt{E_{SW} f_o + P_Q} f_o L_R .
\]

Here, \( E_{SWfO} \) is \( P_{SW} \) and the separation highlights that the switching losses are proportional to \( f_o \). As \( V_{TR} \) is only weakly affected by the conduction losses, a larger \( R_R \) (\( P_{C.R} \)), and therefore a smaller \( Q_R \), only minimally affects \( V_{TR} \), such that a lower quality pickup coil may be used to produce a similar \( V_{TR} \). This is a major difference from the prior art resonant receivers that rely on higher quality factors to reduce \( V_{TR} \).

For higher \(|V_{emf,r}|\) values, conduction losses tend to dominate. More specifically, as conduction losses of \( M_N^+ \) and \( M_N^- \) (\( P_{C.N} \)) and \( R_R \) (\( P_{C.R} \)) scale with \(|V_{emf,r}|^2\), while conduction losses of \( M_P^+ \) and \( M_P^- \) (\( P_{C.P} \)) scale with \(|V_{emf,r}|^3\), the total power losses

\[
\text{Total Power Losses} = P_{LOSS} = P_{SW} + P_{C.N} + P_{C.R} + P_{C.P} + P_{QUIESCENT}.
\]
increase with larger $|V_{\text{emf},r}|$, as shown in Figure 4.12a. However, as conduction losses scale with $P_{\text{EMF},R}$, and to some extent $P_{\text{EMF},R}^{1.5}$, the prototype’s efficiency, $\eta_R$ (defined as $P_{\text{RECT}}/P_{\text{EMF},R}$), remains fairly constant in the large $|V_{\text{emf},r}|$ region, as shown in Figure 4.12b, with a peak efficiency of 80.4%. The simulations show the proposed receiver successfully transferred its maximum power to $C_{\text{RECT}}$ ($P_{\text{RECT}}$) of 179.7 $\mu$W for a $|V_{\text{emf},r}|$ of 350 mV.

![Simulated power losses and receiver efficiency](image)

Figure 4.12. Simulated power losses of bias power $P_{Q,BI}$, gate-driving losses $P_{SW,GD}$, comparator losses $P_{Q,CP}$, PMOS conduction losses $P_{CP}$, NMOS conduction losses $P_{CN}$, and ESR conduction losses $P_{CR}$ across induced receiver voltage $|V_{\text{emf},r}|$ at 125 kHz for a $V_{\text{RECT}}$ of 1.2 V. (b) Simulated receiver efficiency $\eta_R$ and net rectified power $P_{\text{RECT}}$ across peak induced receiver voltage $|V_{\text{emf},r}|$ at 125 kHz and $V_{\text{RECT}}$ of 1.2 V.

4.3 Wireless Power Receiver Prototype

Simulation results showed that the proposed inductive rectifying scheme can draw power from a $|V_{\text{emf},r}|$ voltage of less than 50 mV and successfully transfer (i.e., with positive net power) it to a battery. Still, a prototype for the wireless power receiver is necessary to validate circuit functionality and quantify operational limits. Yet, to test the prototype, an external time-varying magnetic field and a $v_{\text{EMF},R}$ polarity detector need to be realized. To that end, a wireless power transmitter circuit that emanates an external magnetic field and a $v_{\text{EMF},R}$ polarity detector are also designed and implemented. Finally, the prototype of the
wireless power receiver–battery charger system is designed, built, and experimentally tested and evaluated.

### 4.3.1 IC Prototype Wireless Power Receiver System

Figure 4.13a shows the prototype wireless power receiver–battery charger system fabricated with Texas Instruments’ 180-nm CMOS process technology. The 700 x 700 μm² silicon die, shown in Figure 4.13b, includes energizing NMOS switches $M_N^+$, $M_N^-$, de-energizing PMOS switches $M_P^+$, $M_P^-$, self-synchronizing comparators, $C_{PD^+}$, $C_{PD^-}$, control logic, and a bias generator. The full system also includes off-chip components, namely, the receiver coil $L_R$, the rectifier capacitor $C_{RECT}$, and for testing flexibility, both the bias resistor $R_{BIAS}$ and the $v_{EMF,R}$ polarity detector. Additionally, the IC incorporates test-only circuits such as pin-out digital buffers, over-ride MUXs to directly control switches, and extra test-mode logic.

![Figure 4.13](image)

Figure 4.13. (a) Prototype wireless power receiver–battery charger system with the corresponding (b) IC die (transistors dimensions are in μm).

Figure 4.14 shows the testing setup for the wireless power receiver, with a wireless power transmitter generating the time-varying magnetic field and a $v_{EMF,R}$ polarity detector synchronizing the power receiver to the magnetic field. The wireless power transmitter generates the external time-varying magnetic field, which penetrates
the pickup coil’s area and induces the $v_{EMF,R}$ coil voltage. When an AC current flows through the transmitter coil, it generates an external magnetic field. To produce that AC current, a sinusoidal voltage source, $v_T$, drives the transmitter coil along with a series resonant capacitor, $C_T$. The resonant capacitor’s impedance is chosen to cancel the impedance of $L_T$ at the operating frequency, so that a large transmitter coil current and a corresponding large external magnetic field are generated. The receiver’s induced voltage written in terms of the mutual inductance, $M_C$, between the coils is

$$v_{EMF,R} = M_C \frac{di_T}{dt} = k_C \sqrt{L_T L_R} \frac{di_T}{dt},$$

(4.17)

where $k_C$ is the coupling factor.

![Wireless Power Transmitter and Receiver Circuit](image)

**Figure 4.14.** A wireless power transmitter and $v_{EMF,R}$ polarity detector are used as part of the test setup (transistors dimensions are in μm).

The $v_{EMF,R}$ polarity detector, shown in Figure 4.14, creates the $S_{EMF,R}$ signal, which synchronizes energizing and de-energizing events with $v_{EMF,R}$. The polarity information is encoded into $S_{EMF,R}$ with a digital HIGH corresponding to a positive $v_{EMF,R}$ and a digital LOW corresponding to a negative $v_{EMF,R}$. The generator recognizes polarity by noting that $v_{EMF,R}$ is proportional to $di_T/dt$, so that comparing $i_T$ with its delayed version extracts $i_T$’s slope and therefore $v_{EMF,R}$’s polarity. For testing purposes, the $v_{EMF,R}$ polarity detector is external from the wireless power receiver circuit.
The test printed circuit board (PCB), displayed in Figure 4.15a, includes the 28-pin thin shrink small-outline package (TSSOP) prototype IC along with receiver coil $L_R$, rectifier capacitor $C_{RECT}$, bias resistor $R_{BIAS}$, and for testing and measurement purposes: current sensing resistors with their accompanied instrumentation amplifiers and voltage buffers to monitor high impedance switching nodes. A 1.2 V power supply emulated the micro-scale battery for all the experimental tests, except for charging performance, where an isolated $C_{RECT}$ emulated the micro-scale battery. The 400-μH Coilcraft 4513TC receiver coil used introduced an ESR of 9.66 Ω with a quality factor of 29 for the operational frequency of 125 kHz. The power transmitter, as shown in Figure 4.15b, consists of a 14.8-mH Coilcraft ZXC transmitter coil with an ESR of 160 Ω, primary resonant capacitor $C_T$, $v_{EMF,R}$ polarity detector, and external connectors that lead to the $v_T$ source (i.e., power amplifier). To vary $k_C$, the instrumentation stand facilitated 50 mm travel range using a 443-4 Newport linear stage with a 1 μm sensitive SM-50 Newport vernier micrometer.

![Image](image_url)

Figure 4.15. (a) The test printed circuit board (PCB) and (b) test instrumentation stand.
4.3.2 Experimental Results

Time-domain Waveforms: The power transmitter in the test setup is placed at a separation distance between the coils that induces the 125 kHz 330 mV induced coil voltage, seen in Figure 4.16a. Additionally, Figure 4.16b shows the corresponding pickup coil’s current of 4 mA peak to peak throughout a full-cycle of the inductively rectifying scheme. Moreover, Figure 4.16c-e displays the positive de-energizing event waveforms, with rectified current flowing into the $V_{RECT}$ supply, proving the functionality of the inductive rectifying prototype.

Figure 4.16. Experimental time-domain waveforms of the (a) induced receiver coil voltage $v_{EMF,R}$ and (b) receiver coil current $i_L$. Experimental positive de-energizing waveforms of the (c) rectified output current $i_{RECT}$, (d) positive switching node $v_{SW}^+$, and (e) receiver coil current $i_L$ (a–b refers to a different $|V_{emf}|$ then c–e).

The experimental time-domain waveforms are in agreement with simulations, with the exception that the soft-switching times, $\tau_{SS}^+$ and $\tau_{SS}^-$, are slightly longer. The reason for the discrepancy arises from additional PCB capacitance on switching nodes.
\(|v_{SW}^+\) and \(|v_{SW}^-\)| of roughly 1.5 pF that increases the value of \(C_{PAR}\), from which amended simulations showed similar soft-switching times. Here, it is noted, that while the rest of Figure 4.16 was a direct experimental measurement (i.e., using voltage/current probe), \(v_{EMF,R}\) cannot be measured directly as the voltage is internal to the coil and is instead calculated from Equation (4.17); however, the transmitter coil’s current as is required in Equation (4.17), was measured experimentally.

**Charging Performance:** To test the charging performance, a 100-nF SMD ceramic capacitor \(C_{RECT}\) was placed at the \(V_{RECT}\) node of the prototype receiver and pre-charged to 1.2 V (using a diode and a supply). Then, the prototype receiver was enabled to successfully charge \(C_{RECT}\), as shown in Figure 4.17a, for the following \(|V_{emf,r}|\) values: 30.2, 127, 261, and 368 mV. The packets of energy sent every half-cycle (4 μs) gave \(v_{RECT}\) a staircase appearance with the small periodic energy packets resembling that of a pulse charging (trickle charging) profile \([126, 127]\). As expected, larger \(|V_{emf,r}|\) values resulted in a steeper staircase, as \(P_{EMF,R}\) increases with \(|V_{emf,r}|^2\); additionally, as the energy within a packet is larger, the steps sizes also increased with \(|V_{emf,r}|\). Conversely, for lower \(|V_{emf,r}|\) values, not only did \(P_{EMF,R}\) decrease, but power losses became significant until an effective threshold \(V_{TR}\) of 30.2 mV resulted in no power delivery to \(C_{RECT}\).

\[
C_{RECT} = 100 \text{ nF} \\
|V| = 1 \text{ V} \\
|V_{emf}| = V_{TR}
\]

**Figure 4.17.** (a) Experimental time-domain charging profiles for a 100-nF SMD ceramic capacitor at 125 kHz. (b) Experimental frequency response for the effective threshold voltage of the prototyped receiver overlaid with the theoretical effective threshold voltage of resonant receivers with \(Q_R\) of 29 and 100 for a \(V_{RECT}\) of 1.2 V.
**Threshold Frequency Sensitivity:** Testing the frequency sensitivity of the effective threshold amounted to varying the transmitting frequency over 100 – 150 kHz while separating the coils by a distance corresponding to $|V_{emf,r}|$ equal to $V_{TR}$. The results show that the effective threshold voltage, as depicted in Figure 4.17b, varies by only 13.59 mV over a frequency range of 50 kHz. To compare, the theoretical $V_{TR}$ values for the equivalent resonant receiver ($Q_R = 29$) and a receiver with a $Q_R$ of 100 are overlaid onto Figure 4.17b. At the natural frequency ($f_O = 125$ kHz) both resonant receivers have a similar $V_{TR}$ to that of the proposed receiver, but as the deviation from the natural frequency increases so does $V_{TR}$. Additionally, after only a $\pm 1.36\%$ deviation from $\omega_R$ the $V_{TR}$ of the prototype is less than that of even the resonant receiver of $Q_R = 100$. What is more, for larger deviations from $\omega_R$, the $V_{TR}$ of both resonant receivers converge, mitigating the benefits added for higher quality factors, while $V_{TR}$ for of the prototype remains fairly constant and drastically lower than that of the resonant receivers.

**Receiver Power Efficiency:** The prototype’s power loses $P_{LOSS}$, power efficiency $\eta_R$, and rectified power $P_{RECT}$ were all recorded over a $|V_{emf,r}|$ range of 39.5 – 386 mV at a transmitted frequency of 125 kHz, as shown in Figure 4.18. The prototype receiver successfully transferred its maximum net power to $C_{RECT}$ ($P_{RECT}$) of 223.8 $\mu$W for a $|V_{emf,r}|$ of 386 mV, which also corresponded to the prototype’s peak $\eta_R$ of 81.2%. Furthermore, the power efficiency and rectified power match well with simulation, see Figure 4.18b, so that similar conclusions to those obtained in the simulation discussion are drawn. However, as shown in Figure 4.18a, the quiescent power loss of the comparators, $P_{CP}$, is larger than that simulated; this is especially true at lower values of $|V_{emf,r}|$. Again, the reason for the discrepancy arises from the additional PCB capacitance on switching nodes ($v_{SW}^+$ and $v_{SW}^-$), which increased the durations of the soft-switching commutations. This increase in soft-switching time elongates the duration for which the comparators are enabled and drawing quiescent current, so that more quiescent power than that simulated was dissipated.
4.3.3 Discussion

The experiments successfully confirmed that the proposed wireless power receiver and battery charger system implementing the inductive rectifying system is capable of delivering power from low EMF coil voltages to much higher battery voltages. There are a few important advantages worth mentioning about the proposed solution as compared with the most readily found solution, that is, the resonant receiver. First, the presented prototype reduced the effective threshold to 30.2 mV, a 27.1% reduction versus that of an equivalent resonate receiver ($Q_R = 29$). This fundamentally results from shifting the limiting factor of $V_{TR}$ from the $Q_R$ of the pickup coil (resonant receiver) to the power losses of the system, $P_{LOSS(MIN)}$ (proposed receiver). Second, the threshold of the prototype exhibited minimal sensitivity to frequency as compared to that of the resonate receiver and fundamentally results from avoiding the use of a high-$Q$ filter. Third, the presented prototype does not require an off-chip resonant capacitor, aiding in the aim of integration. Lastly, the prototype charged $V_{RECT}$ with small periodic energy packets resembling that of a trickle charging profile found in many battery chargers [126, 127]. This last point is critical for battery charging applications, as the majority of the wireless
power receivers rectify to an intermediate capacitor followed by an additional power conditioning block that finally transfers the power to the battery [128]. This additional power conditioning decreases the receiver power efficiency while increasing the cost, size, and complexity of the wireless power receiver [128].

The proposed inductive rectifying scheme implemented by the prototype, draws more power from the $v_{EMF,R}$ source voltage (i.e., $P_{EMF,R}$) than prior art inductive rectifiers. However, a comparison of power extraction capabilities of the proposed inductive rectifier scheme versus that of the resonant receiver, using Equation (3.3) and Equation (4.3), finds that $P_{EMF,R}$ is greater for the resonant receiver case when

$$\left| V_{emf,r} \right| < \frac{\pi}{4} V_{RECT} \left\rvert_{2\pi f_o = \omega_R} \right..$$

(4.18)

While Equation (4.18) is only valid for the small bandwidth about the resonant frequency, the result suggests that more power can be extracted from the $v_{EMF,R}$ source. The means by which to extract more power from the low $v_{EMF,R}$ voltage source using inductive rectifying is the subject of the following chapter.
CHAPTER 5
INCREASING RECEIVED POWER USING ENERGY-INVESTMENT TECHNIQUES

The proposed inductive rectifying prototype of Chapter 4 reduced the input-referred threshold of inductive rectifiers to unprecedented levels, but was found to have lower power extracting capabilities than that of the resonant receiver. As such, the means by which to extract more power from the low $v_{EMF,R}$ voltage source using inductive rectifying is the subject of this chapter. The resulting fundamental requirements for power extraction motivate the construction of the newly proposed energy-investment power receiver, which uses energy investments from the battery as a means of conditioning the pickup coil to draw more power. Furthermore, the newly proposed energy-investment power receiver has the capacity to extract more power than even that of the resonant receiver.

5.1 Input Power Conditioning

Determining the fundamental requirements of power transfer from transmitter to receiver will ultimately motivate the means by which to increase that received power. With that goal in mind, Figure 5.1a displays the general wireless power receiver architecture. Transmitted power manifests itself on the receiver end from the induced coil voltage $v_{EMF,R}$, which is single-toned and equal to

$$v_{EMF,R} = V_{EMF,R} \cos(\omega t + \theta), \quad (5.1)$$

where $V_{EMF,R}$ and $\theta$ are its amplitude and phase angle, respectively.
Figure 5.1. (a) general wireless power receiver architecture and (b) its equivalent representation as a Fourier series of its coil current components.

Power drawn from the coil voltage is done so via the inductor current $i_L$. All power receivers effectively manipulate $i_L$ such that they draw power from the coil voltage. As such, identifying the requirements for power extraction amounts to identifying which components of $i_L$ are essential. For simplicity, the inductor current is assumed periodic with $v_{EMF,R}$, however, in general $i_L$ need not be periodic to draw similar conclusions (see Appendix A). Given periodicity, $i_L$ can be decomposed into its corresponding Fourier series,

$$i_L = I_{L(\text{DC})} + \sum_{n=1}^{\infty} I_{L(n)} \cos(n\omega_0 t + \phi_n),$$

(5.2)

where $I_{L(\text{DC})}$ is the average inductor current and where $I_{L(n)}$ and $\phi_n$ are the amplitude and phase angle of the $n\omega_0$ frequency component of $i_L$, as is shown in Figure 5.1b. The average power drawn from $v_{EMF,R}$ over an entire operational period is then
\[ P_{EMF,R} = \frac{1}{T_O} \int_{-T_O/2}^{T_O/2} v_{EMF,R} i_L dt , \]  

where the relation between angular frequency \( \omega_O \) and operational period \( T_O \) is simply \( \omega_O T_O = 2\pi \). Then, inserting the expressions from \( i_L \) and \( v_{EMF,R} \) into the equation for \( P_{EMF,R} \) yields

\[ P_{EMF,R} = \frac{1}{T_O} \int_{-T_O/2}^{T_O/2} V_{EMF,R} \cos(\omega_O t + \theta) \left[ I_{L,DC} + \sum_{n=1}^{\infty} I_{L(n)} \cos(n \omega_O t + \phi_n) \right] dt . \]  

This expression greatly simplifies after recognizing that all harmonic contributions from \( i_L \) are orthogonal to the fundamental tone of the coil voltage, meaning that the harmonics of \( i_L \) draw no average power from \( v_{EMF,R} \) [129]. This orthogonality is equivalently stated as

\[ \int_{-T_O/2}^{T_O/2} \cos(\omega_O t + \theta) \cos(n \omega_O t + \phi_n) dt = 0, \quad n \neq 1 . \]  

So that after employing the orthogonality of different frequency components, the average power expression simplifies to

\[ P_{EMF,R} = \frac{1}{T_O} \int_{-T_O/2}^{T_O/2} V_{EMF,R} \cos(\omega_O t + \theta) I_{L(1)} \cos(\omega_O t + \phi_1) dt , \]  

which is to say that the only component of \( i_L \) that draws any net power from the source is the fundamental component. To highlight this, an example case of the power drawn from the second and third harmonics of \( i_L \) are shown in Figure 5.2. The waveforms show that while the instantaneous power drawn is non-zero, its average over the operational period is zero.
When considering power drawn due to the fundamental component of \( i_L \) (i.e., Equation (5.6)), it is instructive to reconstruct the fundamental component of \( i_L \) into an equivalent sum of two components that are in-phase and 90° out-of-phase with \( v_{\text{EMF,R}} \), as geometrically shown in Figure 5.3a and explicitly written as

\[
I_{L(1)} \cos(\omega t + \phi) = I_{L(\text{IN})} \cos(\omega t + \theta) + I_{L(\text{OUT})} \sin(\omega t + \theta).
\]  

(5.7)

Where the in-phase amplitude, \( I_{L(\text{IN})} \), equals

\[
I_{L(\text{IN})} = I_{L(1)} \cos(\theta - \phi),
\]

(5.8)

and where the 90° out-of-phase amplitude, \( I_{L(\text{OUT})} \), equals

\[
I_{L(\text{OUT})} = I_{L(1)} \sin(\theta - \phi).
\]

(5.9)
Then inserting the newly constructed fundamental component into Equation (5.6) yields

$$P_{EMF,R} = \frac{1}{T_o} \int_{-T_o/2}^{T_o/2} V_{EMF,R} \cos(\omega_o t + \theta) \left[ I_{L(IN)} \cos(\omega_o t + \theta) + I_{L(OUT)} \sin(\omega_o t + \theta) \right] dt.$$  \hfill (5.10)

This expression can be simplified by once again making use of orthogonality. In this case it is the out-of-phase component that draws no average power from the coil voltage:

$$\frac{1}{T_o} \int_{-T_o/2}^{T_o/2} V_{EMF,R} \cos(\omega_o t + \theta) I_{L(OUT)} \sin(\omega_o t + \theta) dt = 0.$$  \hfill (5.11)

So that the only component of \(i_L\) that can draw any average power is the fundamental component that is in-phase with the \(v_{EMF,R}\) voltage source. As such, the average power reduces to

$$P_{EMF,R} = \frac{1}{T_o} \int_{-T_o/2}^{T_o/2} V_{EMF,R} \cos(\omega_o t + \theta) I_{L(IN)} \cos(\omega_o t + \theta) dt \quad \frac{V_{EMF,R} I_{L(IN)}}{2} = \frac{V_{EMF,R} I_{L(1)}}{2} \cos(\theta - \phi_1)$$  \hfill (5.12)

Notice that the relationship between the \(I_{L(IN)}\) and \(I_{L(1)}\) is a multiplicative factor of \(\cos(\theta - \phi_1)\), which is commonly referred to as the power factor [129]. This factor represents the projection of the fundamental component onto the in-phase component. The power factor is maximized and equal to one when there is no phase difference between the fundamental component of \(i_L\) and the coil voltage. When the fundamental component is 90º out of phase, the power factor is zero, which is to say that 90º out of...
phase signals are orthogonal. The example shown in Figure 5.4 illustrates that the power drawn by $i_{L(1)}$ is exactly the same as the power drawn by its in-phase component (i.e., $i_{L(IN)}$) and that its out-of-phase component draws no average power.

![Graphs showing (a) the fundamental component of $i_L$, (b) the in-phase component of $i_{L(1)}$, and (c) the out-of-phase component of $i_{L(1)}$.](image)

**Figure 5.4** Power drawn from $v_{EMF,R}$ with (a) the fundamental component of $i_L$, (b) the in-phase component of $i_{L(1)}$, and (c) the out-of-phase component of $i_{L(1)}$.

### 5.1.1 Available Power

Until now, the discussion has focused on the requirements for power extraction from the induced coil voltage $v_{EMF,R}$, which requires the coil current $i_L$ to have a fundamental component that is in-phase with $v_{EMF,R}$. However, not all of the power extracted from $v_{EMF,R}$ (i.e., $P_{EMF,R}$) may transfer to the power converter. In particular, the pickup coil’s ESR will dissipate some of the power from $P_{EMF,R}$ so that the received power is
\[ P_{\text{REC}} = P_{\text{EMF, R}} - P_{\text{C.R}}, \] (5.13)

where the power dissipated by the coil’s ESR is expressed as

\[ P_{\text{C.R}} = R_R^2 I_{L(RMS)}^2 = R_R \frac{1}{T_o} \int_{-T_o/2}^{T_o/2} t_i^2 dt. \] (5.14)

To further examine this power loss, \( i_L \) can be expanded as a Fourier series

\[ P_{\text{C.R}} = R_R \frac{1}{T_o} \int_{-T_o/2}^{T_o/2} \left[ I_{L,\text{(DC)}} + \sum_{n=1}^{\infty} I_{L(n)} \cos(n \omega_o t + \phi_n) \right]^2 dt, \] (5.15)

which simplifies when using frequency orthogonality to null out all cross terms and produce the following expression

\[ P_{\text{C.R}} = R_R \left[ I_{L,\text{(DC)}}^2 + \sum_{n=1}^{\infty} \left( \frac{I_{L(n)}}{\sqrt{2}} \right)^2 \right]. \] (5.16)

Equation 5.16 shows that the power consumed by \( R_R \) is a function of all the frequency components of \( i_L \). This is not the case, however, for \( P_{\text{EMF, R}} \), which only depends on the fundamental component of \( i_L \). As such, inserting Equation 5.16 and 5.12 into 5.13 to yield

\[ P_{\text{REC}} = \frac{V_{\text{EMF, R}} I_{L(1)} \cos(\theta - \phi_1)}{2} - R_R \left[ I_{L,\text{(DC)}}^2 + \sum_{n=1}^{\infty} \left( \frac{I_{L(n)}}{\sqrt{2}} \right)^2 \right], \] (5.17)

highlights that the harmonic and dc components of \( i_L \) reduce the received power, such that maximizing received power requires all dc and harmonic components of \( i_L \) to be zero. Taking that step of setting \( I_{L,\text{(DC)}} \) and \( I_{L(n)} \) to 0, for \( n > 1 \), reduces \( P_{\text{REC}} \) to

\[ P_{\text{REC}} = \frac{V_{\text{EMF, R}} I_{L(1)} \cos(\theta - \phi_1)}{2} - R_R \left( \frac{I_{L(1)}}{\sqrt{2}} \right)^2, \] (5.18)

which when rewritten as its in and out of phase components yields

\[ P_{\text{REC}} = \frac{V_{\text{EMF, R}} I_{L(1)}}{2} - \frac{R_R}{2} \left[ I_{L(\text{IN})}^2 + I_{L(\text{OUT})}^2 \right]. \] (5.19)
Once again the dissipative power $P_{C,R}$ depends on a component, in this case $I_{L(OUT)}$, that does not contribute to $P_{EMF,R}$, which result in a reduction of $P_{REC}$. Therefore, maximizing $P_{REC}$ requires $I_{L(OUT)}$ to be zero, such that $i_L$ and its in-phase fundamental component are equal (i.e., $i_L = i_{L(IN)}$). Then setting $i_L$ equal to $i_{L(IN)}$, yields a received power of

$$P_{REC} = \frac{V_{EMF,R}^2}{2} I_{L(IN)} - \frac{R_R}{2} I_{L(IN)}^2, \quad (5.20)$$

Finally, all that remains is to determine the amplitude of the in-phase component that maximizes $P_{REC}$, which is achieved by setting

$$\frac{\partial P_{REC}}{\partial I_{L(IN)}} = 0. \quad (5.21)$$

The left-hand side of Equation (5.21) equals

$$\frac{\partial P_{REC}}{\partial I_{L(IN)}} = \frac{V_{EMF,R}}{2} + \frac{I_{L(IN)}}{2} \frac{\partial V_{EMF,R}}{\partial I_{L(IN)}} - R_R I_{L(IN)}, \quad (5.22)$$

where the $\partial V_{EMF,R}/\partial I_{L(IN)}$ term accounts for how $V_{EMF,R}$ decreases with increased $I_{L(IN)}$, which originates from loading the wireless transmitter. This term can be interpreted as a small-signal resistance that models the loading and is defined as

$$r_{eq,r} \equiv - \frac{\partial V_{EMF,R}}{\partial I_{L(IN)}}, \quad (5.23)$$

where the negative sign is introduced to keep $r_{eq,r}$ positive, because $V_{EMF,R}$ decreases with additional loading. Then using the newly defined $r_{eq,r}$ to solve Equation (5.21) yields

$$I_{L(IN)} \bigg|_{\frac{\partial P_{REC}}{\partial I_{L(IN)}} = 0} = \frac{V_{EMF,R}}{2R_R + r_{eq,r}} \quad (5.24)$$

and

$$P_{AVA} = P_{REC} \bigg|_{\frac{\partial P_{REC}}{\partial I_{L(IN)}} = 0} = \frac{V_{EMF,R}^2}{8R_R} \left[ \frac{1 + r_{eq,r}^2 R_R}{(1 + 0.5 r_{eq,r}^2 R_R^2)^2} \right]. \quad (5.25)$$
where $P_{AVA}$ is commonly referred to as the available power and equals the maximum achievable received power. $P_{AVA}$ is used as a comparative benchmark, because it determines how effective power is received for any receiver topology. Finally, for the case that the loading can be considered negligible (i.e., $r_{eq,r} \ll R_R$), Equation (5.25) reduces to the more conventional formulation of the available power, namely,

$$P_{AVA} \bigg|_{r_{eq,r} \ll R_R} = \frac{V_{EMF,R}^2}{8R_R}. \quad (5.26)$$

### 5.2 Role of Energy-investment

The previous section of this chapter proved what the coil current (i.e., $i_L$) requirements are for achieving maximum received power, which is more often referred to as the available power of the $v_{EMF,R}$ source. Still, the requirements from the converter’s perspective have yet to be addressed. Specifically, the following analysis will show that the converter needs to condition the coil current by driving the coil with a voltage that lags behind the induced coil voltage. Moreover, the converter must not only receive power, but must at times source it in the form of energy-investments.

To begin with, consider the general wireless power receiver architecture shown in Figure 5.5. For simplicity, the induced coil voltage is assumed to have no phase shift (i.e., $\theta$ in Equation (5.1) is set to zero). Furthermore, and as was previously derived in Equation (5.24), the coil current must be a sinusoidal signal with the same phase and frequency as $v_{EMF,R}$ in order extract all of the available power. In other words, the optimum coil current $i_{L(OPT)}$ is simply a multiplicative factor of $v_{EMF,R}$, which equals

$$i_{L(OPT)} = \frac{v_{EMF,R}}{2R_R + r_{eq,r}} = \frac{V_{EMF,R}}{2R_R + r_{eq,r}} \cos(\omega f t). \quad (5.27)$$
Then, given the requirement of $i_L(OPT)$, the required converter voltage $v_{CONV(OPT)}$ can be deduced using KVL to yield

$$v_{CONV(OPT)} = v_{EMF,R} - R_R i_L(OPT) - L_R \frac{di_L(OPT)}{dt}. \quad (5.28)$$

Then, inserting Equation (5.27) into (5.28) gives

$$v_{CONV(OPT)} = V_{EMF,R} \cos(\omega_o t) - R_R \frac{V_{EMF,R}}{2R_R + r_{eq,r}} \cos(\omega_o t) + L_R \omega_o \frac{V_{EMF,R}}{2R_R + r_{eq,r}} \sin(\omega_o t), \quad (5.29)$$

which with some algebraic manipulation reduces to

$$v_{CONV(OPT)} = \frac{V_{EMF,R}}{2} \left[ \cos(\omega_o t) + \frac{Q_R}{1 + r_{eq,r}/R_R} \sin(\omega_o t) \right], \quad (5.30)$$

where $Q_R$ is the pickup coil’s quality factor and equals $Q_R = \omega_o L_R/R_R$. Notice that $v_{CONV}$ is not entirely in-phase with $v_{EMF,R}$ and instead has an out-of-phase component, which arises from the $\sin(\omega_o t)$ term. In other words, one requirement for the converter voltage to shape $i_L$ into $i_L(OPT)$, is that $v_{CONV}$ lags behind $v_{EMF,R}$. This lag varies between $0^\circ$ and $90^\circ$ and equals

$$\arg\{v_{CONV(OPT)}\} = -\tan^{-1} \left( \frac{Q_R}{1 + r_{eq,r}/R_R} \right). \quad (5.31)$$

This lagging suggests that the impedance looking into the converter is capacitive, which is in agreement with the impedance matching condition. Moreover, it is reassuring to
point out that the input impedance of the power converter in Figure 5.5 must be the complex conjugate match of the pickup coil’s impedance (i.e., impedance matching condition) for the maximum available power condition.

As of yet, there has been no discussion on the role of energy-investment, but as will be shown in the upcoming analysis, the power converter must allow for bidirectional power flow to achieve maximum power transfer. To proceed, consider the instantaneous power flowing into the power converter under the available power conditions

\[
P_{\text{AVA}} = P_{\text{CONV(OPT)}} = v_{\text{CONV(OPT)}}i_{L(OPT)}
\]

where \(P_{\text{AVA}}\) corresponds to the available power found in Equation (5.25). Then, rewriting \(p_{\text{CONV(OPT)}}\) in terms of double-angle trigonometric identities simplifies \(p_{\text{CONV(OPT)}}\) to

\[
p_{\text{CONV(OPT)}} = P_{\text{AVA}} \left[ 1 + \cos(2\omega_o t) + \frac{Q_R}{1 + r_{eq,r}/R_R} \sin(2\omega_o t) \right].
\]

First, notice that the time average of \(p_{\text{CONV(OPT)}}\) equals \(P_{\text{AVA}}\), which means that the converter does indeed receive the available power. Second, the instantaneous converter power oscillates about this average power and at times will be negative:

\[
\min\{p_{\text{CONV(OPT)}}\} = P_{\text{AVA}} \left[ 1 - \sqrt{1 + \left( \frac{Q_R}{1 + r_{eq,r}/R_R} \right)^2} \right] < 0.
\]

Having a negative \(p_{\text{CONV(OPT)}}\) corresponds to the converter temporarily sourcing power into the pickup coil. Its significance is that the power converter must allow for the bidirectional flow of energy to achieve maximal power transfer. Intuitively, this results because \(L_R\) has magnetic energy equal to \(\frac{1}{2}L_Ri_L^2\), so that as \(i_L\) varies across the cycle, energy must be sourced into or drawn from \(L_R\) whenever \(i_L^2\) increases or decreases, respectfully. Moreover, to generate larger peak-to-peak values of \(i_L\) (as is required to
increase $P_{EMF,R}$) more energy needs to be sourced into $L_R$ during its peaks and troughs. However, as $i_{L(OPT)}$ is periodic, there will be no net change in $i_L$ after a full cycle, which is to say that the energy temporarily sourced into $L_R$ will ultimately be returned after a complete cycle. Temporarily sourcing energy into the pickup coil can be considered an investment, because at a later time the energy is returned along with an otherwise unattainable energy profit.

### 5.3 Previous Inductive Rectifying Scheme Reexamined

To give context, the proposed receiver of Chapter 4 only absorbed packets of energy, but never sourced energy. This implies that the receiver suboptimally extracted power from the pickup coil. Therefore, to gain further insight into the ideas of energy investment, that same proposed receiver will be reexamined under the new light of in-phase components and energy investment. Those teachings reveal how to draw more power from the pickup coil.

![Diagram](image)

**Figure 5.6.** (a) Receiver circuit and (b) steady-state waveforms of the previous inductive rectifying scheme from Chapter 4.

Figure 5.6 displays the inductive rectifying scheme of Chapter 4. As previously described, the active diodes $S_D^+$ and $S_D^-$ only allow positive current to flow into $V_{RECT}$ as the $i_{RECT}$ waveform shows. This means that the converter only receives power but never sources it, which from the previous analysis suggests that the receiver operates in a suboptimal fashion. To gain insight on how power is drawn from the $v_{EMF,R}$ source, the
current flowing through the coil, i.e., \( i_L \), can be decomposed into its in-phase and out-of-phase components, as is shown in Figure 5.7. The out-of-phase component draws no power from the coil and can be disregarded for the power extraction analysis. The remainder of \( i_L \), which are the in-phase harmonic components of \( i_L \) or \( i_L(TRAP) \) in Figure 5.7, has a shape that is similar to a square wave, but has slanted rising/falling edges that make it trapezoidal. Furthermore, the fundamental component of this trapezoidal waveform can be pulled out as \( i_L(IN) \) in Figure 5.7. \( i_L(IN) \) is the only component that draws any net power from \( v_{EMF,R} \) and its amplitude should be made as large as conduction losses and loading effects allow.

![Diagram of current decomposition](image)

**Figure 5.7.** De-composition of previous inductive rectifying scheme’s coil current \((i_L)\) into its in-phase \((i_L(IN))\) and out-of-phase \((i_L(OUT))\) components.

From a visual or geometric perspective, a larger peak-to-peak valued \( i_L(TRAP) \) contains a larger component of \( i_L(IN) \) (as will be verified in the upcoming section). This
means that increasing $i_{L(TRAP)}$’s peak-to-peak value of $\Delta i_L$ increases the only power extracting component, namely, $i_{L(IN)}$. Therefore, a larger $\Delta i_L$ corresponds to more power extraction from $v_{EMF,R}$ (i.e., a larger $P_{EMF,R}$). Unfortunately, the pickup coil’s self-inductance, $L_R$, impedes the change of coil current, such that the low $v_{EMF,R}$ voltage source can only generate a small $\Delta i_L$ (Equation 4.1). And although the converter has the capacity to generate larger voltages (i.e., $V_{RECT}$), it only applies them for enough time to de-energize $L_R$ and set $i_L$ back to zero. If, however, the active diodes were replaced with switches so that the converter could apply these voltages for a longer time, then a larger peak-to-peak value of $i_{L(TRAP)}$ could form and more power could be extracted. From an energy investment perspective, the switches would allow for the bi-directional flow of current and power, so that the converter could source the additional energy into $L_R$ that is required to generate the larger peak-to-peak values of $i_L$. These ideas bring forth the motivation for the newly proposed energy investing power receiver in the following section.

### 5.4 Proposed Energy-investment Scheme

The proposed energy-investing scheme shown in Figure 5.8 facilitates bi-directional power flow by replacing the uni-directional active diodes with switches. Bi-directional power flow allows the converter to invest additional energy into $L_R$, which is needed to generate the larger peak-to-peak values of $i_L$ that draw more power from $v_{EMF,R}$. 
Figure 5.8. States of the proposed energy-investment scheme: (a) initial investment, (b) positive energize, (c) positive de-energize/invest, (d) negative energize, and (e) negative de-energize/invest.
Operation begins when $v_{EMF,R}$ transitions positive, at which point an initial investment of energy is transferred from $V_{RECT}$ to $L_R$, as shown in Figure 5.8a. To do so, switches $S_N^+$ and $S_P^-$ close so that $i_L$ quickly ramps up to $I_{INV}$. During this time, the current flowing into $V_{RECT}$, i.e., $i_{RECT}$, is negative such that $V_{RECT}$ invests energy into $L_R$. After the desired $I_{INV}$ develops, $S_P^-$ opens and $S_N^-$ closes to short-circuit the pickup coil and allow the higher valued $i_L$ to continue flowing in-phase with $v_{EMF,R}$, as shown in Figure 5.8b. Just prior to the $v_{EMF,R}$ positive-to-negative transition, $S_N^+$ opens and $S_P^+$ closes to quickly ramp $i_L$ down to $-I_{INV}$ to ensure that $v_{EMF,R}$ and $i_L$ remain in phase, as is shown in Figure 5.8c. During this state, energy first transfers into $V_{RECT}$ when $i_L$ is positive and is then sourced by $V_{RECT}$ when $i_L$ is negative, but overall results in a positive net energy transfer to $V_{RECT}$. After which, as shown in Figure 5.8d, $S_P^+$ opens and $S_N^+$ closes to again short-circuit the coil and again allow the higher valued $|i_L|$ to continue flowing in-phase with $v_{EMF,R}$ (i.e., both have a negative polarity). Finally, $S_N^-$ opens and $S_P^-$ closes just prior to the $v_{EMF,R}$ negative-to-positive transition to again ensure that $v_{EMF,R}$ and $i_L$ remain in phase, as shown in Figure 5.8e. After which, a new cycle begins with Table 5.1 summarizing the switch positions and pickup coil voltages. Furthermore, Figure 5.9 displays the steady-state waveforms of the energy investment scheme.

**TABLE 5.1 STATE DIAGRAM**

<table>
<thead>
<tr>
<th>State of $v_{EMF,R}$</th>
<th>Duration</th>
<th>$v_{CONV} = v_{SW^+} - v_{SW^-}$</th>
<th>$S_N^+$</th>
<th>$S_D^+$</th>
<th>$S_N^-$</th>
<th>$S_D^-$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$-/+$ Transition +</td>
<td>$\tau_{RECT}$</td>
<td>$-V_{RECT}$</td>
<td>On</td>
<td>Off</td>
<td>Off</td>
<td>On</td>
</tr>
<tr>
<td>$-/+$ Transition -</td>
<td>$\tau_{EN^+}$</td>
<td>0</td>
<td>On</td>
<td>Off</td>
<td>On</td>
<td>Off</td>
</tr>
<tr>
<td>$-/+$ Transition -</td>
<td>$\tau_{RECT^-}$</td>
<td>$V_{RECT}$</td>
<td>Off</td>
<td>On</td>
<td>On</td>
<td>Off</td>
</tr>
<tr>
<td>$-/+$ Transition +</td>
<td>$\tau_{EN^-}$</td>
<td>0</td>
<td>On</td>
<td>Off</td>
<td>On</td>
<td>Off</td>
</tr>
</tbody>
</table>
Determining the power extraction (i.e., $P_{\text{EMF},R}$) for this proposed scheme amounts to deriving $I_{\text{LIN}}$ as $P_{\text{EMF},R} = V_{\text{EMF},R}I_{\text{LIN}}/2$ (from Equation (5.12)). In order to determine the value of $I_{\text{LIN}}$, it is useful to view $i_L$ as being driven by the superposition of both $v_{\text{EMF},R}$ and $v_{\text{CONV}}$ voltages as shown in Figure 5.10, such that $i_L$ is

$$i_L = i_{L(\text{EMF},R)} + i_{L(\text{CONV})}, \quad (5.35)$$

where

$$i_{L(\text{EMF},R)} = i_L \bigg|_{v_{\text{CONV}}=0} = \frac{\int_{0}^{\text{v}_{\text{EMF},R}} v_{\text{EMF},R} \ dt}{L_R} \quad (5.36)$$

and

$$i_{L(\text{CONV})} = i_L \bigg|_{v_{\text{EMF},R}=0} = \frac{\int_{0}^{\text{v}_{\text{CONV}}} v_{\text{CONV}} \ dt}{L_R}. \quad (5.37)$$

The term arising from the $v_{\text{EMF},R}$ voltage equals
\[ i_{L(VEMF,R)} = i_L = \int_{v_{pc}=0} V_{EMF,R} L_R dt = \int \frac{V_{EMF,R} \sin(\omega_o t)}{L_R} dt = -\frac{V_{EMF,R} \cos(\omega_o t)}{\omega_o L_R}, \] (5.38)

such that \( i_{L(VEMF,R)} \)'s amplitude equals

\[ I_{L(VEMF,R)} = \frac{V_{EMF,R}}{\omega_o L_R}. \] (5.39)

Figure 5.10 Construction of \( i_L \) as the superposition of the current generated by \( v_{EMF,R} \) (i.e., \( i_{L(VEMF,R)} \)) and current generated by \( v_{CONV} \) (i.e., \( i_{L(VCONV)} \)).
Notice that the $i_{L(\text{VEMF,R})}$ term is out-of-phase with $v_{\text{EMF,R}}$ so that it does not contribute to $P_{\text{EMF,R}}$. However, the term generated by the $v_{\text{CONV}}$ voltage (i.e., $i_{L(\text{VCONV})}$) is in-phase with $v_{\text{EMF,R}}$ as shown in Figure 5.10. $i_{L(\text{VCONV})}$’s trapezoidal waveform has an amplitude of $I_{\text{INV}} + \Delta iL/2$ and a rise/fall time of $\tau_{\text{RECT}}$. Furthermore, notice that $i_{L(\text{VCONV})}$ is of the same form as the previous scheme’s $i_{L(\text{TRAP})}$ from Figure 5.7, but can be made to have a larger peak-to-peak value by extending $\tau_{\text{RECT}}$. This larger peak-to-peak waveform contains a larger fundamental component, which allows this scheme to draw more average power. In particular, $i_{L(\text{VCONV})}$’s fundamental component can be calculated from Fourier analysis to equal

$$I_{L(IN)} = 2 \frac{\tau_{\text{EN}}}{T_{O}} \int_{0}^{T_{O}} i_{L(\text{VCONV})} \sin(\omega_{O}t)dt = \frac{4}{\pi} \frac{V_{\text{RECT}} \sin \left( \pi \frac{\tau_{\text{RECT}}}{T_{O}} \right)}{\omega_{O}L_{R}}. \quad (5.40)$$

As such, the power extraction is

$$P_{\text{EMF,R}} = \frac{V_{\text{EMF,R}} I_{L(IN)}}{2} = \frac{2}{\pi} \frac{V_{\text{EMF,R}} V_{\text{RECT}} \sin \left( \pi \frac{\tau_{\text{RECT}}}{T_{O}} \right)}{\omega_{O}L_{R}}. \quad (5.41)$$

Notice that $I_{L(IN)}$ increases with extended $\tau_{\text{RECT}}$ up until the limiting case in which $\tau_{\text{EN}}$ goes to zero, which corresponds to a $\tau_{\text{RECT}}$ equal to $T_{O}/2$, as shown in Figure 5.11. For that extreme case, $I_{L(IN)}$ equals its maximum value, namely

$$\max \left\{ I_{L(IN)} \right\} = I_{L(IN)} \bigg|_{\tau_{\text{RECT}} = T_{O}/2} = \frac{4}{\pi} \frac{V_{\text{RECT}}}{\omega_{O}L_{R}}.$$

![Figure 5.11. $\tau_{\text{RECT}}^+$ and $\tau_{\text{RECT}}^-$ set to $T_{O}/2$ to produce the maximum $I_{L(IN)}$ for this topology.](image)
To compare the power extracting capabilities of the previous inductive rectifying scheme of Chapter 4, the resonant receiver found in the literature, and the proposed energy-investment scheme, the negligible loading condition is assumed (i.e., $v_{EMF,R}$’s amplitude is unaffected by loading). This assumption is made for simplicity, but will be reinvestigated in the investment limitations section of this chapter. Assuming the negligible loading condition, the maximum power $P_{EMF,R}$ of the proposed energy investing scheme equals

$$\max \{P_{EMF,R}\} = \frac{V_{EMF,R} \cdot \max \{I_{L(IN)}\}}{2} = \frac{2 \cdot V_{EMF,R} \cdot V_{RECT}}{\pi \cdot \omega_o \cdot L_R}. \quad (5.43)$$

Table 5.2 showcases the maximum $P_{EMF,R}$ for the inductive rectifying power receiver of Chapter 4, the proposed energy-investment power receiver, and the resonant power receiver found in the literature. The table highlights that the proposed energy-investment receiver has the potential to extract the most power among all of the receivers. Furthermore, when compared to the previous scheme, the proposed receiver has a substantial power extracting gain of $V_{RECT}/V_{EMF,R}$ which is significant for low coil voltages (~100 mV). When compared to the resonant receiver, the power extracting gain is not as substantial, but still yields a 27% increase in power.

**Table 5.2 Comparison of Maximum $P_{EMF,R}$ for Various Wireless Power Receivers**

<table>
<thead>
<tr>
<th></th>
<th>Inductive Rectifying (Chapter 4)</th>
<th>Energy Investment (Proposed)</th>
<th>Resonant Receiver (Literature)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\max {P_{EMF,R}}$</td>
<td>$\frac{2}{\pi} \left( \frac{V_{EMF,R}^2}{\omega_o \cdot L_R} \right)$</td>
<td>$\frac{2}{\pi} \left( \frac{V_{EMF,R} \cdot V_{RECT}}{\omega_o \cdot L_R} \right)$</td>
<td>$\frac{1}{2} \left( \frac{V_{EMF,R} \cdot V_{RECT}}{\omega_o \cdot L_R} \right)$</td>
</tr>
</tbody>
</table>

†Negligible loading condition is assumed.

### 5.4.1 Limitations of Investment

Ideally, this energy investment scheme extracts more $P_{EMF,R}$ with a higher $I_{L(IN)}$; however, there are two cases that limit the extent to which $I_{L(IN)}$ should be increased: the over-damping case and the conduction loss limited case. The first case stems from $I_{L(IN)}$ being
large enough to induce a significant back EMF onto the transmitter coil, represented as $v_{EMF,T}$ in Figure 5.12. This back EMF reduces the peak-to-peak primary current, $i_T$, and therefore the induced $v_{EMF,R}$ voltage seen on the pickup coil. When the loaded $V_{EMF,R}$ voltage is less than half of the unloaded $V_{EMF,R}$ voltage, the system is over-damped so that increases in $I_{L(IN)}$ result in lower $P_{EMF,R}$ [22].

![Figure 5.12](image)

**Figure 5.12.** How a higher $I_{L(IN)}$ induces a back EMF ($v_{EMF,T}$) to reduce transmitter current ($i_T$) and lower the received coil voltage ($v_{EMF,R}$).

The second limitation occurs when the conduction losses associated with the larger coil currents overwhelm the power extraction benefits. This occurs because the conduction losses are at least proportional to $I_{L(IN)}^2$ (at least, because the losses may be higher for power factors less than one) [129], while $P_{EMF,R}$ is at most only proportional to $I_{L(IN)}$ (at most, because of the previously mentioned dampening). Furthermore, the conduction losses are unavoidable, because the pickup coil’s ESR, $R_R$, is in series with $L_R$. As these limitations bound $I_{L(IN)}$, an optimal $I_{L(IN)}$ may be envisioned that corresponds to the maximal power delivered to the load. Finally, it is noted that another form of limitation occurs when the system’s maximal $I_{L(IN)}$ is insufficient to reach either of the two above-mentioned limitations. These limitations will be further examined in the next section of this chapter.
5.5 Prototyped CMOS Energy-investing Wireless Power Receiver

For evaluation purposes, the 180-nm 350 × 700 μm² CMOS wireless power receiver from Chapter 4 was reused with a few modifications that allowed for the testing of this proposed energy investment scheme. The system with its alterations is shown in Figure 5.13. In particular, the modifications included the addition of a synchronizer block and the addition of offset voltages, $V_{OS}$, to the self-synchronizing comparators $C_{PD}^+$ and $C_{PD}^−$ found in the newly labeled $\tau_{RECT}$ controller blocks.

5.5.1 Control

The newly added synchronizer block prompts the system to transition from the energizing state (i.e., $M_N^+$ and $M_N^−$ engaged) to a rectifying state (i.e., either $M_N^+$ and $M_P^−$ engaged or $M_N^−$ and $M_P^+$ engaged) and chooses to which rectifying state to transition dependent on $v_{EMF,R}$’s polarity. $v_{EMF,R}$’s polarity is indirectly sensed through $i_T$, as shown in Figure 5.14, which lags behind $v_{EMF,R}$ by roughly 90° (as $v_{EMF,R} \propto di_T/dt$). The synchronizer block then monitors for $i_T$ zero crossings via comparator $C_{PSYN}$ and delays its output of $S_{SYN}'$ by an adjustable delay of $\tau_{DLY}$ prior to feeding the final $S_{SYN}$ signal into the wireless power receiver circuit. $\tau_{DLY}$ is chosen such that $S_{SYN}$ transitions by a time of $\tau_{RECT}/2$ prior to a $v_{EMF,R}$ zero crossing (as shown in Figure 5.14).
Figure 5.14. Time-domain waveforms used by the synchronizer block to generate the synchronizing signal ($S_{SYN}$).

A HIGH-to-LOW transition of $S_{SYN}$ signifies an anticipated positive-to-negative $v_{EMF,R}$ transition, which from Table 5.1 dictates a transition to the positive side rectifying state (i.e., $M_N^-$ and $M_P^+$ engaged). When a HIGH-to-LOW logic transition of $S_{SYN}$ takes place, the control logic disengages $M_N^+$ with ZVS and allows $L_R$’s current of $i_L$ to raise the switching voltage $v_{SW}^+$ up until the point that comparator $C_P^+$ transitions low to engage $M_P^+$ with another ZVS event and begin the positive side rectifying state. However, unlike conventional active diodes, $C_D^+$ has an intentionally added negative offset voltage of $V_{OS}$, which shifts the value of $i_L$ at which $C_D^+$ trips from zero to $-I_{INV}$ as in Figure 5.14. $V_{OS}$ and $M_P^+$’s switch resistance of $R_P$ define this $I_{INV}$ value, because the voltage drop across $M_P^+$ is $i_L R_P$, such that $C_D^+$ trips HIGH when $i_L R_P$ equals $V_{OS}$ or

$$I_{INV} = \frac{V_{OS}}{R_P}. \quad (5.44)$$
When $C_D^+$ transitions HIGH to mark the end of the $\tau_{RECT}^+$ time, $M_P^+$ disengages with ZVS and the SR latch toggles in preparation for the next energizing state (i.e., $M_N^+$ and $M_N^-$ engaged), but does not yet engage $M_N^+$ because of the ZVD NOR gate. With $M_P^+$ disengaged, $i_L$, which is now negative, inductively discharges $v_{SW}^+$ until the ZVD NOR gate transitions HIGH to finally engage $M_N^+$ with approximate ZVS. After which, an identical process takes place for the second half of the period, with the exception of $S_{SYN}$ making a LOW-to-HIGH logic transition to begin the commutation from the energizing state to the negative rectifying state (i.e., $M_N^+$ and $M_P^-$ engaged).

5.5.2 Power Losses

Power losses of the CMOS implementation, $P_{LOSS}$, reduce the net power transferred to $V_{RECT}$ (i.e., $P_{RECT}$) from the otherwise ideal case of $P_{EMF.R}$:

$$P_{RECT} = P_{EMF.R} - P_{LOSS}. \quad (5.45)$$

The power loss components consist of conduction losses ($P_C$), switching losses ($P_{SW}$), and quiescent losses ($P_Q$). The conduction losses are comprised of the Ohmic losses in the pickup coil’s ESR and the MOSFET’s triode resistances. The ESR’s power loss, $P_{C.R}$, is

$$P_{C.R} = i_{L(RMS)}^2 R_R, \quad (5.46)$$

where $i_{L(RMS)}$ refers to the root-mean-square value of $i_L$, which can be found to equal

$$i_{L(RMS)}^2 = \frac{1}{T_o} \int_0^{T_o} i_L^2 dt = \left( \frac{V_{EMF.R}}{4\omega_L L_R} \right)^2 + \left( \frac{\tau_{RECT} V_{RECT}}{2L_R} \right)^2 \left[ 1 - \frac{4}{3} \left( \frac{\tau_{RECT}}{T_o} \right) \right]. \quad (5.47)$$

When considering the NMOS conduction losses, it is important to recognize that both NMOS switches are engaged during the energizing times ($\tau_{EN}^+$ and $\tau_{EN}^-$) and that only one of the switches is engaged during the rectifying time ($M_N^+$ is engaged during $\tau_{RECT}^-$ and $M_N^-$ is engaged during $\tau_{RECT}^+$). Therefore, the conduction losses associated with the NMOS switches $P_{C,N}$ is
\[ P_{C,N} = i_{L,EN(RMS)}^2 (2R_N) + i_{L,RECT(RMS)}^2 R_N, \]  

(5.48)

where \( R_N \) is the triode resistance of one of the equally sized NMOS switches and \( i_{L,EN(RMS)} \) and \( i_{L,RECT(RMS)} \) are the root-mean-square values of the energizing currents \( i_{L,EN} \) and the rectifying current \( i_{L,RECT} \) shown in Figure 5.15, respectively. The PMOS switches only conduct during the rectifying time and only one conducts each rectifying event (\( M_P^+ \) is engaged during \( \tau_{RECT}^+ \) and \( M_P^- \) is engaged during \( \tau_{RECT}^- \)). As such, the conduction losses associated with the PMOS switches \( P_{C,P} \) is

\[ P_{C,P} = i_{L,RECT(RMS)}^2 R_P, \]  

(5.49)

where \( R_P \) is the triode resistance of one of the equally sized PMOS switches. For completeness, the RMS value of the \( i_{L,EN} \) is

\[ i_{L,EN(RMS)}^2 = \frac{1}{T_O} \int_0^{\tau} i_{L,EN}^2 dt \]

\[ = \left( \frac{V_{EMF,R}}{\omega_o L_R} \right)^2 \left[ \frac{1}{2} - \frac{\tau_{RECT}}{T_O} - \frac{1}{2\pi} \sin \left( 2\pi \frac{\tau_{RECT}}{T_O} \right) \right] + \left( \frac{\tau_{RECT} V_{RECT}}{2L_R} \right)^2 \left( 1 - 2 \frac{\tau_{RECT}}{T_O} \right) \]

(5.50)

and the RMS value of \( i_{L,RECT} \) is

\[ i_{L,RECT(RMS)}^2 = \frac{1}{T_O} \int_0^{\tau} i_{L,RECT}^2 dt \]

\[ = \left( \frac{V_{EMF,R}}{\omega_o L_R} \right)^2 \left[ \frac{\tau_{RECT}}{T_O} + \frac{1}{2\pi} \sin \left( 2\pi \frac{\tau_{RECT}}{T_O} \right) \right] + \left( \frac{\tau_{RECT} V_{RECT}}{2L_R} \right)^2 \left( \frac{2}{3} \frac{\tau_{RECT}}{T_O} \right)^2 \].

(5.51)

Finally, combining all the conduction losses from the pickup coil’s ESR and the MOSFET switches yields

\[ P_c = P_{C,R} + P_{C,N} + P_{C,P}. \]

(5.52)
The system also dissipates power from switching each of the MOSFETs on and off once per cycle. Each MOSFET’s gate capacitance is charged from zero volts to $V_{RECT}$ once per cycle by its corresponding driver. As such, the power required to charge all the MOSFET gates once per cycle is

$$P_{SW,GD} = (2C_{G,N} + 2C_{G,P})V^2_{RECT}f_o,$$  \hspace{1cm} (5.53)

where $C_{G,N}$ and $C_{G,P}$ are the gate capacitances of each of the NMOS and PMOS switch, respectively. It should be noted that this converter does not dissipate any additional switching losses associated with hard switching, namely I-V overlap losses. This is because all the switching events occur with soft switching, specifically zero volt switching, as such the gate drive losses comprise all of the switching losses.

Finally, the last of the losses are the quiescent power losses, $P_Q$, which arise from comparators $CP_{D^+}$ and $CP_{D^-}$, and their associated bias current generator. To conserve power, the control logic only enables $CP_{D^+}$ and $CP_{D^-}$ when they are required (i.e., $\tau_{RECT}^+$ or $\tau_{RECT}^-$), but as the bias generator cannot be disabled, $P_Q$ is
\[ P_Q = P_{\text{BIAS}} + 2P_{\text{CP}} = I_{\text{BIAS}}V_{\text{RECT}} + 2\left( I_{\text{CP}}V_{\text{RECT}} \frac{\tau_{\text{RECT}}}{T_O} \right), \]  

(5.54)

where \( I_{\text{BIAS}} \) and \( P_{\text{BIAS}} \) are the quiescent current and power of the bias current generator and \( I_{\text{CP}} \) and \( P_{\text{CP}} \) is the enabled current and power consumption of each of the comparators.

### 5.5.3 Investment Limitations of the Prototyped Implementation

As mentioned previously, power losses and over-damping limit the extent to which \( I_{L(IIN)} \) should be increased, while the maximal \( \tau_{\text{RECT}} \) time (i.e., \( \max \tau_{\text{RECT}} = T_O/2 \)) limits the extent to which \( I_{L(IIN)} \) can be increased. Note, that this converter adjusts \( I_{L(IIN)} \) by modifying \( \tau_{\text{RECT}} \) with their relationship being monotonic (from Equation 5.40). To quantify when these limitations occur for this prototype, the expression for output power (from Equation (5.45)) is rewritten below

\[ P_{\text{RECT}} = P_{\text{EMF,R}} - P_{\text{LOSS}}. \]  

(5.55)

The power loss limitation occurs when \( dP_{\text{LOSS}}/d\tau_{\text{RECT}} \) exceeds \( dP_{\text{EMF,S}}/d\tau_{\text{RECT}} \), which is to say that increasing \( \tau_{\text{RECT}} \) further increases the losses more than it increases power extracted. Furthermore, as \( P_C \) roughly follows \( \tau_{\text{RECT}}^2 \) (experimentally shown in the following section), \( P_Q \) increases with \( \tau_{\text{RECT}} \), and \( P_{\text{EMF,R}} \) is at most proportional to \( \sin(\pi \tau_{\text{RECT}}/T_O) \), then \( P_{\text{LOSS}} \) can potentially outpace \( P_{\text{EMF,R}} \) with increased \( \tau_{\text{RECT}} \).

The over-damping limitation occurs when increased loading reduces \( V_{\text{EMF,R}} \) to the point that increases in \( \tau_{\text{RECT}} \) actually reduce \( P_{\text{EMF,R}} \) (i.e., \( dP_{\text{EMF,R}}/d\tau_{\text{RECT}} < 0 \)). To quantify the loading, the simplified load model shown in Figure 5.16a replaces the power receiver and introduces an equivalent loading resistor, \( R_{\text{EQ,R}} \), and inductor, \( L_R \), that account for the in-phase and out-of-phase \( i_L \), respectively. It is noted that the higher frequency terms associated with \( i_L \) (and in particular \( i_{L(I(VCONV))} \)) are not modeled, as they would be filtered out by the transmitter’s \( L_T-C_T \) tank anyway. Figure 5.16b displays how the load model
reflects back to the transmitter and highlights that increases in $I_{\text{L(IN)}}$ or coupling (i.e., $k_C$) linearly increase the effective loading resistance, $R_{EQ,T}$, to further dampen the transmitter. Finally, the reflected load also introduces a reactive component, $L_{EQ,T}$, that also loads the transmitter, but is independent of $I_{\text{L(IN)}}$.

![Diagram of Power Transmitter and Load Model]

$M_C = k_C \sqrt{L_T R_T}$

**Figure 5.16.** Equivalent loading model of the (a) receiver and (b) its reflected load.

The final limitation occurs when the system’s maximal $I_{\text{L(IN)}}$ is insufficient to reach either the power losses or the over-dampening limitation. This maximal $I_{\text{L(IN)}}$ occurs when $\tau_{RECT}$ equals $T_o/2$, as described in Equation (5.42), so that

$$\max \left\{ P_{\text{EMF,R}} \right\} = \frac{V_{\text{EMF,R}} \max \left\{ I_{\text{L(IN)}} \right\}}{2} = \frac{2}{\pi} \left( \frac{V_{\text{EMF,R}} V_{\text{RECT}}}{\omega_0 L_R} \right)$$

(5.56)

describes the maximum power this converter can extract given that loading is negligible.

### 5.6 Experimental Results and Performance

#### 5.6.1 Time-domain Waveforms

Figure 5.17 showcases experimental time-domain waveforms of the proposed energy-investment receiver. The figure shows the particular case of an induced coil voltage (i.e., $v_{\text{EMF,R}}$) operating at 125 kHz with an amplitude of 150 mV. Additionally, the converter operates with a $\tau_{RECT}$ of 875 ns, such that the receiver is capable of producing a pickup
coil current of 3.5 mA peak to peak. The experimental time-domain waveforms of Figure 5.17 are of the same profile and in good agreement with theory. Furthermore, notice that during the rectifying times (i.e., $\tau_{RECT}^+$ and $\tau_{RECT}^-$) the voltage across the switching nodes (i.e., $v_{CONV}$) has a slight slant about $V_{RECT}$; the reason being, that the voltage drops across $M_P^+$ and $M_P^-$ depend on $i_L$ during their respective rectifying time. Finally, it is noted, that while the rest of Figure 5.17 was a direct experimental measurement (i.e., using voltage/current probe), $v_{EMF.R}$ cannot be measured directly as the voltage is internal to the coil and is instead calculated from Equation (4.17); however, the transmitter coil’s current as is required in Equation (4.17), was measured experimentally.

5.6.2 Power Coupling Performance

Experimental results show that, at least initially, increasing $\tau_{RECT}$ as a means to increase $I_{L(IN)}$ resulted in an increase in $P_{RECT}$, for both high and low coupling regions, as shown in Figure 5.18. For the low coupling region, defined as negligible transmitter loading, $V_{EMF.R}$ remains fairly constant across $\tau_{RECT}$ so that $P_{EMF.R}$ roughly follows $I_{L(IN)}$ (as $I_{L(IN)} \propto \sin[2\pi\tau_{RECT}/T_o]$). However, $P_{LOSS}$ is non-negligible and increases with $\tau_{RECT}$. As $P_C$
dominates these losses, $P_{LOSS}$ tends to scale with $\tau_{RECT}^2$. Given that $P_{LOSS}$ outpaces $P_{EMF,R}$, there is a maximum $P_{RECT}$ of 81.7 $\mu$W, with the associated optimal $\tau_{RECT}$ time of 1.44 $\mu$s.

Note, that at this optimal $\tau_{RECT}$ time, $P_C$ roughly equals half of the extracted power, $P_{EMF,R}$, a trait corresponding to the theoretical maximal power transfer (i.e., impedance matching) [22]. However, as $P_C$ accounts for more than the losses associated with $R_R$ (i.e., losses associated with $R_N$ and $R_P$) and as there are also non-conductive losses (i.e., $P_Q$ and $P_{SW.GD}$), then the maximum $P_{EMF,R}$ falls just short of the theoretical maximal power point.

For the high coupling regime, defined as non-negligible primary loading, $V_{EMF,R}$ decreases with increased $\tau_{RECT}$, as the increase in $I_{L(IN)}$ induces a back EMF large enough to load the primary. At first, when the $\tau_{RECT}$ time is brief, $P_{EMF,R}$ increases with $\tau_{RECT}$, but
as $\tau_{\text{RECT}}$ lengthens and primary loading increases, the $V_{\text{EMF.R}}$ voltage decreases to the point that larger $\tau_{\text{RECT}}$ times result in a decrease in $P_{\text{EMF.R}}$. While the optimal $\tau_{\text{RECT}}$ is mostly defined by loading, there is still a non-negligible $P_{\text{LOSS}}$ that also limits the $\tau_{\text{RECT}}$ time.

5.6.3 Damping Effects

Adjustment of the $\tau_{\text{RECT}}$ time alters the degree of primary loading, such that the system has the potential to run at different operating points, namely, high efficiency, maximal power, or somewhere in-between. Specifically, as larger $\tau_{\text{RECT}}$ times (i.e., larger $I_{\text{L(IN)}}$) damp the primary, as shown in Figure 5.19, a larger fraction of power flows to the receiver ($P_{\text{EMF.R}}$) rather than being dissipated on the transmitter (via $R_T$), or equivalently, the primary-to-secondary efficiency, $\eta_T$, (defined as $P_{\text{EMF.R}}/P_T$) increases with loading. However, for the total system efficiency, $\eta_{\text{SYS}}$, (defined as $P_{\text{RECT}}/P_T$) to increase, both $\eta_T$ and the receiver’s efficiency, $\eta_R$, (defined as $P_{\text{RECT}}/P_{\text{EMF.R}}$) need consideration. Which is why, although $\eta_T$ increases with larger $\tau_{\text{RECT}}$ for both low and high coupling, $\eta_{\text{SYS}}$ begins decreasing once $P_{\text{LOSS}}$ becomes comparable to $P_{\text{EMF.R}}$ (i.e., $\eta_R$ decreasing). As such, $\eta_{\text{SYS}}$ for the high coupling case improves after the maximal $P_{\text{RECT}}$, while $\eta_{\text{SYS}}$ for the low coupling case does not. Finally, adjusting $\tau_{\text{RECT}}$ to change the loading, allows for the selection of an operating point most suitable for the application.
5.6.4 Optimal Investment

While adjustability of $\tau_{RECT}$ allows for a wide range of operating points, the optimal $\tau_{RECT}$ is defined here as the $\tau_{RECT}$ that delivers the most power to $V_{RECT}$ (maximum $P_{RECT}$). Figure 5.20 shows that the optimal $\tau_{RECT}$ depends on coupling factor, with the optimal $\tau_{RECT}$ being limited by power losses for low coupling factors and over-damping for high coupling factors and some combination in-between for moderate coupling factors. Additionally, Figure 5.20 shows that the maximal $P_{RECT}$ increases with coupling factor. Finally, the ability to adjust $\tau_{RECT}$ is critical for tracking the maximum power point across a wide coupling range, because the coupling factor is highly sensitive to coil separation and angular orientation.
Figure 5.20. Measured maximum output power with corresponding optimal $\tau_{\text{RECT}}$ across coupling factor.

5.7 Summary

Power extraction from a tonal induced coil voltage (i.e., $v_{\text{EMF,R}}$) requires that the coil current (i.e., $i_L$) have a component that is both at the same frequency and in-phase with $v_{\text{EMF,R}}$. While harmonics and out-of-phase components of $i_L$ do not draw power from $v_{\text{EMF,R}}$, they do dissipate power in the coil’s ESR and should be minimized to increase the received power. Available power is a useful comparative benchmark for determining how effective a wireless power receiver is at drawing power, because it equals the maximum achievable power for a given pickup coil. The wireless power receiver must allow for bi-directional power flow to achieve maximum power transfer. Intuitively, this results because the coil’s self-inductance (i.e., $L_R$) has a magnetic energy of $\frac{1}{2}L_Ri_L^2$ that requires supplementary energy in the form of an investment during the peaks and troughs of the power-extracting component of $i_L$. As such, a wireless power receiver that facilitates energy-investments is proposed.

The experimental results of the wireless power receiver demonstrate that investing energy into the pickup coil increases output power. Investing energy, however, both increases the system’s power losses and dampens the power transmitter, which limits the
extent to which investments bring value. As such, an adjustable energy investment, as demonstrated with the 180-nm CMOS prototype, allows for the optimal selection of investment that balances the benefits and limitations to ultimately maximize output power. Increasing output power this way, beyond simply investing a fixed amount, is important in inductively coupled powering, because as coil separation and orientation vary the coupling factor, only an adjustable investment may recalibrate to the new optimal investment value.

While the goal of the CMOS prototype was to assess the efficacy of investing energy, the system required auxiliary information from the synchronizer block to control the prototype. The synchronizer block ultimately derived its timing information from the transmitter current, which is rarely accessible in wireless power transfer applications. As such, Chapter 6 describes a self-synchronizing technique that does not require auxiliary information, so that the wireless power receiver can be integrated into a standalone solution.
Both of the proposed inductive rectifiers in Chapter 4 and Chapter 5 required that their switching events were synchronized with the incoming $v_{EMF,R}$ signal. To do so, a dedicated synchronization block (or $v_{EMF,R}$ polarity detector for Chapter 4) was used to inform the converter when to switch. This block ensured that the switching events and therefore $i_L$ remained synchronized to the $v_{EMF,R}$ signal. Still, this block derived its timing information from the wireless power transmitter (specifically the transmitter current), because the $v_{EMF,R}$ voltage is inaccessible. More specifically, the pickup coil is comprised of the series combination of the $v_{EMF,R}$ voltage and its self-inductance $L_R$ so that there is no direct access to the $v_{EMF,R}$ voltage. Still, a complete inductively-coupled solution cannot rely on the transmitter’s information, because if there was a physical link (i.e., a wire) to convey that information then power could also be transferred across that link, negating the need for wireless powering. As such, this chapter describes and proposes a method to synchronize the wireless power receiver while only using information encoded in the pickup coil (receiver coil). This way a completely wireless solution is possible.

6.1 Synchronization Scheme

The proposed synchronization scheme begins with a calibration phase in which the operational period $T_D$ is sampled. The period information is measured by monitoring the $v_{EMF,R}$ voltage, but as mentioned previously $L_R$ and $R_R$ obstruct direct access to the $v_{EMF,R}$ voltage. However, when the pickup coil is open circuited, as shown in Figure 6.1a, the $v_{EMF,R}$ voltage appears across the terminals of the pickup coil because $i_L$ and $di_L/dt$ are zero and consequently so are the voltage drops across $R_R$ and $L_R$. Then, to measure the operational period, a didactic stopwatch is started when $v_{EMF,R}$ makes a negative-to-
positive transition, as shown in Figure 6.1b. The stopwatch is stopped and its time recorded once $v_{\text{EMF.R}}$ makes another negative-to-positive transition, as shown in Figure 6.1c. The time recorded, $T_{\text{SAM}}$, is the sampled operational period. It is important to note that during calibration no power can be transferred from the $v_{\text{EMF.R}}$ source, because $i_L$ is zero from the open-circuit condition. Therefore, during power transfer $v_{\text{EMF.R}}$ cannot be sensed using this condition and instead the sampled period $T_{\text{SAM}}$ is used to predict $v_{\text{EMF.R}}$’s periodicity during power transfer.

![Diagram](image.png)

*Figure 6.1. (a) Monitoring the $v_{\text{EMF.R}}$ voltage by open circuiting the pickup coil, (b) starting a stopwatch timer to sample $v_{\text{EMF,R}}$’s period and (c) stopping it to record $v_{\text{EMF,R}}$’s period.*
During power transfer the sampled period $T_{SAMP}$ is used to generate a timing reference with which the power converter maintains synchronization with the $v_{EMF,R}$ voltage. For simplicity, the timing reference shown in Figure 6.2 predicts when $v_{EMF,R}$ crosses zero (the implemented timing reference of the built prototype in the following section operates with a phase shift). To detect the $v_{EMF,R}$ zero crossings, the stop watch in Figure 6.2 initially resets with $v_{EMF,R}$ equal to zero. Then half of the sampled operational period $T_{SAMP}/2$ is compared with the running stop watch and when they are equal the stopwatch is reset and the predicted zero crossing information is feed to the power converter. Similarly, once reset the stopwatch continues running until another $T_{SAMP}/2$ has passed and the cycle repeats. Each time the stop watch resets the power converter is informed that a predicted $v_{EMF,R}$ zero crossing has occurred and using that information the power converter can maintain synchronized with the $v_{EMF,R}$ signal.

![Diagram of power transfer](image)

Figure 6.2. Generating timing information by predicting $v_{EMF,R}$’s zero crossings.
6.2 Synchronized Inductively-Coupled Power Receiver

6.2.1 Operation

The prototyped receiver, shown in Figure 6.3, relies on the synchronizer block to orchestrate power transfer from the induced coil voltage, $v_{EMF,R}$, to the output voltage $V_{RECT}$. The synchronizer block produces a square wave, $v_{SYNC}$, which is used to synchronize the switching events of the power receiver with the $v_{EMF,R}$ voltage. For now, the internal details of the synchronizer are deferred to the next subsection, where those details will have appropriate context. This subsection pertains to operation during power transfer with $v_{SYNC}$ taken as a given.

![Diagram](image)

**Figure 6.3.** Prototyped self-synchronizing wireless power receiver (transistor dimensions in μm).

During operation the calibration signal $v_{RECAL}$ is LOW so that all comparators and drivers in Figure 6.3 are enabled. When $v_{EMF,R}$ is in its positive half-cycle and $v_{SYNC}$ is HIGH both NMOS power switches $M_N^+$ and $M_N^-$ engage to short the pickup coil and build current and energy onto the coil’s self-inductance $L_R$, as shown in the power transfer portion of Figure 6.4. Then when prompted by the synchronizer block (with a HIGH-to-LOW $v_{SYNC}$ transition), $M_N^+$ disengages and $M_P^+$ engages with the aid of zero
volt switching (ZVS) comparator $CP_{ZVS,P}^+$ to deliver charge to $V_{RECT}$. $M_P^+$ remains engaged until the tunable delay block, $\tau_{RECT}$, prompts $M_P^+$ to disengage. During this time the coil current reverses, which corresponds to an energy investment, in preparation for the negative half-cycle. When $M_P^+$ disengages, ZVS comparator $CP_{ZVS,N}^+$ cues $M_N^+$ to shut and again short the pickup coil. During the negative half-cycle the receiver operates in a symmetrical fashion to that during the positive half-cycle, by first transferring energy from the $v_{EMF,R}$ source to the coil’s self-inductance. Then, when $v_{SYNC}$ transitions HIGH, $M_N^-$ opens and $M_P^-$ shuts with instruction from $CP_{ZVS,P}^-$ to deliver charge to $V_{RECT}$. After delay $\tau_{RECT}$, when the coil current has again reversed, $M_P^-$ disengages. Finally, comparator $CP_{ZVS,N}^-$ commands $M_N^-$ to engage during the positive half-cycle to complete a full $v_{EMF,R}$ operational period, $T_O$. The operation repeats every cycle until the system signals to recalibrate the synchronizer block.

![Diagram of switching nodes and voltages](image)

**Figure 6.4.** Extrapolated induced coil voltage $v_{EMF,R}$ and synchronizing $v_{SYNC}$ from measured coil current $i_L$ and switching nodes $v_{SW}^+$ and $v_{SW}^−$. 

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6.2.2 Calibration

The synchronizer block, partially shown in Figure 6.5, operates under two phases: calibration and prediction. The purpose of the calibration phase is to sense and record \( v_{EMF,R} \)'s period \( T_O \). To do so, power transfer halts to allow sense switches \( M_{SEN}^+ \) and \( M_{SEN}^- \) to connect the coil to a sense resistor \( R_{SEN} \) that is of much higher impedance than \( L_R \) (i.e., \( R_{SEN} \gg \omega O L_R \)). As such, the voltage across \( R_{SEN} \) approximately equals the induced coil voltage, as shown on \( v_{SW}^+ \) node of Figure 6.6. Comparator \( CP_{SEN} \), which samples the polarity of that voltage, trips from LOW to HIGH when \( v_{EMF,R} \) makes a negative-to-positive transition and starts a prediction counter, \( CNT_{PRED} \). The idea here is to record the operational period into an equivalent number of clock cycles, so that after a complete period when \( CP_{SEN} \) makes another LOW-to-HIGH transition, register \( REG_{PRED} \) stores the running count for use during the prediction phase. After storing the count, the counter resets and the prediction phase begins.

![Figure 6.5. Calibrating the synchronizer by sampling operational period and storing it as an equivalent number of clock pulses (transistor dimensions are in \( \mu \text{m} \)).](image-url)
6.2.3 Synchronization

At the end of calibration, when \( v_{EMF,R} \) enters its positive half-cycle, \( M_{SEN}^+ \) and \( M_{SEN}^- \) open, \( CNT_{PRED} \) resets, and \( L_R \) starts energizing from \( v_{EMF,R} \), as Figure 6.6 shows at 11 and 82 \( \mu \)s. For the first \( \tau_{EN}^+ \), when the HIGH-if-equal logic in Figure 6.7 determines that \( CNT_{PRED} \) reaches half \( REG_{PRED} \)'s recorded count minus the predetermined phase correct value, \( CNT_{PRED} \) resets and \( v_{SYNC} \) commands \( L_R \) to drain into \( V_{RECT} \) just prior to the \( v_{EMF,R} \) positive-to-negative transition. The phase correct value corresponds to the equivalent number of clock pulses that equals half of \( \tau_{RECT} \), so that \( L_R \) begins de-energizing by a time of \( \tau_{RECT}/2 \) prior to the \( v_{EMF,R} \) zero crossing. After \( \tau_{RECT} \), \( L_R \) energizes from \( v_{EMF,R} \) during the negative half-cycle until a time of \( \tau_{RECT}/2 \) prior to the next \( v_{EMF,R} \) zero crossing. To implement this, the phase correct block disables and \( CNT_{PRED} \) counts to half of \( REG_{PRED} \)'s recorded value, which toggles \( v_{SYNC} \) and resets \( CNT_{PRED} \). After this, another half-cycle sequence begins and the process repeats with the phase correct block remaining disabled. Note that for the case where the stored count in \( REG_{PRED} \) is odd, dividing by two is not possible, as such, a 0.5-bit correction block adds the odd bit every other half cycle to correct for the error after an entire cycle.
Figure 6.6 highlights that when transitioning from calibration to power transfer, $i_L$ initially has a negative dc offset, which later decays to zero. This decay is analogous to the exponential decay found in a series $RL$ circuit with a time constant of $L/R$. The dc component of $i_L$ goes to zero because the average voltage across the series combination of $L_R$ and $R_R$ over an entire period is zero. The average voltage across $L_R$ and $R_R$ is zero because $v_{EMF,R}$ has no dc component and because $v_{SW^+}$ and $v_{SW^-}$ are symmetric so that their average voltages equal and therefore cancel. For further intuition, a dc perspective is employed, where $L_R$ becomes a short and $R_R$ experiences zero dc voltage, all of which results in $i_L$ having a dc component of zero.

For further intuition, a dc perspective is employed, where $L_R$ becomes a short and $R_R$ experiences zero dc voltage, all of which results in $i_L$ having a dc component of zero.

**Figure 6.7.** Functional diagram of synchronizer during power transmission.

### 6.2.4 Calibration Error

Because the internal clock frequency $f_{CLK}$ has no correlation with $v_{EMF,R}$’s operational frequency, an integer number of $T_{CLK}$ periods does not normally fit into the continuous-valued operational period $T_O$. As a result, the effective time recorded in $REG_{PRED}$ has a quantization error of

$$-T_{CLK} \leq \Delta t_{ERR(Q)} \leq T_{CLK},$$

where $\Delta t_{ERR(Q)}$ is the quantization error. This error results in the receiver draining $L_R$ into $V_{RECT}$ slightly ahead or slightly behind the ideal time (i.e., $\tau_{RECT}/2$ before $v_{EMF,R}$’s zero crossing). Whether under or over forecasted, this quantization error compounds after each $v_{EMF,R}$ cycle, because the synchronizer continues to reuse the same erroneously sampled
operational period with each prediction. As such, \( v_{SYNC} \)'s phase with respect to \( v_{EMF,R} \) drifts with time. So that \( v_{SYNC} \)'s phase deviates from its ideal case (i.e., no quantization error) with a phase error \( \Delta \theta \) of

\[
\Delta \theta = \omega_o t - \omega_{SYNC} t,
\]

where \( t \) is the time since the end of the calibration and \( \omega_{SYNC} \) is the angular frequency of \( v_{SYNC} \), which is expressed as

\[
\omega_{SYNC} = \frac{2\pi}{T_o + \Delta \tau_{ERR(Q)}}.
\]

Combining Equation (6.2) and Equation (6.3) yields

\[
\Delta \theta = \frac{\Delta \tau_{ERR(Q)}}{T_o} \left( \frac{1}{1 + \Delta \tau_{ERR(Q)}/T_o} \right) \omega_o t.
\]

Equation (6.4) states that given a \( \Delta \tau_{ERR(Q)} \) (other than zero), the phase error between \( v_{EMF,R} \) and \( v_{SYNC} \) increases with time. This \( \Delta \theta \) can be thought of as the beat frequency between \( v_{EMF,R} \) and \( v_{SYNC} \). Figure 6.8 highlights that if \( \Delta \tau_{ERR(Q)} \) is negative then \( v_{SYNC} \) and consequently \( i_L \) is fast and if \( \Delta \tau_{ERR(Q)} \) is positive then \( v_{SYNC} \) and consequently \( i_L \) is slow with respect to \( v_{EMF,R} \).

![Figure 6.8. Measured coil currents for positive (slow) and negative (fast) quantization errors \( \Delta \tau_{ERR(Q)} \).](image)

As a limiting case, the phase error should not grow to the extent that \( v_{EMF,R} \) and \( v_{SYNC} \) are 90° out of phase, because that would correspond to the case that \( v_{EMF,R} \) and \( i_L \)
are also $90^\circ$ out of phase and have zero power factor where there is no longer power being drawn. As such, the system recalibrates after $CNT_{\text{RECAL}}$ in Figure 6.7 counts $N_{\text{PER}}$ number of $v_{\text{EMF,R}}$ periods, which for the example case of Figure 6.6 is 7 periods. To avoid investing energy in $L_R$ just prior to transitioning into calibration, where that energy would be lost, $v_{\text{RECAL}}$ shuts $M_p^+$ and allows diode-connected $M_D$ in Figure 6.3 to asynchronously drain $L_R$ entirely, as Figure 6.6 shows when $i_L$ falls to zero near 70 $\mu$s.

### 6.3 Power Transfer

Under ideal conditions (i.e., without quantization error) the power drawn from the $v_{\text{EMF,R}}$ source, as was derived in Chapter 5, would be

$$P_{\text{EMF,R(\text{Ideal})}} = \frac{1}{T_O} \int_0^{T_O} v_{\text{EMF,R}}i_L dt = \frac{2}{\pi} \frac{V_{\text{EMF,R}} V_{\text{RECT}} \sin \left( \frac{\pi \tau_{\text{RECT}}}{T_O} \right)}{\omega_0 L_R},$$

(6.5)

where $P_{\text{EMF,R(\text{Ideal})}}$ is the ideal power drawn and $V_{\text{EMF,R}}$ is the amplitude of $v_{\text{EMF,R}}$. With quantization, however, the power drawn from the $v_{\text{EMF,R}}$ source decreases because $i_L$ is either fast or slow with respect to $v_{\text{EMF,R}}$. To quantify this, $i_L$, as was defined in Equation (5.35), must be altered to account for drift. In particular, the fundamental component of $i_L$ that was once entirely in-phase with $v_{\text{EMF,R}}$, i.e., $I_{L(IN)}$ from Equation (5.40) now operates with a $\Delta \theta$ phase error, such that that power extraction with quantization error $P_{\text{EMF,R(Err)}}$ equals

$$P_{\text{EMF,R(Err)}} = \frac{1}{(N_{\text{PER}} + 2)T_O} \int_0^{(N_{\text{PER}} + 1/2)T_O} v_{\text{EMF,R}}i_L dt.$$

(6.6)

Note that $P_{\text{EMF,R(Err)}}$ accounts for the lack of energy transfer during calibration by averaging the power across a time of $(N_{\text{PER}}+2)T_O$ while only integrating over a time of $(N_{\text{PER}}+1/2)T_O$ (the additional $1/2$ term in the bounds of integration considers that the last de-
energizing event always occurs on an odd-numbered half-cycle). For further simplification, Equation (6.4) is inserted into Equation (6.5) and trigonometric identities are employed to yield

\[
P_{\text{EMF,R(ERR)}} = \frac{V_{\text{EMF,R}}}{{N_{\text{PER}} + 2}} \int_0^{\frac{N_{\text{PER}} + 1/2}{T_o}} \frac{1}{2} \left[ \cos \left( \frac{\Delta \tau_{\text{ERR}(Q)}}{T_o} \right) \right] + \cos \left( \frac{2 + \Delta \tau_{\text{ERR}(Q)}}{1 + \Delta \tau_{\text{ERR}(Q)}} \right) dt, \tag{6.7}
\]

which reduces significantly with the \(\Delta \tau_{\text{ERR}(Q)} < T_o\) approximation:

\[
P_{\text{EMF,R(ERR)}} = \frac{V_{\text{EMF,R}}}{{N_{\text{PER}} + 2}} \int_0^{\frac{N_{\text{PER}} + 1/2}{T_o}} \frac{1}{2} \left[ \cos \left( \frac{\Delta \tau_{\text{ERR}(Q)}}{T_o} \right) \right] + \cos \left( 2\omega_o t \right) dt. \tag{6.8}
\]

Then, integrating yields the \(P_{\text{EMF,R(ERR)}}\) for a given \(\Delta \tau_{\text{ERR}(Q)}\) to equal

\[
P_{\text{EMF,R(ERR)}} = \frac{1}{2} V_{\text{EMF,R}} I_{\text{L(IN)}} \left( \frac{N_{\text{PER}} + 1/2}{N_{\text{PER}} + 2} \right) \sin \left[ 2\pi \frac{\Delta \tau_{\text{ERR}(Q)}}{T_o} \left( \frac{N_{\text{PER}} + 1/2}{N_{\text{PER}} + 2} \right) \right], \tag{6.9}
\]

where the cardinal sine function \(\text{sinc}(x) = \sin(x)/x\). Finally, Equation (6.9) can be rewritten as a function of the ideal power extraction to produce

\[
\frac{P_{\text{EMF,R(ERR)}}}{P_{\text{EMF,R(IDEAL)}}} = \left( \frac{N_{\text{PER}} + 1/2}{N_{\text{PER}} + 2} \right) \sin \left[ 2\pi \frac{\Delta \tau_{\text{ERR}(Q)}}{T_o} \left( \frac{N_{\text{PER}} + 1/2}{N_{\text{PER}} + 2} \right) \right]. \tag{6.10}
\]

Before proceeding, it is worth investigating Equation (6.10). First, note that when \(\Delta \tau_{\text{ERR}(Q)}\) is zero and \(N_{\text{PER}}\) goes to infinity \(P_{\text{EMF,R(ERR)}}\) equals \(P_{\text{EMF,R(IDEAL)}}\), which makes intuitive sense because there is no quantization error and the fraction of time spent calibrating goes to zero. Second, notice that increasing \(\Delta \tau_{\text{ERR}(Q)}\) always decreases \(P_{\text{EMF,R(ERR)}}\) (within reasonably small \(\Delta \tau_{\text{ERR}(Q)}: \Delta \tau_{\text{ERR}(Q)} < T_o\), yet increasing \(N_{\text{PER}}\) initially increases \(P_{\text{EMF,R(ERR)}}\) and then decreases \(P_{\text{EMF,R(ERR)}}\) with larger values. The trend of \(P_{\text{EMF,R(ERR)}}\) with regard to \(N_{\text{PER}}\) results because when \(N_{\text{PER}}\) is small increasing \(N_{\text{PER}}\) decreases the fraction of time that the receiver is calibrating with no power transfer and when \(N_{\text{PER}}\) is large the phase error \(\Delta \theta\) has grown to such an extent that synchronization errors dominate. Lastly, \(\Delta \tau_{\text{ERR}(Q)}\) is a random variable that originated during the sampling
process of $T_O$ and quantifying its effects on the average power drawn from $v_{EMF,R}$ amounts to determining the expected value of $P_{EMF,R(ERR)}$, which is expressed as

$$E[P_{EMF,R(ERR)}] = \int P_{EMF,R(ERR)} \, PDF (\Delta\tau_{ERR(Q)}) \, d\Delta\tau_{ERR(Q)},$$

(6.11)

where $PDF(\cdot)$ is the probability density function of $\Delta\tau_{ERR(Q)}$. It is assumed here that the random variable $P_{EMF,R(ERR)}$ is ergodic, such that its time average and ensemble average equal, which was validated with experimental results. For simplicity the distribution is assumed to be uniform across the range of $\Delta\tau_{ERR(Q)}$, such that

$$PDF (\Delta\tau_{ERR(Q)}) = \text{unif}(-T_{CLK}, T_{CLK}) = \frac{1}{2T_{CLK}}. \tag{6.12}$$

Then, inserting Equation (6.12) and Equation (6.10) into Equation (6.11) yields

$$E[P_{EMF,R(ERR)}] = \frac{1}{2T_{CLK}} \int_{-T_{CLK}}^{T_{CLK}} P_{EMF,R(Ideal)} \left( \frac{N_{PER} + 1/2}{N_{PER} + 2} \right) \sin \left[ 2\pi \frac{\Delta\tau_{ERR(Q)}}{T_O} \left( \frac{N_{PER} + 1/2}{N_{PER} + 2} \right) \right] d\Delta\tau_{ERR(Q)}, \tag{6.13}$$

where $\Delta\tau_{ERR(Q)}$ has a uniform distribution between $-T_{CLK}$ and $T_{CLK}$. This expression can be further simplified to

$$E[P_{EMF,R(ERR)}] = \frac{N_{PER} + 1/2}{N_{PER} + 2} \frac{\sin \left[ 2\pi \frac{f_o}{f_{CLK}} \left( \frac{N_{PER} + 1/2}{N_{PER} + 2} \right) \right]}{2\pi \frac{f_o}{f_{CLK}} \left( \frac{N_{PER} + 1/2}{N_{PER} + 2} \right)}, \tag{6.14}$$

which is plotted in Figure 6.9 and where $\text{Si}(x)$ is the sine integral function described by

$$\text{Si}(x) = \int_0^x \frac{\sin u}{u} \, du. \tag{6.15}$$

Figure 6.9 reinforces the previously observed trend with increasing $N_{PER}$, viz., an initial increase in $P_{EMF,R(ERR)}$ followed by a maximum $P_{EMF,R(ERR)}$ and finally a decrease in $P_{EMF,R(ERR)}$ for large $N_{PER}$. The plot also displays a family of curves of $f_{CLK}$, which emphasis that a higher $f_{CLK}$ frequency limits the quantization error $\Delta\tau_{ERR(Q)}$, such that the
synchronizer can predict more operational periods before drift and de-synchronization hinder power extraction.

Figure 6.9. Fraction of power extraction \( P_{\text{EMF,R(ERR)}} \) with quantization error and calibration compared to the ideal case \( P_{\text{EMF,R(IDEAL)}} \) over number of predictions \( N_{\text{PER}} \) and clock frequencies \( f_{\text{CLK}} \).

### 6.3.1 Power Loss

This receiver dissipates power via clock generation \( P_{\text{OSC}} \), digital losses \( P_{\text{DIG}} \), conduction losses \( P_{C} \), switching losses \( P_{SW} \), and quiescent losses \( P_{Q} \). Furthermore, opportunity loss \( P_{\text{LOST}} \) quantifies the missed power that could have been sourced by \( v_{\text{EMF,R}} \) if there was perfect synchronization, which is expressed as

\[
P_{\text{LOST}} = P_{\text{EMF,R(IDEAL)}} - P_{\text{EMF,R(ERR)}}
\]  

(6.16)

and with Equation (6.14) reduces to

\[
P_{\text{LOST}} = P_{\text{EMF,R(IDEAL)}} \left\{ 1 - \left( \frac{N_{\text{PER}} + 1/2}{N_{\text{PER}} + 2} \right) \sin \left( \frac{2\pi f_{O}}{f_{\text{CLK}}} \left( \frac{N_{\text{PER}} + 1/2}{N_{\text{PER}} + 2} \right) \right) \right\},
\]

(6.17)

which is plotted in Figure 6.10 for various clock frequencies. As can be seen, the percentage of \( P_{\text{EMF,R(IDEAL)}} \) that is missed as an opportunity loss first begins decreasing with \( N_{\text{PER}} \). This is because increasing \( N_{\text{PER}} \) decreases the fraction of time that the receiver is calibrating and no power transfers. However, as \( N_{\text{PER}} \) continues increasing the phase
error grows to the extent that de-synchronization becomes dominant, which is why there is a minimum in $P_{LOST}$. Also, notice that because faster clock frequencies are more accurate in recording the period, they can forecast a higher $N_{PER}$ before $\Delta \theta$ becomes significant.

![Figure 6.10. Opportunity loss $P_{LOSS}$ as a function of the number of predictions $N_{PER}$ and clock frequency $f_{CLK}$.](image)

Increasing the clock frequency has its own tradeoff, because if the clock generation is done via a relaxation oscillator, as it is for this system, the oscillator must replenish the energy it dissipates in setting the oscillation frequency every cycle. For this implementation, the relaxation oscillator charges and discharges capacitor $C_{OSC}$ by $\Delta V_{OSC}$ and consumes a power of

$$P_{OSC} = E_{OSC} f_{CLK} = \left( C_{OSC} \Delta V_{OSC}^2 \right) f_{CLK}. \quad (6.18)$$

Additionally, as all the digital circuitry is clocked at $f_{CLK}$, the gate driving losses of the digital circuitry also increases with $f_{CLK}$ and equals

$$P_{DIG} = C_{DIG} V_{RECT}^2 f_{CLK}, \quad (6.19)$$

where $C_{DIG}$ is the total effective capacitance seen by the clock signal. And although clock gating and a specialized minimum-latch architecture were implemented, $P_{DIG}$ consumed a significant fraction of all but the conduction losses.
As for the conduction losses, the pickup coil’s equivalent series resistance $R_R$, CMOS switches $M_N^+$, $M_N^-$, $M_P^+$, and $M_P^-$, and diode-connected $M_D$ all dissipate power. $R_R$, $M_N^+$, and $M_N^-$ consume power during $\tau_{EN}^+$ and $\tau_{EN}^-$, while $R_R$, $M_N^-$, and $M_P^+$ (and $M_N^+$ and $M_P^-$) consume power across $\tau_{RECT}^+$ (and $\tau_{RECT}^-$). Finally, $M_D$ consumes power on the final de-energizing event prior to calibration. Collecting terms results in

$$
P_C = i_{L(RMS)}^2 R_R + i_{L\text{SHORT}(RMS)}^2 R_{MN} + i_{L \text{BAT}(RMS)}^2 (R_{MN} + R_{MP}) + i_{D(AVG)} v_{SG.D},$$

(6.20)

where $R_{MN}$ and $R_{MP}$ are n- and p-type MOS triode resistance, and $v_{SG.D}$ is the on voltage for diode-connected $M_D$.

$V_{RECT}$ also consumes energy in charging each CMOS switch’s gate capacitance once per cycle. As a result, charging each n- and p-type gate-capacitance of $C_{GN}$ and $C_{GP}$ consumes

$$
P_{sw} = (2 C_{GN} + 2 C_{GP}) V_{RECT}^2 f_o \left( \frac{N_{PER} + 1/2}{N_{PER} + 2} \right).$$

(6.21)

The additional fraction consisting of $N_{PER}$ accounts for the halt in gate driving during calibration. Lastly, all of the following functional blocks consume quiescent power: the current bias $P_{BIAS}$, zero-volt switching (ZVS) comparators $P_{ZVS}$, $\tau_{RECT}$ delay timer $P_{TMR}$, and sense comparator $P_{SENSE}$. To save power, the timer is only enabled when required to generate a delay and similarly the sense comparator is only enabled during the calibration time. Collecting terms results in the a quiescent power of

$$
P_Q = P_{BIAS} + P_{ZVS} + P_{TMR} \left( \frac{2 \tau_{RECT}}{T_o} \right) \left( \frac{N_{PER} + 1/2}{N_{PER} + 2} \right) + P_{SENSE} \left( \frac{3/2}{N_{PER} + 2} \right).$$

(6.22)

### 6.4 Integrated Circuit

#### 6.4.1 Power Stage

As was described in the operation section, comparators $CP_{ZVS.N^+}$, $CP_{ZVS.N^-}$, $CP_{ZVS.P^+}$, and $CP_{ZVS.P^-}$ designate when to engage their respective CMOS switch (viz., $M_N^+$, $M_N^-$, $M_P^+$, $M_P^-$).
and $M_F^-$, respectfully), and more than that, they do so with ZVS. The comparators accomplish ZVS because they directly monitor the drain to source voltage of the CMOS switches and wait until the voltage drop across the switch is approximately zero before engaging the switch. Moreover, the parasitic winding capacitance $C_{PAR}$ of the pickup coil (shown in Figure 6.3) aids in ZVS when the CMOS switches open, because $C_{PAR}$ limits the $dv/dt$ of the switching nodes $v_{SW^+}$ and $v_{SW^-}$ so that drain to source voltage of the switch remains constant and roughly equal to zero when opening. Finally, resistive charging and discharging of parasitic $C_{PAR}$, as the name suggests, would normally drain energy from the system, but as the charging and discharging is done inductively (or adiabatically) with $L_R$, the energy deposited onto $C_{PAR}$ ultimately returns back to $L_R$.

![Figure 6.11](image_url)

Figure 6.11. (a) High-side and (b) low-side zero volt switching comparators $CP_{ZVS.P}$ and $CP_{ZVS.N}$, respectfully (transistor dimensions are in μm).

The high-side ZVS comparators $CP_{ZVS.P^+}$ and $CP_{ZVS.P^-}$ as well as the low-side ZVS comparators $CP_{ZVS.N^+}$ and $CP_{ZVS.N^-}$ use a common gate input stage, as shown in Figure 6.11. This topology offers a common-mode input range that accommodates above-rail comparisons for the high-side comparators and below-ground comparison for the low-side comparators. Furthermore, when $v_{SW}$ goes above $V_{RECT}$ in Figure 6.11a or when $v_{SW}$ goes below ground in Figure 6.11b, common gate $M_{GC2}$ does not suffer from conventional slew rate limitations and if overdriven drives large currents for a fast comparison. This is why, while only biased with 50 nA, the comparators respond in less than 10 ns, as is shown in Figure 6.12. Figure 6.13 shows a zoomed out view of how the
output current $i_{RECT}$ flows into $V_{RECT}$ for charging and out of $V_{RECT}$ for investment over an entire prediction phase.

![Figure 6.12. Measured output current $i_{RECT}$ and positive switching voltage $v_{SW}^+$ during $\tau_{RECT}$ time.](image)

It is also worth mentioning that this power stage utilizes a resonant flip technique when the energy in $L_R$ is insufficient to charge the switching node up to $V_{RECT}$ during the
beginning of a \( \tau_{RECT} \) time, as shown in Figure 6.14. This situation of deficient energy in \( L_R \) occurs when the calibration has just completed and power transfer has just begun, which corresponds to \( t = 0 \) in Figure 6.14. If \( V_{EMF,R} \) is small then the energy drawn during the first \( \tau_{EN}^+ \) is also small and in Figure 6.14 it is insufficient to charge \( v_{SW}^+ \) up to \( V_{RECT} \) during the \( \tau_{RECT}^+ \) time. As such, the energy transfers from \( L_R \) to \( C_{PAR} \) and then back to \( L_R \) for half of a resonant cycle before \( CP_{ZVS,N}^+ \) detects that \( v_{SW}^+ \) goes below ground. During that half-resonant time the inductor current flipped direction in a quasi-lossless fashion before starting the negative energizing time \( \tau_{EN}^- \). During this energizing time, \( L_R \) received an investment with which it now has sufficient energy to charge the switching node (i.e., \( v_{SW}^- \)) up to \( V_{RECT} \), as shown in Figure 6.14. Once this energy threshold is overcome, \( V_{RECT} \) will supply the required investment for all of the subsequent half-cycles until the next prediction phase when this process repeats.

![Figure 6.14. Measured waveforms of resonant flip when \( V_{EMF,R} \) is too small to boost \( v_{SW}^+ \) up to \( V_{RECT} \).](image-url)
6.4.2 PTAT-current Generator

The 50 nA proportional to absolute temperature (PTAT) current generator, shown in Figure 6.15, biases the ZVS comparators, sense comparator \( CP_{SEN} \), and the \( \tau_{RECT} \) timer cell. Here, the n-type current mirror \( M_{MIR1} - M_{MIR2} \) forces the drain currents of \( M_{PTAT1} \) and \( M_{PTAT2} \) to be equal, but as \( M_{PTAT2} \) is sized eight times larger its source-to-gate voltage \( v_{SG2} \) is smaller than \( M_{PTAT1} \)'s source-to-gate voltage \( v_{SG1} \). Furthermore, as these MOSFETs operate in the subthreshold regime, the difference of their source-to-gate voltages generates a PTAT voltage \( V_{PTAT} \), which when impressed on resistor \( R_{PTAT} \) generates the following PTAT current

\[
I_{PTAT} = \frac{V_{SG1} - V_{SG2}}{R_{PTAT}} = \frac{V_{PTAT}}{R_{PTAT}} = \frac{U_T \ln(8)}{\kappa R_{PTAT}},
\]

(6.23)

where \( U_T \) is the thermal voltage and \( \kappa \) is the capacitive divider between the gate oxide and depletion capacitance [56]. Finally, the start-up circuit ensures that the circuit is in its stable non-zero state by comparing if the bias current (via \( M_{NST1} \)) is larger than what the diode-connected \( M_{PST2} \) and \( M_{PST1} \) transistors source.

![Figure 6.15. PTAT-current generator (transistor dimensions are in μm).](image-url)
6.4.3 EMF Sense Comparator

The EMF sense comparator, \(CP_{SEN}\) in Figure 6.5, detects \(v_{EMF,R}\) zero crossings during the calibration phase as a means of recording the operational period \(T_O\). In-between calibrations, however, \(CP_{SEN}\), as shown in Figure 6.16, disables with \(S_{CAL}\) and \(S_{SEN}\) set LOW in an effort to conserve power. When the calibration phase begins, with \(S_{CAL}\) set HIGH but \(S_{SEN}\) still LOW, the fast startup circuit produces a \(v_{BIAS}\) voltage that increases the currents mirrored by 10× for a faster comparison. Moreover, switches \(M_{BURN1}\) and \(M_{BURN2}\) engage and impress \(R_{SENSE}\) across \(v_{SW}^+\) and \(v_{SW}^-\), but as \(S_{SEN}\) is still LOW switches \(M_{EN1}\) and \(M_{EN2}\) isolate \(CP_{SEN}\) from the incoming signal. Prior to setting \(S_{SEN}\) HIGH, a ring suppression time ensures that any remnant energy in the parasitic capacitance of the switching nodes (i.e., \(v_{SW}^+\) and \(v_{SW}^-\)) and any remnant energy in \(L_R\) dissipates into \(R_{SEN}\). Moreover, the value of \(R_{SEN}\) is set to critically damp the second-order system that \(L_R\) and the parasitic capacitance make; which is to say that \(R_{SEN}\) dissipates the remnant energy as fast as possible so that \(v_{SW}^+\) begins tracking \(v_{EMF,R}\) as soon as possible.

When \(S_{SEN}\) does go HIGH, after all ringing is suppressed and \(v_{SW}^+\) approximately follows \(v_{EMF,R}\), an input capacitance \(C_{FILT}\) aids in filtering out high frequency noise on the switching nodes. After which, gate-coupled pair \(M_{GC1}\) and \(M_{GC2}\) convert the difference in switching voltages into a differential current that ultimately flows through \(R_{DIFF1}\) and \(R_{DIFF2}\) to generate differential voltage gain across \(v_G^+\) and \(v_G^-\) equal to

\[
A_{IN,DIFF} = \frac{\Delta v_G}{\Delta v_{SW}} = g_{m,GC}R_{DIFF} = \frac{kRT}{U_T} R_{DIFF} = \ln(8) \frac{R_{DIFF}}{R_{PTAT}},
\]

where \(g_{m,GC}\) is the transconductance of the input pair, which operates in subthreshold. Notice, that the gain is temperature independent and that when the resistors are of the same type, as they are here, \(A_{IN,DIFF}\) only varies with resistor matching. \(M_{CM1}\) and \(M_{CM2}\) aid in biasing the following stage while suppressing the common-mode gain of the input stage. Then, the voltage \(\Delta v_G\) drives the differential pair \(M_{DIFF1}\) and \(M_{DIFF2}\) with current latch load. The outcome of the latch determines whether to push or pull current from the
Figure 6.16. EMF sense comparator (transistor dimensions are in μm).
v_{DEC} node and complete the comparison. Asymmetric hysteresis via \( M_{HYST} \) aids in noise suppression and allows for zero volt comparison when determining a negative to positive \( v_{EMF, R} \) transition.

### 6.4.4 Low Power Oscillator

Figure 6.17 displays the source-coupled relaxation oscillator that generates the clock frequency for the system, i.e., \( f_{CLK} \). The oscillator receives its current bias from a dedicated \( V_{SGP} \) bias generator, which drops \( M_{REF} \)’s \( V_{SGP} \) voltage over \( R_{BIAS} \) to set the current bias \( I_{SGP} \) that equals

\[
I_{SGP} = \frac{V_{SGP}}{R_{BIAS}}.
\]  

(6.25)

Note, that the n-type cascodes \( M_{CASX} \) used in the \( M_{CASX}-M_{CURX} \) current mirrors of the bias generator and throughout the oscillator, operate in subthreshold, while the bottom devices \( M_{CURX} \), operate in above-threshold. This allows bottom devices \( M_{CURX} \) to remain in the saturation region even though both \( M_{CASX} \) and \( M_{CURX} \) share the same gate voltage.

The oscillator operates by either charging or discharging \( C_{OSC} \) with the bias current \( I_{SGP} \) and determines charging direction by the state of cross-coupled latch \( M_{CC1} \) and \( M_{CC2} \). If, for example, \( M_{CC1} \) is on and \( M_{CC2} \) is off, then \( i_{LATCH}^+ \) equals \( 2I_{SGP} \) and \( v_{LATCH}^+ \) falls to sink that current and reinforce the state, while \( i_{LATCH}^- \) is zero and \( v_{LATCH}^- \) remains at \( V_{RECT} \). Furthermore, when in this state, a current of value \( I_{SGP} \) flows through \( C_{OSC} \) to charge it until \( v_{OSC} \) grows to the point that the cross-coupled latch changes state. This state change occurs when \( v_{OSC} \) equals the \( V_{SGP} \) voltage of latch transistor \( M_{LI} \) when conducting \( I_{SGP} \). In this new state, \( M_{CC2} \) is on and \( M_{CC1} \) is off so that this time \( C_{OSC} \) is discharged by a current of value \( I_{SGP} \). This continues until \( v_{OSC} \) equals \( -V_{SGP} \) at which point the oscillator returns to the original state (i.e., \( M_{CC1} \) on and \( M_{CC2} \) off). As such, \( v_{OSC} \) changes by twice the \( v_{SGP} \) voltage before changing state, or
Figure 6.17. Generation of clock frequency $f_{CLK}$ via source-coupled relaxation oscillator and corresponding bias generator (transistor dimensions are in $\mu$m).
\[ \Delta V_{OSC} = 2V_{SGP} = \frac{I_{SGP}}{C_{OSC}} \left( \frac{T_{CLK}}{2} \right), \]  

which has a discharging time of \( T_{CLK}/2 \) because half the time is spent charging and the other half discharging. Then, expressing in terms of \( f_{CLK} \) yields

\[ f_{CLK} = \frac{I_{SGP}}{4C_{OSC}V_{GSP}} = \frac{1}{4C_{OSC}R_{BIAS}}. \]  

Finally, a push-pull output stage compares the state of the latch and feeds that comparative result to a cascade of high-\( V_{TH} \) inverters. These high-\( V_{TH} \) inverters sharpen the clock edges while reducing shoot-through losses.

### 6.4.5 Timer

The timer, as shown in Figure 6.18a, generates the \( \tau_{RECT} \) time by comparing how long it takes to charge capacitor \( C_{RAMP} \) with an adjustable current reference \( I_{CHG} \) to a voltage \( v_{RAMP} \) that exceeds an external reference voltage \( V_{REF} \) of 0.8 V. The comparator \( CP_{TMR} \), determines when \( v_{RAMP} \) is larger than \( v_{REF} \), at which point the SR latch resets and \( M_{DIS} \) discharges \( C_{RAMP} \) in preparation for the next \( \tau_{RECT} \) time. Furthermore, when reset, \( M_{PASS} \) opens to drive \( I_{CHG} \) to zero and conserve power. When enabled (set is HIGH), an external current reference \( I_{EXT} \) of value 30 nA – 1 \( \mu \)A generates the \( I_{CHG} \) current via the \( \times16 \) current mirror \( M_{MIR}\cdot M_{CH} \) to offer a \( \tau_{RECT} \) range of 70 ns – 1.8 \( \mu \)s as the expression for the \( \tau_{RECT} \)

\[ \tau_{RECT} = \frac{C_{RAMP}V_{REF}}{16I_{EXT}} \]  

predicts. Lastly, comparator \( CP_{TMR} \), shown in Figure 6.18b, uses a source cross-coupled input pair to eliminate slew-rate conditions when \( v_{RAMP} \) exceeds \( V_{REF} \) for a faster comparison.
Figure 6.18. \( t_{\text{RECT}} \) generation using (a) timer circuit with its corresponding (b) comparator \( CP_{\text{TMR}} \) (transistor dimensions are in \( \mu \text{m} \)).

### 6.5 Experimental Results

The 180-nm 510 × 510-\( \mu \text{m}^2 \) die in Figure 6.19 incorporates the power receiver proposed in Figure 6.3, except for the 2.6 × 3.5 × 11.7 mm\(^3\) 400-\( \mu \text{H} \) Coilcraft 4513TC receiver coil \( L_R \), the 300-nF SMD ceramic holding capacitor \( C_{\text{RECT}} \), and timer current \( I_{\text{EXT}} \) and voltage \( V_{\text{EXT}} \) reference generators; the reference generators are off chip to add flexibility when testing the system. \( L_R \) exhibits an ESR (i.e., \( R_R \)) of 9.66 \( \Omega \) with a quality factor of 29 at 125 kHz, which is the system’s operating frequency. The test stand incorporates a 443-4 Newport linear stage with a 1-\( \mu \text{m} \) sensitive micrometer, shown in Figure 6.19, to simultaneously vary transmission distance \( d_C \) and peak induced coil voltage \( V_{\text{EMF.R}} \).
6.5.1 Receiver Power Efficiency

Figure 6.20 displays how output power $P_{RECT}$, losses $P_{LOSS}$, and receiver efficiency $\eta_R$:

$$\eta_R = \frac{P_{RECT}}{P_{EMF.R(ERR)}} = \frac{P_{EMF.R(ERR)} - P_{LOSS}}{P_{EMF.R(ERR)}} = \frac{P_{EMF.R(IDEAL)} - P_{LOSS}}{P_{EMF.R(IDEAL)} - P_{LOSS}}$$

(6.29)

vary across transmission distance $d_C$ and coil voltage $v_{EMF.R}$. For distant power transmission ($d_C > 40\text{mm}$), output power is low, because there is little available power for such small coil voltages at these distances and because the fixed power losses: quiescent $P_Q$, switching $P_{SW}$, digital $P_{DIG}$, and oscillator $P_{OSC}$ that total $7.8\mu W$ become overwhelming, as Figure 6.21 shows. For near power transmission ($d_C \leq 30\text{mm}$), $\eta_R$ is relatively high (ranges from 67–84%) because power drawn from the $v_{EMF.R}$ source increases with larger coil voltages and because even the most dominant losses, conduction from coil ESR $P_{C(RS)}$ and MOS switches/diode $P_{C(MOS)}$, are diminutive (the system operates under an investment-limited regime).

Figure 6.20. Measured output power, system losses, and conversion efficiency across transmission distance and induced coil voltage.
6.5.2 Optimal Predictions

Figure 6.22 displays how output power $P_{RECT}$ varies over the number of predicted operational periods $N_{PER}$ with two different clock frequencies $f_{CLK}$ and two different transmission distances $d_C$. In all cases, increasing $N_{PER}$, at least initially, increases output power. This is the case because no power transfer takes place during calibration, so that increasing the prediction phase (i.e., increased $N_{PER}$) decreases the fraction of time without power transfer. However, as $N_{PER}$ increases further, the output powers peak (with the exception of $f_{CLK} = 14$ MHz traces, because of the limited programmable range of $N_{PER}$), which results from increasingly inaccurate predictions with higher $N_{PER}$. Furthermore, notice that for near transmission, i.e., high $V_{EMF,R}$ source power, a faster $f_{CLK}$ can predict more operational periods with less penalty than a slower $f_{CLK}$. This is because a faster $f_{CLK}$ or a shorter clock period $T_{CLK}$ truncates the maximum quantization or time error. Still, increasing $f_{CLK}$ raises the digital and oscillator losses ($P_{DIG}$ and $P_{OSC}$) of the system from 6.2 $\mu$W for a $f_{CLK}$ of 9.2 MHz to 9.9 $\mu$W for an $f_{CLK}$ of 14 MHz, which is to say that for distant transmission or low $V_{EMF,R}$ source power a slower $f_{CLK}$ that does not overwhelm the system with losses is preferred. Figure 6.23 corroborates this by displaying how the maximum transmission distance $d_{C(MAX)}$ peaks at 7 cm when $f_{CLK}$
equals 5.25 MHz. Furthermore, Figure 6.24 displays how using a larger pickup coil, of size $4.7 \times 6.9 \times 28\text{-mm}^3$, can increase the maximum transmission distance to 13 cm and decrease the minimum EMF voltage to $42 \text{ mV}_{PK}$.

![Figure 6.22. Measured output power across the number of $v_{EMF,R}$ periods between recalibrations at several clock frequencies.](image)

![Figure 6.23. Measured EMF threshold voltage $v_{EMF,R(MIN)}$ and maximum transmission distance $d_{C(MAX)}$ of the proposed receiver across clock frequency.](image)

![Figure 6.24. Measured EMF threshold voltage $v_{EMF,R(MIN)}$ and maximum transmission distance $d_{C(MAX)}$ of the proposed receiver across clock frequency for a large and small pickup coil.](image)
6.5.3 Charging Performance

The time-domain charging profiles in Figure 6.25 demonstrate how the prototyped system charged $C_{RECT}$’s 300 nF at 125 kHz when driven at transmission distances of 1, 2, 3, 4, and 5 cm. Since $C_{RECT}$ receives packets of energy every half-cycle, $C_{RECT}$’s $V_{RECT}$ rises in staircase fashion every 4 μs, much like a pulse-charged system does. Here, closer transmission distances raise $V_{RECT}$’s rising stair-step rate because $C_{RECT}$ charges more quickly with higher $P_{EMF,R}$. Furthermore, notice that the stair steps are not perfectly flat, which results because the system consumes power. Finally, the system calibrates every 13 steps, during which no power transfers to $C_{RECT}$ so that $V_{RECT}$’s staircase waveform appears to be missing steps during the calibration phase.

![Charging Profiles](image)

**Figure 6.25.** Measured time-domain charging profiles for a 300-nF SMD ceramic capacitor at 125 kHz.
6.5.4 Frequency Response

Varying the operational frequency $f_o$ by ±20% across 50 kHz about the 125-kHz nominal point only changed the minimum $v_{EMF,R(MIN)}$ voltage by 14.8 mV, as Figure 6.26 shows. This deviation is small because the synchronizer calibrates itself to the new operational frequency. This adaptability is not present in resonant receivers and a ±20% mismatch between operating and resonating frequency results in variation of $v_{EMF,R(MIN)}$ as large as 529 mV (from Figure 4.17b). Moreover, most resonant receivers operate in the MHz range to reduce the value and size of $C_R$ to an integratable scale. However, these higher frequencies increase switching losses and require faster control circuits that consume more energy. By removing $C_R$, the proposed receiver can operate at a slower operating frequency without suffering the penalty of either higher losses or a larger PCB footprint.

![Figure 6.26. Measured EMF threshold voltage of the proposed receiver across operation frequency.](image)

6.5.5 Startup and low-$V_{EMF,R}$ Flag

Unlike steady-state operation, where to some extent $v_{EMF,R}$’s phase is known (bounded by $\Delta \theta$) and an accurate measurement of $v_{EMF,R}$’s period may be recorded during calibration, in startup $v_{EMF,R}$’s phase is completely random. To avoid an erroneous measurement of $v_{EMR}$’s period during the startup calibration, comparator $CP_{SEN}$ counts through three $v_{EMF,R}$ periods before the recorded measurement occurs, which is why the initial calibration time lasts about four times longer than normal, as shown in Figure 6.27. Additionally, as $CP_{SEN}$ has hysteresis of about 16 mV, if the incoming amplitude of
\( v_{EMF,R} \) is smaller than \( CP_{SEN} \)'s hysteresis, then \( CP_{SEN} \) will not trip and the converter remains in the calibration phase, which avoids operating at a loss because power cannot be drawn from such a low \( V_{EMF,R} \) voltage anyway. Furthermore, when in this low-\( V_{EMF,R} \) state, the prediction counter \( CNT_{PRED} \) still counts, as it expects the comparator to eventually trip. To signal that \( v_{EMF,R} \) it too low (i.e., \( CP_{SEN} \) never trips to reset \( CNT_{PRED} \)), an overflow bit latches high when the counter \( CNT_{PRED} \) overflows to flag the low-\( V_{EMF,R} \) event.

![Waveform Diagram](image)

**Figure 6.27.** Measured time-domain waveforms during startup.

## 6.6 Summary

The previously proposed inductive rectifiers of Chapter 4 and 5 required auxiliary information from the transmitter to perform synchronization. As transmitter information is rarely accessible, this chapter described a self-synchronizing technique that only relies on information derived from the pickup coil. Synchronization information on the pickup coil is encoded in \( v_{EMF,R} \)'s phase and frequency, yet as the coil’s self-inductance \( L_R \)
appears in series with $v_{EMF,R}$, the $v_{EMF,R}$ voltage is normally inaccessible. To measure $v_{EMF,R}$, the coil is open-circuited to null out $L_R$’s voltage drop and make the $v_{EMF,R}$ voltage appear over the pickup coil. The pickup coil is open-circuited during the calibration phase, where $v_{EMF,R}$ period is recorded into an equivalent number of clock cycles. Then during the prediction phase, $v_{EMF,R}$’s recorded period is used to predict future switching events, such that coil current and voltage (i.e., $i_L$ and $v_{EMF,R}$) remain in phase and synchronized. However, due to the quantization error associated with attempting to record an analog value of time (i.e., $T_o$) into an integer number of clock periods, each successive prediction using the same erroneously sampled operational period results in compounding error such that $i_L$ and $v_{EMF,R}$ diverge from one another with each prediction. As such, the system must recalibrate after some $N_{PER}$ number of operational periods. A higher frequency clock helps truncate this quantization error, such that a higher $N_{PER}$ number of predictions can be made, but generation of a higher frequency clock also requires additional power, such that there is a tradeoff in clock frequency. An integrated prototype verified this self-synchronization scheme, which yielded 38% – 84% power-conversion efficiencies across 1.0 – 5.0 cm. Additionally, the CMOS power receiver generated net power from as little as 46.6 mVPK of $V_{EMF,R}$ across a separation of up to 7.0 cm and received a maximum output power of 557 μW.
CHAPTER 7

CONCLUSIONS

Continued advances in microfabrication have enabled the miniaturization of microelectronic and microelectromechanical (MEMS) systems to form ultra-compact microsystems, such as wireless micro-sensors and biomedical implants. The advanced functional requirements of such systems are taxing to the power budget, which reduces operational lifetime of the system as the miniaturized on-board energy sources have reduced energy capacity. Harvesting energy from the environment is therefore appealing, but not yet a reality for many applications, because miniaturized state-of-the-art transducers do not yet generate sufficient power from the ambient environment (typically limited to single-digit-microwatt power levels). Therefore, wirelessly transferring power to a microsystem from a dedicated source via inductive coupling can supply the additional power required to extend the operational lifetimes of these microsystems. Inductively coupled power transfer can also recharge the battery of a microsystem, so that the microsystem can continue to operate in-between interrogations (i.e., recharge cycles).

7.1 Miniaturized Inductively Coupled Power Receivers

Wireless power transfer via inductive coupling utilizes the magnetic field generated by a distant transmitter coil, \( \vec{B}_{\text{EXT}} \) shown in Figure 7.1, to induce an electromotive force (EMF) onto the receiver pickup coil from which a receiver draws power. The magnitude of the voltage induced, \( v_{\text{EMF,R}} \), is proportional to the magnetic flux in the receiver coil, i.e., \( \Phi_{\text{FLUX}} \), which in turn is proportional to the area that bounds the coil, \( A_{\text{ENC}} \). Miniaturized receiver coils, like those found in wireless microsystems, have small \( A_{\text{ENC}} \) and low magnetic flux, which ultimately results in low \( v_{\text{EMF,R}} \) voltages induced onto the receiver coil. This low voltage generates two technical challenges: (i) low voltage rectification and (ii) increasing received power.
The most common wireless receiver architecture in the literature is the \textit{LC}-boosted or resonant receiver shown in Figure 7.2a. This receiver resolves the challenge of low voltage rectification by introducing capacitor $C_R$ to implement a $L_R$-$C_R$ resonant tank that is tuned to the incoming $v_{\text{EMF}, R}$ signal. The filter is selected to have a high quality factor to boost the peak capacitor voltage, $v_C$, to rectifiable levels. Matching the resonant frequency to the incoming $v_{\text{EMF}, R}$ frequency is critical for operation as high-$Q$ filters have low bandwidth (i.e., $\Delta\omega_{3\text{dB}}=\omega_0/Q$).

Increasing the power transferred to the receiver amounts to conditioning the coil current, $i_L$, because the power sourced by $v_{\text{EMF}, R}$ is the product of $v_{\text{EMF}, R}$ and $i_L$. As the
magnitudes of $v_{\text{EMF}}$R is small, the magnitude of the coil current needs to be large. Furthermore, the two signals, i.e., $v_{\text{EMF}}$R and $i_L$, should be in-phase with one another, because the out-of-phase components draw no average power from $v_{\text{EMF}}$R (often referred to as reactive power). Figure 7.2b illustrates how the resonant receiver conditions the coil current for higher power extraction. Firstly, notice that the capacitor voltage $v_C$ that drives the pickup coil is lagging from $i_L$ and $v_{\text{EMF}}$R by about 90°. This lagging $v_C$ is what drives the coil current to be in-phase with $v_{\text{EMF}}$R, because $L_R$ induces a current that leads the voltage impressed over it by 90°. This phase cancelation is often referred to as the conjugate matching condition. Secondly, notice that energy transfers from $C_R$ to $L_R$ every quarter cycle, as the energy in $C_R$ and $L_R$ is $\frac{1}{2}C_Rv_C^2$ and $\frac{1}{2}L_Ri_L^2$, respectively. This energy transfer or investment from $C_R$ to $L_R$ is necessary for the generation of the large coil currents needed for higher power transfer, because in order to support the large instantaneous energy in $L_R$, which equals $\frac{1}{2}L_Ri_L^2$, energy needed to be invested from $C_R$.

7.2 Research Objective

The purpose of this research is to investigate how to transfer power wirelessly using a loosely-coupled inductive link and to develop, design, simulate, build, test, and evaluate a CMOS charger integrated circuit (IC) that wirelessly charges the battery of a microsystem. A fundamental challenge here is that miniaturized receiver coils only produce millivolts of AC voltage, which is difficult to convert into DC form. Although LC-boosted diode-bridge rectifiers in the literature today extract energy from similar AC sources, they can do so only when AC voltages are higher than what miniaturized coils can produce, unless tuned off-chip capacitors are available, which counters the aim of integration. Therefore, rather than rectify the AC voltage, this research rectified the current that the AC voltage induces in the coil. This way, the system can still draw power from voltages that fall below the inherent threshold limit of diode-bridge rectifiers. Still, output power was low because, with these low currents, small coils can only extract a
diminutive fraction of the magnetic energy available, which is why investing battery energy into the coil to build larger coil currents generated higher output power.

7.3 Research Contributions

7.3.1 Main Contribution

The main contribution of this research is a novel miniaturized inductively coupled power receiver that accomplishes the low EMF voltage rectification required for power delivery to a wireless microsystem. The proposed energy-investment receiver, shown in Figure 7.3a, uses a switching network to impose a pickup coil voltage $v_{PC}$, which emulates that of the resonant receiver’s capacitor voltage, $v_C$ in Figure 7.2b. To see how, first consider that the switching network allows for three voltage levels of $v_{PC}$: $V_{RECT}$, zero, and $-V_{RECT}$. Furthermore, consider that when orchestrating the switching network appropriately, $v_{PC}$’s fundamental component, as seen in Figure 7.3b, follows that of the resonant capacitor’s voltage in Figure 7.2b. Appropriate capacitor voltage emulation is achieved by requiring that $v_{PC}$’s fundamental component lag behind $v_{EMF,R}$ by 90°. As such, the switching network emulates quasi-resonance conditioning onto the pickup coil without having to physically realize a capacitor.

Adjusting the duration of $\tau_{RECT}^+$ and $\tau_{RECT}^-$ varies the amplitude of $v_{PC}$’s fundamental component. This flexibility allows the amplitude of the fundamental component of $v_{PC}$ to be 27% larger than that of the resonant converter when the total $\tau_{RECT}$ time (i.e, $\tau_{RECT}^+ + \tau_{RECT}^-$) extends across the entire period. This is because the fundamental component of a square wave is 27% larger than that of a sinusoidal wave for the same peak-to-peak value. This increase in the fundamental component of $v_{PC}$ translates into the capacity to extract more power than the resonant receiver (27% more power extraction capability). Moreover, an adjustable fundamental component of $v_{PC}$ offers the potential to run the system at different operating points, namely, high
efficiency, maximal power, or some combination in-between. Adjustable loading is also important for adaptive selection of the optimal \( \tau_{RECT} \) in applications where coil separation and orientation vary the coupling factor.

![Diagram of proposed energy-investment inductive rectifier with corresponding time-domain waveforms for EMF voltage \( (v_{EMF,R}) \), coil current \( (i_L) \), and pickup coil voltage \( (v_{PC} = v_{SW}^+ - v_{SW}^-) \).]

As mentioned previously, increasing power transfer to the receiver amounts to increasing the magnitude of the coil current, as the power sourced from \( v_{EMF,R} \) is the product of their in-phase components. Generating larger coil currents requires that energy be temporarily supplied into \( L_R \). Intuitively, this results because the coil’s self-inductance (i.e., \( L_R \)) has a magnetic energy of \( \frac{1}{2}L_R i_L^2 \) that requires supplementary energy in the form of an investment during the peaks and troughs of \( i_L \). As such, the switch network facilitates bi-directional power flow, from which \( V_{RECT} \) can supply the energy investment necessary for generation of higher coil currents, which results in higher power transfer.

This novel inductive rectification scheme circumvents the threshold limitations of conventional voltage-mode rectifiers by current-mode rectification, which is to say that there is no fundamental voltage with which \( v_{EMF,R} \) must overcome. Instead, the threshold that results is a power threshold, in which the incoming power sourced by \( v_{EMF,R} \) must be greater than the power losses associated with the converter. By utilizing a slower switching frequency (equal to the incoming \( v_{EMF,R} \) frequency), frequency-related power losses like gate-drive, \( I-V \) overlap, and controller losses (as faster-responding circuits
require more power) are reduced. The combination of increased power extraction and decreased losses reduces the input-referred threshold to unprecedented values for inductive rectifiers.

The removal of the resonant capacitor aids in miniaturizing the inductively coupled power receiver solution, which is crucial in wireless microsystem applications. Furthermore, the proposed receiver uses the pickup coil’s self-inductance as the power transfer element, such that the pickup coil is the only off-chip component required for power transfer (other than the output energy storage i.e., battery or capacitor), which ultimately aids in micro-scale system integration. Unlike the resonant receiver, which requires the $L_R-C_R$ resonant tank to be tuned to the incoming $v_{EMF,R}$ frequency, this proposed energy-investment receiver self-synchronizes to the $v_{EMF,R}$ frequency to minimize frequency sensitivity. Adjusting the switching frequency to track the $v_{EMF,R}$ frequency can be thought of intuitively as tuning the emulated capacitor value to ensure continued quasi-resonance. A novel self-synchronization scheme is introduced in Chapter 6, which measures and records $v_{EMF,R}$’s operational period to forecast future $v_{EMF,R}$-waveform information. Using these predictions, the receiver can synchronize its switching events with $v_{EMF,R}$ to reduce frequency sensitivity.

### 7.3.2 Other Contributions

The requirement of a low power loss design as a means to reduce the input-referred threshold and increase system efficiency generated additional contributions from the development of low power loss design strategies. In particular, system-level strategies include: switching all of the power MOSFETs with zero volt switching (ZVS), using active diodes (sometimes referred to as diode-emulation switches) instead of conventional p-n or Schottky diodes, inductively driving switching nodes, disabling circuit blocks to save quiescent power when not in use, balancing quantization error power losses with clock-related power losses, and optimal power switch sizing. Circuit-
level strategies include: subthreshold-operated circuits, fast start-up circuits to quickly enable blocks from deep sleep, clock-gating and a specialized minimum-latch architecture to reduce digital gate driving losses, and a low-power source-coupled relaxation oscillator to reduce clock related power losses.

7.3.3 Publications

Thus far, this research has generated three journal publications, with a fourth under review, along with a conference publication. The JSSC publication details the advantages of the inductive rectifying scheme compared to that of the resonant receiver, describes the fabricated prototype of Chapter 4 and displays, as well as discusses, experimental results. The two TCAS-II publications detail the benefits of investment as a means to boost power extraction from low EMF voltages and the August 2013 journal details experimental results. Additionally, a JESTPE manuscript has been submitted and is currently being reviewed. The JESTPE manuscript details the self-calibration scheme of Chapter 6 along with system and circuit level implementation of the scheme and additionally displays, as well as discusses, validating experimental results. Finally, the ISOCC conference publication discusses appropriate sizing of CMOS switches (i.e., balancing gate-driving and conduction losses) for the proposed inductive rectifier scheme of Chapter 4.

Peer-Reviewed Journals


**Peer-Reviewed Conference-Publication**


### 7.4 Technological Limitations and Future Research Direction

For all of the benefits of the proposed inductive-rectifier wireless power receiver, the technology has technical limitations. First, the system cannot startup if the battery (i.e., $V_{RECT}$) is depleted of energy. Secondly, determination of the optimal investment energy is currently being implemented in an open loop fashion. Thirdly, although functional as a charger, the receiver cannot directly regulate the supply for a wireless microsystem load, which is important in applications that do not have an on-board battery. Another limitation is the lack of support for near field communication (NFC), which is the preferred communication method if an inductive link is available. Lastly, the current operational frequency of the system can only support the lowest radio frequency
identification (RFID) communication band. These technological limitations motivate future research and are briefly discussed in the following subsections.

7.4.1 Zero-energy Startup

Inductive rectifiers, which include the receivers proposed in this research, require initial charge on the output capacitor $C_{RECT}$ to startup. Without this supply voltage, control circuitry is incapable of orchestrating power transfer, and possibly more importantly, power MOSFETs cannot be switched on and off. This is a serious limitation when compared to the resonant receiver, which can startup with zero voltage on $C_{RECT}$. The significance of this is that if the receiver experiences a severe drought of incoming power and the wireless microsystem continues to expend the remnant energy on $C_{RECT}$ until it depletes, then when a transmitter attempts to replenish the receiver, the receiver is unable to harness that potential energy. Effectively, if the receiver ever runs out of energy on $C_{RECT}$ then the receiver remains nonfunctional indefinitely. Furthermore, if the frequency of recharging cycles from the transmitter to the receiver is irregular, then it is much more likely that the receiver will experience a prolonged power drought that makes it inoperable. As such, it is of interest to enhance the inductive rectifier family with some zero-energy startup capability.

It is worth mentioning that adding the passive components found in traditional methods of startup, such as using a resonant capacitor as is found in resonant receivers or using a transformer to step up the voltage, would counter the aim of integration and would negate all the benefits of the streamlined receivers proposed in this research. Second, the proposed receivers presented in this work implicitly have a network of body diodes that implement a diode-bridge to the output, as shown in Figure 7.4a. To reduce the turn-on voltage of this diode-bridge, Schottky diodes could be placed in parallel with power MOSFETs, as shown in Figure 7.4b. Even with this Schottky-diode implementation, however, $v_{EMF,R}$’s amplitude would still need to be on the order of one
volt before the $V_{RECT}$ voltage would be sufficiently high enough to start driving the power MOSFETs. As such, further research on low-voltage startup, such as [130], is still required to reduce the requirements on $v_{EMF,R}$ during zero-energy startup.

![Figure 7.4](image1.png)

**Figure 7.4.** Diode-bridge rectifier to be used as a startup circuit using (a) body diodes already present in MOSFET switches or (b) additionally added Schottky diodes placed in parallel to switches for reduced diode-bridge threshold voltage.

### 7.4.2 Optimal Energy Investment

The proposed wireless power receivers of Chapter 5 and Chapter 6 invest energy from the battery as a means of conditioning the pickup coil current to draw more power from the $v_{EMF,R}$ source voltage. Furthermore, and as was discussed in Chapter 5, investing too much energy into the pickup coil may result in either excessive conduction losses or transmitter overloading (dependent on coupling regime), both of which reduce the average power delivered to the battery. As not investing enough energy also results in reduced power delivery, there is an optimal energy investment which maximizes power delivery. Selecting the investment energy via $\tau_{RECT}$ modulation was implemented manually for both wireless power receivers in Chapter 5 and Chapter 6 (i.e., trim bit setting adjusted the diode-emulation comparator offset voltage in Chapter 5 and $I_{EXT}$ adjusted the $\tau_{RECT}$ timer block in Chapter 6). However, implementing a maximum power point tracking (MPPT) loop that automatically adjusts the $\tau_{RECT}$ time would allow the system to harness maximum power in an autonomous fashion, which is why it is of interest to explore implementations of MPPT for the proposed power receivers.
Figure 7.5 displays a simplified block level schematic of how a MPPT loop might be implemented [131]. This hypothetical system uses a power sensor to measure output power and a perturb and disturb block to monitor how changes in $\tau_{\text{RECT}}$ effect output power. This way, the perturb and disturb block can adjust $\tau_{\text{RECT}}$ in a fashion that increases output power until the system settles to the maximum power point. However, implementation of MPPT is not as straightforward as Figure 7.5 might suggest, especially in low-power applications where the tracking loop must not draw excessive quiescent power. For example, sensing output power, which amounts to measuring average current into the fixed $V_{\text{RECT}}$ voltage, requires fast current sensing because $i_{\text{RECT}}$ has a pulsed waveform that only flows during a brief $\tau_{\text{RECT}}$ time. Other sensing methods measure the change in $V_{\text{RECT}}$ to infer the charge and energy transferred to the output, but require additional sample and hold circuits [132]. Ultimately, future research on the subject is necessary for implementing a low-power MPPT, which might utilize some of the characteristics unique to this power receiver topology.

Figure 7.5. Simplified schematic of a maximum power point tracking implementation.

7.4.3 Load Regulation and Pickup Coil Reuse

This work focused on the development of a wireless power receiver that recharged the battery of a wireless microsystem. However, in applications with a dedicated transmitter,
like that of many biomedical implants [22, 133], the receiver experiences a continuous stream of energy, such that a battery is unnecessary and is often removed. In those applications, the receiver needs to regulate the voltage for the remainder of the microsystem. Currently, the proposed receivers of Chapter 5 and Chapter 6 do not regulate this voltage, but have the capacity to do so by adjusting the $\tau_{RECT}$ time as is shown in Figure 7.6. In this hypothetical system, an error amplifier compares a scaled version of the $V_{RECT}$ voltage with a reference voltage, $V_{REF}$, to generate the appropriate $\tau_{RECT}$ time required to satisfy the power requirement of the load, $Z_{LOAD}$. Finally, it is important to recognize that increasing $\tau_{RECT}$ will not generate sufficient power to satisfy the load if the load’s power requirement is higher than the maximum power point of the receiver.

![Figure 7.6. Simplified schematic of a load regulation implementation.](image)

Figure 7.6 displays a potential load regulation architecture, but wireless microsystems are typically complex multi-functional systems that require multiple voltage domains. For example, a microprocessor might require a 1 V supply rail that supports dynamic voltage scaling (DVS), while the transceiver’s RF power amplifier might require a 5 V supply rail to generate sufficient RF signal. Generation of these multiple voltage domains traditionally requires either the use of linear regulators, which

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are inefficient, or switch-mode regulators, which require off-chip components. The wireless receiver presented in this work, however, has the potential for reuse of the pickup coil as the magnetic transfer element found in a switch-mode regulator. Figure 7.7 displays the power stage of a single input multiple output (SIMO) implementation of the wireless power receiver. For an implementation like this, repeated packets of energy (delivered during their respective $\tau_{REC}$ times) might be sent to each load to maintain regulation. After which, any additional incoming energy may be used to recharge a battery, i.e., $V_{REC}$. Furthermore, the pickup coil may also be reutilized when there is no external magnetic field and for the case of Figure 7.7 the battery can buck or boost using the self-inductance of the pickup coil $L_R$ to transfer energy to the remaining loads. Still, ideas on load regulation and pickup coil reuse are premature and further research on the feasibility and performance of such architectures is required.

![Figure 7.7. Implementation of a single input multiple output power stage with a pickup coil reuse feature.](image)

### 7.4.4 Near-Field Communication

One of the benefits of using an inductively-coupled system to recharge the battery of a wireless microsystem, is that its inductive link may double as a communicative link, where the wireless microsystem may upload information to the transmitter using near field communication (NFC). This communication link is ideal for wireless microsystems, because NFC dissipates significantly less power than RF or radiative communication does. For NFC, information is conveyed to the transmitter using an on-off keying (OOK)
encoding scheme, where the receiver dramatically adjusts its input impedance (typically implemented by either shorting the pickup coil or not shorting it, i.e., power transfer) and the transmitter observes this change of impedance via backscattering (the back-EMF onto the transmitter coil changes dramatically). The proposed receivers of Chapter 5 and Chapter 6 do not comply with NFC, as the main focus of this work was power transfer. Still, compliance with NFC standards is necessary for the proposed receivers to be accepted as a viable alternative to the resonant receiver. Implementation of NFC for the proposed receivers of Chapter 5 and Chapter 6 is envisioned to be implemented in one of two ways. The first would allocate a time for which the pickup coil can be shorted, as is done with conventional resonant receivers, and then immediately follow with a calibration phase and then resume power transfer. The second would adjust the $\tau_{\text{RECT}}$ time as a means of modulating the loading seen by the transmitter, which would allow power transfer to continue uninterrupted. Ultimately, further research is necessary in assessing which implementation is better suited for optimal power transfer while still complying with NFC standards.

7.4.5 Operating Frequency

The novel power receivers presented in this work (Chapter 4 – 6) utilized an inductive-rectification scheme to circumvent the need for a resonant capacitor, which decoupled the relationship between operational frequency and capacitance. As such, the operational frequency for the novel power receivers could be chosen to be at much lower frequencies, i.e., 125 kHz, where frequency-related power losses (i.e., gate-drive and controller losses) could be much lower. The operational frequency of 125 kHz was selected because it is the lowest frequency that lies in the RFID communication band. Still, the RFID frequency spectrum is wide and many of the wireless power transmitters that could be viably used to recharge a wireless microsystem are at higher frequencies, e.g., 13.56 MHz. As such, further research on the subject of implementing low-power control
circuits that could respond to higher frequencies would allow the topology presented in this work to be extended to higher frequencies.

7.5 Summary

This research investigated how to effectively transfer power wirelessly using a loosely-coupled inductive link. Furthermore, this research developed, designed, simulated, built, tested, and evaluated a CMOS charger integrated circuit (IC) that wirelessly charged an energy-storage device that mimicked the battery of a microsystem. Specifically, a novel inductive-based rectifier was presented as the topology for the proposed wireless power receiver that could harness power from low EMF signals (~ 50 mV) without the requirement of a resonant capacitor. Moreover, investing energy from the battery to the pickup coil as a means of conditioning its current allowed for higher power extraction than that of even the resonant receiver. Finally, a novel synchronizing scheme allowed the wireless power receiver to operate autonomously by calibrating the switching frequency of the receiver to the incoming EMF signal. Using inductively-coupled power transfer to recharge the battery of a wireless microsystem can extend its lifetime semi-indefinitely (limited by battery cycle life), whereas using state-of-the-art energy sources (such as electrochemical batteries, supercapacitors, fuel cells, and nuclear batteries) to power the device is limited by its fixed energy storage.
The conditions for maximum power transfer across the inductively coupled system shown in Figure A.1 can be found by determining the function of load current $i_{\text{LOAD}}(t)$ that maximizes energy transfer. To begin with, the energy transferred to the load can be expressed as

$$E_{\text{LOAD}} = \int_{-\infty}^{\infty} v_{\text{LOAD}}(t) i_{\text{LOAD}}(t) dt,$$

where $v_{\text{LOAD}}(t)$ is the voltage impressed on the load. Because the system is linear, it is convenient to express Equation (A.1) in the frequency domain. This is done by using Parseval’s theorem to transform Equation A.1 to

$$\int_{-\infty}^{\infty} v_{\text{LOAD}}(t) i_{\text{LOAD}}(t) dt = \frac{1}{2\pi} \int_{-\infty}^{\infty} \text{Re}\left\{ \tilde{V}_{\text{load}}(\omega) \tilde{I}_{\text{load}}(\omega)^* \right\} d\omega,$$

where $\tilde{V}_{\text{load}}(\omega)$ and $\tilde{I}_{\text{load}}(\omega)$ are the Fourier transforms of $v_{\text{LOAD}}(t)$ and $i_{\text{LOAD}}(t)$, respectively. Moreover, the Fourier transform $\tilde{F}(\omega)$ of $f(t)$ is defined as

$$\tilde{F}(\omega) = \int_{-\infty}^{\infty} f(t) e^{-j\omega t} dt.$$

Figure A.1. Functional schematic of inductively-coupled power transfer.
As the inductively-coupled system is a linear time-invariant system, a network representation, as shown in Figure A.2, allows for direct determination of $V_{load}(\omega)$ using transfer functions. Here, $T_v(\omega)$ is defined as the transfer function from transmission voltage $V_t(\omega)$ to load voltage $V_{load}(\omega)$ with $I_{load}(\omega)$ nulled to zero, specifically,

$V_{load}(\omega)\bigg|_{I_{load}(\omega)=0} = T_v(\omega)V_t(\omega). \quad (A.4)$

Furthermore, $Z_o(\omega)$ is the output impedance and is defined as the transfer function from load current $I_{load}(\omega)$ to load voltage $V_{load}(\omega)$ with $V_t(\omega)$ nulled to zero, namely,

$V_{load}(\omega)\bigg|_{V_t(\omega)=0} = -Z_o(\omega)I_{load}(\omega). \quad (A.5)$

The load voltage can then be expressed as the superposition of the Equation (A.4) and Equation (A.5):

$V_{load}(\omega) = V_t(\omega)T_v(\omega) - Z_o(\omega)I_{load}(\omega). \quad (A.6)$

The newly formulated load voltage of Equation (A.6) can then be inserted to Equation (A.2) to generate

$E_{LOAD} = \frac{1}{2\pi} \int_{-\infty}^{\infty} \text{Re} \{ \left[ V_t(\omega)T_v(\omega) - Z_o(\omega)I_{load}(\omega) \right] I_{load}(\omega)^* \} d\omega, \quad (A.7)$

which reduces to
when rewriting into phasor representation; with \( \alpha(\omega) \), \( \beta(\omega) \), \( \phi(\omega) \), and \( \psi(\omega) \) corresponding to the phase components of \( \tilde{V}_{load}(\omega) \), \( \tilde{I}_{r}(\omega) \), \( \tilde{I}_{load}(\omega) \), and \( \tilde{Z}_{o}(\omega) \), respectfully. Simplifying Equation (A.8) further yields

\[
E_{LOAD} = \frac{1}{2\pi} \int_{-\infty}^{\infty} \text{Re} \left\{ \tilde{V}(\omega) \left| \tilde{I}_{r}(\omega) \right| e^{j[\alpha(\omega)+\beta(\omega)-\phi(\omega)]} - \tilde{Z}_{o}(\omega) e^{j[\psi(\omega)]} \left| \tilde{I}_{load}(\omega) \right|^2 \right\} d\omega, \quad (A.8)
\]

The condition for maximum power transfer amounts to determining the magnitude and phase of \( \tilde{I}_{load}(\omega) \) which maximizes Equation (A.9). This problem can be framed as a calculus of variations problem, with

\[
E_{LOAD} = \int_{-\infty}^{\infty} f \left( \left| \tilde{I}_{load}(\omega) \right|, \phi(\omega); \omega \right) d\omega \quad (A.10)
\]

being the integrand to be optimized. To maximize \( E_{LOAD} \), the following conditions must be set [134]:

\[
\frac{\partial f \left( \left| \tilde{I}_{load}(\omega) \right|, \phi(\omega); \omega \right)}{\partial \left| \tilde{I}_{load}(\omega) \right|} = 0 \quad (A.11)
\]

and

\[
\frac{\partial f \left( \left| \tilde{I}_{load}(\omega) \right|, \phi(\omega); \omega \right)}{\partial \phi(\omega)} = 0. \quad (A.12)
\]

Evaluating Equation (A.11) results in

\[
\frac{\partial f \left( \left| \tilde{I}_{load}(\omega) \right|, \phi(\omega); \omega \right)}{\partial \left| \tilde{I}_{load}(\omega) \right|} = \left| \tilde{V}(\omega) \left| \tilde{I}_{r}(\omega) \right| \cos[\alpha(\omega)+\beta(\omega)-\phi(\omega)] - 2\left| \tilde{Z}_{o}(\omega) \right| \left| \tilde{I}_{load}(\omega) \right| \cos[\psi(\omega)] \right| \quad (A.13)
\]
and setting it to zero yields the optimal magnitude of load current to be

\[ \left| \vec{I}_{\text{load}}(\omega) \right| = \frac{\left| \vec{V}_i(\omega) \right| \left| \vec{I}_{\text{source}}(\omega) \right| \cos[\alpha(\omega) + \beta(\omega) - \phi(\omega)]}{2 \left| Z_o(\omega) \right| \left| \vec{I}_{\text{load}}(\omega) \right| \cos[\psi(\omega)]}. \quad (A.14) \]

Evaluating Equation (A.12) results in

\[ \left. \frac{\partial}{\partial \phi(\omega)} \left[ \vec{I}_{\text{load}}(\omega), \phi(\omega) \right] \right|_{\phi(\omega) = 0} = \left( \frac{\vec{V}_i(\omega) \left| \vec{I}_{\text{source}}(\omega) \right| \sin[\alpha(\omega) + \beta(\omega) - \phi(\omega)]}{2 \left| Z_o(\omega) \right| \left| \vec{I}_{\text{load}}(\omega) \right|} \right). \quad (A.15) \]

and setting it to zero yields the optimal phase of load current to be

\[ \phi(\omega) = \alpha(\omega) + \beta(\omega) + n\pi, \quad n \in \mathbb{Z}, \quad (A.16) \]

where the maximum condition corresponds to \( n \) being even, which for simplicity, \( n \) equal to zero is selected as other even solutions are redundant. Finally, as reprise, the optimal \( \vec{I}_{\text{load}}(\omega) \) is

\[ \vec{I}_{\text{LOAD(MAX)}}(\omega) = \frac{\vec{V}_i(\omega) \vec{I}_{\text{source}}(\omega)}{2 \text{Re}\left\{ Z_o(\omega) \right\}}. \quad (A.17) \]

The requirements for maximal power transfer are quite general and can be used for other applications other than this inductively coupled system. To determine the exact requirements for this inductively coupled system expressions for \( \vec{V}_i(\omega) \) and \( Z_o(\omega) \) are required. From Figure A.1, \( \vec{V}_i(\omega) \) can be derived to be

\[ \vec{V}_i(\omega) = \frac{-\omega^2 C_T k_c \sqrt{L_T L_R}}{1 - \omega^2 L_T C_T + j\omega C_T R_T}, \quad (A.18) \]

and \( Z_o(\omega) \) can be derived to be

\[ Z_o(\omega) = \frac{j\omega^3 C_T k_c^2 L_T L_R}{1 - \omega^2 L_T C_T + j\omega C_T R_T} + j\omega L_T + R_L. \quad (A.19) \]
Then, for a single toned $V_{\text{load}}(\omega)$ with frequency content at $\omega_O^2 = 1/L_IC_T$, as in conventional inductively-coupled power transfer, transfer functions $\tilde{T}_v(\omega)$ and $\tilde{Z}_o(\omega)$ further simplify to

$$
\tilde{T}_v(\omega) \bigg|_{\omega=\omega_o} = j\omega_o \frac{k_c \sqrt{L_T L_R}}{R_T}, \tag{A.20}
$$

and

$$
\tilde{Z}_o(\omega) \bigg|_{\omega=\omega_o} = \frac{\omega_O^2 k_c^2 L_T L_R}{R_T} + j\omega_o L_T + R_R. \tag{A.21}
$$

Then inserting Equation (A.20) and Equation (A.21) into Equation (A.17) yields

$$
\frac{\tilde{I}_{\text{LOAD(MAX)}}(\omega)}{\tilde{V}_t(\omega)} \bigg|_{\omega=\omega_o} = \frac{j\omega_o k_c \sqrt{L_T L_R}}{R_T \left( \frac{\omega_O^2 k_c^2 L_T L_R}{R_T} + R_R \right)} = \frac{j\omega_o k_c \sqrt{L_T L_R}}{2R_R \left[ 1 + k_c^2 Q_T Q_R \right]}, \tag{A.22}
$$

where $Q_T = \omega_O L_T / R_T$ and $Q_R = \omega_O L_R / R_R$. Finally, for transmission voltage of $v_T(t) = V_T \sin(\omega_O t)$, as is taken throughout this text, translation of $\tilde{I}_{\text{LOAD(MAX)}}$ back to the time-domain using Equation (A.20) is simply a phase and magnitude translation of $v_T$ (because sinusoidals are the eigenfunctions of linear time-invariant systems). As such, the load current that maximizes power transfer $i_{\text{LOAD(MAX)}}(t)$ is

$$
i_{\text{LOAD(MAX)}}(t) = -\left. \frac{\omega_o k_c \sqrt{L_T L_R}}{2R_R \left[ 1 + k_c^2 Q_T Q_R \right]} \right| V_T \cos(\omega_o t). \tag{A.23}
$$
Figure B.1. displays the lumped impedance network of a receiver or transmitter coil, with \( Z_{COIL} \) constituting the collective impedance across its terminals. The quality factor of this network is defined as [96]:

\[
Q = \frac{\text{Im}\{Z_{COIL}\}}{\text{Re}\{Z_{COIL}\}},
\]

(B.1)

with \( Z_{COIL} \) equaling

\[
Z_{COIL} = (j\omega L + R) \parallel \frac{1}{j\omega C_{PAR}}.
\]

(B.2)

To proceed, Equation (B.2) will be simplified. Evaluation of the parallel operator yields

\[
Z_{COIL} = \frac{j\omega L + R}{1 + (j\omega L + R)j\omega C_{PAR}},
\]

(B.3)

which further simplifies to

\[
Z_{COIL} = \frac{j\omega L + R}{(1 - \omega^2 L C_{PAR}) + j\omega R C_{PAR}}.
\]

(B.4)

Multiplying numerator and denominator with the complex conjugate of the denominator yields the standard complex rectangular form:

\[
Z_{COIL} = \frac{R + j\omega \left[ L \left( 1 - \omega^2 L C_{PAR} \right) - R^2 C_{PAR} \right]}{\left( 1 - \omega^2 L C_{PAR} \right)^2 + (\omega R C_{PAR})^2}.
\]

(B.5)
It is constructive to rewrite the 2nd order system of Equation (B.5) into its natural frequency, which is often referred to as the self-resonant frequency $\omega_{SR}$, namely,

$$\omega_{SR} = \frac{1}{\sqrt{LC_{PAR}}}$$

(B.6)

and its damping ratio $\zeta$:

$$\zeta = \frac{R}{2} \sqrt{\frac{C_{PAR}}{L}}.$$  

(B.7)

Inserting these new expressions into Equation (B.5) yields

$$Z_{COIL} = \frac{R \left\{ 1 + j \frac{\omega}{R} \left[ 1 - (\omega/\omega_{SR})^2 - (2\zeta)^2 \right] \right\}}{\left[ 1 - (\omega/\omega_{SR})^2 \right]^2 + [2\zeta(\omega/\omega_{SR})]^2}.$$  

(B.8)

Then applying the quality factor definition results in

$$Q = \frac{\text{Im} \{Z_{COIL} \}}{\text{Re} \{Z_{COIL} \}} = \frac{\omega L}{R} \left[ 1 - (\omega/\omega_{SR})^2 - (2\zeta)^2 \right].$$  

(B.9)

Equation (B.9) is the complete expression for the quality factor of the lumped model in Figure B.1. Still, further simplifications can be made by noting that the coil is operated at much lower frequencies than its self-resonant frequency (i.e., $\omega \ll \omega_{SR}$) and the coil exhibits an extremely underdamped response (i.e., $2\zeta \ll 1$). Applying these approximations yields the quality factor expression that is used throughout the text, namely

$$Q \bigg|_{\omega \ll \omega_{SR}} = \frac{\omega L}{R},$$

(B.10)
APPENDIX C

**$P_{EMF,R}$ DERIVATION FOR THE RESONANT RECEIVER**

Figure C.1 depicts the resonant receiver with its corresponding high-$Q$ filter. The filter consist of an $L_R$-$C_R$ tank, which is assumed to be tuned to the driving frequency of the input $v_{EMF,R}$ voltage source, explicitly,

$$\omega_0 = \frac{1}{\sqrt{L_R C_R}}. \quad (C.1)$$

When $v_{EMF,R}$ drives the tuned $L_R$-$C_R$ tank, the capacitor voltage, $v_C$ resonantly builds until it surpasses the voltage threshold established by the voltage-mode rectifier, in this case $v_{C(PK)}$. During the clipping, the extra energy and current in $L_R$ deplete into $V_{RECT}$. Immediately afterwards, the stored energy on $C_R$ transfers back to $L_R$, forcing the current to flow in the opposite direction while discharging $C_R$. The resonant cycle continues until $v_C$ flips polarity, during which, $v_{EMF,R}$ supplies additional energy into the $L_R$-$C_R$ tank, so that after a half-resonant cycle, energy drawn from $v_{EMF,R}$ manifests itself as the additional current in $L_R$ that transfers into $V_{RECT}$ when $v_C$ clips.

![Figure C.1](image)

**Figure C.1.** Resonant receiver (a) circuit with (b) corresponding time-domain waveforms.

To simplify the problem, instead of having bursts of energy transfer to the battery when $v_C$ clips, the rectifier may be replaced with an equivalent resistance, $R_{EQ}$, that continuously draws power over the half-cycle, but still limits the peak voltage on $C_R$ to
This equivalent resistance model, as shown in Figure C.2, mimics the loading of the rectifier, but significantly simplifies the analysis. However, the appropriate value of $R_{EQ}$ must be determined, and its value is subject to the following constraint:

$$|V_c| = V_{C(PK)}.$$  \hfill (C.2)

To demine how this constraint translates to the $v_{EMF,R}$ voltage, the transfer function from $V_{emf,r}$ to $V_c$ can be expressed as

$$\frac{V_c}{V_{emf,r}} = \frac{1}{s^2L_RC_R + \frac{sL_R}{R_{EQ}} + 1},$$  \hfill (C.3)

and as the $L_R$-$C_R$ is resonantly driven,

$$\frac{V_c}{V_{emf,r}} \bigg|_{s=j\omega} = \frac{R_{EQ}}{j\omega L_R}.$$  \hfill (C.4)

By substituting Equation (C.4) into Equation (C.2)

$$R_{EQ} = \omega L_R \frac{|V_{C(PK)}|}{|V_{emf,r}|},$$  \hfill (C.5)

Figure C.2. Equivalent resonant receiver (a) circuit with (b) corresponding time-domain waveforms.

Now that the appropriate loading may be emulated with the $R_{EQ}$ value in Equation (C.5), the average power sourced by $v_{EMF,R}$ can be found with
\[ P_{EMF,R} = \frac{1}{2} \text{Re}\{ V_{\text{emf},r} I_1^* \}. \]  

(C.6)

The phasor \( I_1 \) can be written in terms of \( V_{\text{emf},r} \) (with driving angular frequency \( \omega_O \))

\[ I_1 = \frac{V_{\text{emf},r}}{j\omega_O L_R + \frac{R_{EQ}}{1 + j\omega_O R_{EQ} C_R}}, \]  

(C.7)

which further simplifies with Equation (C.5) to

\[ I_1 = \frac{V_{\text{emf},r}}{j\omega_O L_R} \left( 1 + j \frac{V_{C(PK)}}{V_{\text{emf},r}} \right). \]  

(C.8)

Finally, inserting Equation (C.8) into Equation (C.6) results in

\[ P_{EMF,R} = -\frac{1}{2} \left( \frac{V_{\text{emf},r} V_{C(PK)}}{\omega_O L_R} \right), \]  

(C.9)

where the negative sign suggests that power is being sourced. The negative sign is simply used for perspective and can be dropped when referred to as sourced power.
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