Thin Film Resistance to Hydrofluoric Acid Etch with Applications in Monolithic Micro-electronic/MEMS Integration

A Thesis
Presented to
The Academic Faculty
by
Todd G McKenzie

In Partial Fulfillment
of the Requirements for the Degree
Master of Science in Electrical and Computer Engineering

School of Electrical and Computer Engineering
Georgia Institute of Technology
July 2003
Thin Film Resistance to Hydrofluoric Acid Etch with Applications in Monolithic Microelectronic/MEMS Integration

Approved by:

Dr. James Meindl

Dr. Zhijing Zhou

Dr. Mark Allen

Date Approved 7/10/2003
Optimus Parentibus
ACKNOWLEDGEMENTS

I would like to thank the members of the CMOS and GSI groups at the Microelectronics Research Center. Thanks to Leslie Oommen George, Frederic L'Herbec, Somaskanda Thyagaraja, and Eric Woods for their assistance. I would also like to thank Dr. James Meindl, Dr. Zhiping Zhou, and Dr. Mark Allen for serving on my thesis committee. Special thanks to Dr. Zhou for his guidance.
TABLE OF CONTENTS

DEDICATION iii

ACKNOWLEDGEMENTS iv

LIST OF TABLES vii

LIST OF FIGURES viii

I INTRODUCTION 1
   1.1 Thesis Focus ........................................... 1
   1.2 Microelectronics/MEMS Background ...................... 2
   1.3 Structure of the Thesis ................................ 10

II CHEMISTRY OF ETCHING UTILIZING HYDROFLUORIC ACID 11
   2.1 Hydrofluoric Acid ....................................... 11
   2.2 Silicon Dioxide and Hydrofluoric Acid ................. 12
   2.3 Metals and Hydrofluoric Acid .......................... 12

III TECHNICAL FOCUS AND MATERIAL CONSIDERATIONS 15
   3.1 Thin Film Performance During Etch ..................... 15
   3.2 Application to Microelectronic/MEMS Integration ........ 16
   3.3 Material Considerations ................................ 16

IV ANALYTICAL TECHNIQUES AND EXPERIMENTAL METHODS 19
   4.1 Etch Resistance Test ................................... 19
   4.2 Barrier During HF Attack Test ......................... 20
   4.3 Circuitry Protection Test ............................... 23

V EXPERIMENTAL RESULTS 29
   5.1 Test Structure and Sacrificial Material Etch Resistance 29
   5.2 Protective Material Etch Resistance .................... 30
   5.3 Concentrated HF Barrier Performance .................. 48
   5.4 Protection For Underlying Microelectronics Application 53

VI CONCLUSIONS 55
   6.1 Suggestions for Future Work ............................ 57
### LIST OF TABLES

<table>
<thead>
<tr>
<th>Table</th>
<th>Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Simplified run sheet for a M2MS-first microelectronic/MEMS integrated process.</td>
<td>9</td>
</tr>
<tr>
<td>2</td>
<td>Bulk Silicate Glass Etch Rates at 25°C (µm/min)</td>
<td>13</td>
</tr>
<tr>
<td>3</td>
<td>Survey of HF Attack of Select Metallic Materials</td>
<td>14</td>
</tr>
<tr>
<td>4</td>
<td>Protective Material Candidates</td>
<td>17</td>
</tr>
<tr>
<td>5</td>
<td>Select Metal Thin Film Electrical Resistivities</td>
<td>20</td>
</tr>
<tr>
<td>6</td>
<td>Keithley 2600 resistance test specification</td>
<td>23</td>
</tr>
<tr>
<td>7</td>
<td>Underlying microelectronic metallization test structure fabrication run sheet</td>
<td>28</td>
</tr>
<tr>
<td>8</td>
<td>Test structure vs. time to discontinuity (mins).</td>
<td>54</td>
</tr>
<tr>
<td>9</td>
<td>Time to first sign of adhesion loss of selected films to silicon and silicon dioxide when exposed to hydrofluoric acid</td>
<td>56</td>
</tr>
</tbody>
</table>
LIST OF FIGURES

1 Package-Level Microelectronic/MEMS Integration .................. 4
2 Chip-Level Microelectronic/MEMS Integration ....................... 4
3 Device-Level Microelectronic/MEMS Integration ...................... 5
4 Hydrogen bonding between covalently bonded HF molecules. Covalent and hydrogen bonds are shown with solid and dotted lines, respectively. .................. 12
5 Titanium test pattern (shown shaded) on a silicon wafer. ............. 21
6 Top portion of wafer covered to partially block subsequent deposition. .. 21
7 Completed HF barrier test structure. ................................ 21
8 Experimental Test Wafer Holder ...................................... 22
9 Cadence layout of test structure design .............................. 23
10 Test structure 1 .................................................. 24
11 Test structure 1 closeup ........................................... 24
12 Test structure 2 .................................................. 25
13 Test structure 3 .................................................. 26
14 Test structure 3 closeup ........................................... 26
15 Fabricated Ti Test Pattern ........................................... 27
16 SiO2 film thickness vs. time for concentrated HF immersion etch test. .. 29
17 Al film thickness vs. time for concentrated HF immersion etch test. .... 30
18 Cr film thickness vs. time for concentrated HF immersion etch test. ..... 31
19 The chromium-coated wafer subsequent to 6 minute etch. .............. 32
20 Chromium film surface after 2 minutes of hydrofluoric acid attack. ...... 32
21 Chromium film surface after 4 minutes of hydrofluoric acid attack. ...... 33
22 Chromium film surface after 6 minutes of hydrofluoric acid attack. ...... 33
23 Mo film thickness vs. time for concentrated HF immersion etch test. ..... 34
24 Molybdenum film surface after 15 minutes of hydrofluoric acid attack; some pinholes have formed ........................................... 35
25 Ni film thickness vs. time for concentrated HF immersion etch test. ..... 36
26 The nickel-coated wafer subsequent to 30 seconds etch. ............... 36
27 Nickel film surface after 30 seconds of hydrofluoric acid attack; pinholes have formed ........................................... 37

viii
28 Nickel film surface after 30 seconds of hydrofluoric acid attack; cracks have formed near the edge of the wafer. ........................................... 37
29 The platinum-coated wafer subsequent to etch 10 minute etch. ........................................... 39
30 Platinum film surface after 10 minutes of hydrofluoric acid attack. Circular crack-like features have formed. ........................................... 39
31 Platinum film surface after 10 minutes of hydrofluoric acid attack. Cracks in the film are easily seen here at the edge of the wafer. ........................................... 40
32 Si3N4 film thickness vs. time for concentrated HF immersion etch test. ........................................... 41
33 The silicon nitride-coated wafer subsequent to 30 seconds HF etch. ........................................... 41
34 Silicon nitride film surface after 30 seconds of hydrofluoric acid attack. The film uniformity subsequent to etch is poor and has a standard deviation of over 200Å........................................... 42
35 The silver-coated wafer subsequent to 10 minute HF etch. ........................................... 43
36 Silver film surface after 10 minutes of hydrofluoric acid attack. Large areas which have partially delaminated from the substrate are visible. ........................................... 43
37 Ta film thickness vs. time for concentrated HF immersion etch test. ........................................... 44
38 Tantalum wafer subsequent to 6 minute etch. The Ta film has been etched at the interface, leaving a small circle of film behind. ........................................... 45
39 Tantalum film surface after 6 minutes of hydrofluoric acid attack. Here the edge of the remaining Ta film is shown. ........................................... 45
40 W film thickness vs. time for concentrated HF immersion etch test. ........................................... 46
41 Tungsten wafer subsequent to 15 minute etch. Pinholes have formed, but the film is free of cracks and signs of delamination. ........................................... 47
42 Tungsten film surface after 5 minutes of hydrofluoric acid attack. Here pinholes have formed. ........................................... 47
43 Tungsten film surface after 15 minutes of hydrofluoric acid attack; pinholes are abundant. ........................................... 48
44 Continuous resistance measurement vs. time for Ti test structure protected by photore sist during 49% HF immersion. ........................................... 49
45 Continuous resistance measurement vs. time for Ti test structure protected by silicon nitride during 49% HF immersion. ........................................... 49
46 Continuous resistance measurement vs. time for Ti test structure protected by aluminum during 49% HF immersion. ........................................... 50
47 Continuous resistance measurement vs. time for Ti test structure protected by copper during 49% HF immersion. ........................................... 50
48 Continuous resistance measurement vs. time for Ti test structure protected by chromium during 49% HF immersion. ........................................... 51
Continuous resistance measurement vs. time for Ti test structure protected by molybdenum during 49% HF immersion.

Continuous resistance measurement vs. time for Ti test structure protected by platinum during 49% HF immersion.

Continuous resistance measurement vs. time for Ti test structure protected by silver during 49% HF immersion.

Continuous resistance measurement vs. time for Ti test structure protected by tungsten during 49% HF immersion.

Etch rate in concentrated HF vs. protective thin film. Silicon nitride is excised, but has an etch rate of 1566Å/min. The exact etch rates of photore sist, platinum, copper, and silver could not be determined.

Time to failure vs. protective thin film.
CHAPTER I

INTRODUCTION

1.1 Thesis Focus

This thesis examines thin film resistance to hydrofluoric (HF) acid etch. A prominent application of HF-resistant thin films is in the area of monolithic microelectronic/micro-electromechanical systems (MEMS) integration, where the films can be used to protect microelectronics during MEMS release in MEMS-first processes, for example.

Integration of microelectronics and MEMS is important in the fabrication of "smart" sensors/actuators which incorporate electronics with mechanical components. Integrated electronics are able to provide such features as signal amplification, analog to digital (A/D) conversion, standard interfaces, self-testing, fault tolerance, and digital compensation which, in effect, extend overall system accuracy, dynamic range, and reliability.

J. H. Smith et al. [1] have studied the monolithic integration of microelectronics/MEMS extensively and in their work encountered problems using photoresist as a protective layer for microelectronics during undoped, densified glasses etch steps utilizing HF solutions. The inability of photoresist to withstand long HF etches was found to be a factor that imposes limits on the design rules used for spacing release access holes in the structure.

While resists are commonly used as etch masking materials in microfabrication, etch processes involving elevated temperature or high acidity often find these polymer films inadequate. In these cases, certain metals or dielectrics, which can withstand those conditions more effectively, can be used [2]. A thorough understanding of metallic and dielectric thin film resistance to HF etch is therefore essential for the potential utilization of thin films as protective barrier layers during MEMS release steps.

This study encompasses a review of the chemistry of etching utilizing HF, an empirical study of the resistance of metallic and dielectric thin films to HF etch, and a focused study of the application of thin films as protective barrier layers for underlying microelectronics.
during concentrated HF etch processing.

1.2 Microelectronics/MEMS Background

MEMS

The history of micromachining can be traced back to its roots decades ago. The first study of the piezoresistive effect in germanium and silicon was conducted in 1954 by C. S. Smith [3]. The piezoresistive effect is the change in the resistivity of a material due to applied mechanical strain. This strain can be induced by a change in environmental pressure, for example. In fact, the history of silicon pressure sensors is very much representative of the evolution of microsensors, as it is the most successful microsensor design to date.

The piezoresistive coefficients measured by Smith indicated that the gauge factor of Ge and Si strain gauges could potentially be ten to twenty times larger than those for metal strain gauges. As a result, discrete silicon strain gauges were developed commercially just a few years later by several manufacturers. The first high-volume pressure sensor was launched by National Semiconductor in 1974 and included a temperature controller (in a hybrid package) for constant temperature operation. By this time, piezoresistive pressure sensor technology had become a low-cost, batch-fabricated manufacturing technology. Further improvements of this technology included etch stops for improved control of diaphragm etching, the utilization of ion implantation for improved control of the piezoresistor fabrication, anodic bonding (electrostatic bonding) and silicon-to-silicon fusion bonding for improved packaging of the pressure sensors.

While piezoresistive sensors are good solutions in many situations where pressure sensor is required, they are very sensitive to interference. To achieve better sensitivity and stability, capacitive pressure sensors were first developed and demonstrated in the late 1970s and the first integrated monolithic capacitive pressure sensor was reported in 1980 [4].

Later, during the late 1980s, the introduction of new fabrication techniques for mechanisms on silicon were demonstrated [5, 6] and was a turning point for the field. For the first time, it was possible to fabricate mechanical parts that could execute unrestrained motion
in at least one degree of freedom (e.g. gears, gear trains, linkages, etc.). Shortly thereafter, this technology enabled the development of electrostatic micromotors [7,8] and motivated the development of other types of microactuators such as valves, pumps, switches, tweezers, and lateral resonant devices [9].

Microsensor technology has also matured substantially. A variety of sensors for measuring position, velocity, acceleration, pressure, force, torque, flow, magnetic field, temperature, gas composition, humidity, pH, solution/body fluid ionic concentration, and biological gas/liquid/molecular concentrations have been developed and some commercialized.

Microelectronics

The invention of the transistor in 1947 [10,11] initiated a fast-paced microelectronic technology revolution which is still continuing to the present day. The first integrated circuit (IC) was fabricated by Jack Kilby of Texas Instruments in 1958, using a germanium substrate. A few months later, Robert Noyce of Fairchild Semiconductor announced the development of a planar silicon IC.

Since these early beginnings, the complexity of ICs has doubled every two to three years, as predicted by Moore’s Law, since 1970. Unprecedented advances in performance and capability have paralleled this enormous increase in transistor packing density. Over the past two decades, large, expensive, complex systems have been, in many instances, replaced by small, high performance integrated circuits costing many times less than their predecessors. Microprocessors and microcomputers, based on constantly evolving integrated circuit technology, have revolutionized communication, entertainment, health care, manufacturing, management and many other aspects of our lives.

Microelectronic/MEMS Integration

Microelectronic systems would completely cut off from their surroundings were it not for their mechanical interface with the outside world: MEMS. So while performance enhancement and minimum feature size reduction of microelectronics will continue to play an important role in the evolution of the integrated circuit, the integration, and more importantly the monolithic integration, of microelectronics and sensing/actuating functionalities
traditionally provided by components external to integrated circuitry will play an important part in the advancement of microtechnology.

Levels of Integration

Microelectronic and MEMS devices can be integrated at the package, chip, and device levels.

Integration at the package level is shown in Figure 1. At this integration level, microelectronic and MEMS elements are fabricated on separate substrates utilizing distinct processes, individually diced and packaged, and finally integrated together on a printed wiring board (PWB).

![Figure 1: Package-Level Microelectronic/MEMS Integration](image)

The next level of integration, chip-level integration, is shown in Figure 2. Sometimes referred to as multi-chip module (MCM) technology, this level of integration incorporates microelectronics and MEMS chips which are fabricated separately and then subsequently wirebonded together within a single package.

![Figure 2: Chip-Level Microelectronic/MEMS Integration](image)

The deepest level of integration, device-level or monolithic integration, is depicted in
Figure 3. The monolithic integration of microelectronics and MEMS, as the name implies, involves an integrated fabrication process which builds both types of devices on the same substrate.

![Diagram of Chip, Device, Microelectronics, and MEMS integration](image)

Figure 3: Device-Level Microelectronic/MEMS Integration

While integration at the package [12], chip [13, 14], and device-level [15–18] have all been explored, monolithic integration is, in many cases, the best cost-effective high-volume integration method.

Monolithic Microelectronic/MEMS Integration Technology

The monolithic integration of microelectronics and MEMS is the decisive migration from multi-substrate to single-substrate design/processing/packaging schema for these two technologies.

The reduction in overall physical chip count alone can serve as a significant cost savings measure at the system level as it may reduce the use of expensive board space. Combining many chips into one integrated chip also reduces system footprint size in another way. The removal of one level of physical hierarchy, from a design standpoint, allows more freedom during the partitioning and placement stages of the physical design layout process, which can reduce the critical path length of the design. This potential reduction in critical path length can mean an increase in performance, contribute to a decrease in signal degradation and cross-talk, and help improve the SNR ratio [19].

The advantages of device-level integrative designs over package- and chip-level in terms of cost, ease of test, performance impact, miniaturization, and power consumption are considered.
Cost

Cost is an important factor of consideration with regard to process integration. With respect to either the stand-alone microelectronics or MEMS processes, one combined process necessarily leads to an increase in both the mask count and the total process step count which can serve to prolong production time and decrease product yield - both directly proportional to cost. On the other hand, the manufacture of separate chips, factoring in their associated post-fabrication interconnection is very costly both in terms of time expenditure and yield loss. Consequently, microelectronics/MEMS integration is cost-effective in high-volume production or when some other factor is paramount such as light-weight/ultra-small size (viz. medical applications), system performance, or low power consumption (viz. portability).

Testing

The integration of additional functionality on a single chip can make the post-fabrication testing more difficult than with smaller, less complicated chips. This is one reason why self-test functions are often included in the design of microelectronics/MEMS integrated systems as it saves both test time and cost. In fact, the self-test and auto-calibration capabilities of microelectronic/MEMS integrated systems (as opposed to hybrid systems) contribute quite significantly to their cost effectiveness [20].

Performance

Microelectronic/MEMS integration allows for a great increase in performance for a number of reasons. The fact that MEMS and microelectronics devices are physically closer to one another (and thus suffer a lower parasitic interconnection) reduces signal degradation, cross-talk, and overall signal-to-noise ratio (SNR). In addition, amplification of sensor signals at the sensor site also allows for the full utilization of the dynamic range of the A/D converter, a common component of microelectronic/MEMS integrated systems.
Minimautization

Miniaturization is not a new idea in the arena of microelectronics. Only in this sense, the goal of miniaturization is not solely the increase of transistor packing density, but rather the increased diversification of on-chip functionality in an ultra-compact light-weight monolithic system. Microelectronic/MEMS integration makes a significant contribution to the compactness of the overall system.

Power Consumption

As many of the microelectronic/MEMS systems are portable in natural, low power consumption is of great concern. The monolithic integration of microelectronics and MEMS technologies is conducive to power consumption reduction. The shorter interconnects between the two devices allows for less transconductive heating and therefore less energy loss in the system.

Benefits and Challenges

As described above, microelectronic/MEMS monolithically integrated systems provide the benefits of reliability, flexibility, plug & play capability through digital interfaces, simple calibration, self-test, miniaturization, and low cost. Fabrication of these monolithic microelectronic/MEMS integrated systems, on the other hand, provide a unique challenge.

Monolithic Microelectronic/MEMS Integrated Fabrication

Two important categories of such microelectronic/MEMS integration techniques (MEMS-first and MEMS-last) clearly define the position of the principal MEMS fabrication steps within the process sequence. Certain tradeoffs must be made with either integration technique.

MEMS-Last

The fabrication of MEMS structures following microelectronics processing completion is a microelectronic/MEMS integration approach which has been studied by many groups [21-,
23] and requires significant modification of the microelectronics process due the high temperature deposition (≈ 600°C) and annealing steps (≈ 900°C) associated with commonly-used polysilicon MEMS structural films. While these high temperature processes are employed to achieve low-resistive, low-tensile-strength MEMS films, such heat steps are not compatible with microelectronic fabrication. Such high temperature processes cause unwanted diffusion of dopants in microelectronics devices (P⁺ source and drain regions and threshold voltage adjustment implants are both especially susceptible) and are limited to the melting temperature of the microelectronic metallization. Temperature constraints are usually set at around 450°C, with a possible ceiling of 525°C [24]. To deal with this issue, several combative measures have been employed by various researchers. To reduce the effect of high temperature constraint of microelectronics metallization, researchers have tried replacing Al metalization with Tungsten, which has a higher melting point. Unfortunately, using W-based metalization has been found to degrade transistor performance and increase the complexity of IC fabrication [25]. Also, to reduce the required high deposition and anneal temperatures of polysilicon-based MEMS structures, polycrystalline silicon-germanium [26] or pure germanium [27] can be used to replace polysilicon as a structural material.

The utilization of polysilicon in a MEMS-first fabrication approach to monolithic microelectronic/MEMS integration is an impractical, but not impossible task. The high temperature deposition and annealing steps required for polysilicon processing necessitates profound modification of both the standard microelectronic and MEMS processes. This is a significant disadvantage with respect to MEMS-first integration processes with similar materials.

MEMS-First

Fabrication of MEMS structures prior to the fabrication of microelectronics fabrication is an important and well-explored solution space for microelectronic/MEMS integrated processes. Prima facie this approach is very attractive as it requires little modification of either the microelectronic or MEMS fabrication processes. There are, however, several issues (viz. step coverage, passivation, counter-doping) associated with MEMS-first integration which must be addressed. Problems are often encountered during microelectronic
1. Fabricate MEMS
2. Fill with sacrificial material
3. Cover MEMS
4. Fabricate microelectronics
5. Uncover MEMS
6. Protect microelectronics
7. Release MEMS by etching sacrificial material
8. Remove microelectronics protection

Table 1: Simplified run sheet for a MEMS-first microelectronic/MEMS integrated process.

processing due to uneven topography of high profile MEMS structures. This problem can be avoided entirely by recessing the MEMS structures in a trench, filling them in, and then planarizing [28]. If phosphosilicate glass (PSG) doped films are used as a sacrificial material for MEMS release or heavily doped MEMS structures are situated in close proximity to microelectronics, well drive-in steps can cause counter-doping problems. Each of these problems can easily be avoided with minimal effort by utilizing undoped or lightly doped sacrificial layers and imposing strict design spacing rules, for example. Such spacing rules would help ensure that MEMS structures that contain metals, polymers, or piezoelectrics do not contaminate microelectronic devices.

The MEMS-first approach to monolithic microelectronic/MEMS integration requires virtually no modification to either the standard microelectronic or MEMS processes. This is a huge advantage as IC manufacturers have invested enormous resources into the development of standard CMOS, bipolar and BICMOS processes. Using these same processes as a vehicle for monolithic microelectronic/MEMS integration reduces the non-recurring engineering cost of the integration effort significantly.

A simplified process run sheet for MEMS-first microelectronic/MEMS integrated processes is given in Table 1. The thin film thesis research presented here has a direct application MEMS-first monolithic microelectronic/MEMS integration (viz. steps 6-7 of Table 1).
1.3 Structure of the Thesis

Chapter II describes the chemistry of etching using hydrofluoric acid. The HF etch of silicon dioxide and attack of HF on metals and metal oxides is considered. Chapter III outlines the focus of the thesis and the materials involved. It provides motivation for the experiments presented in the next chapter. Chapter IV introduces several experiments relating to thin films and protection against HF. Chapters V and VI reveal the results and draw conclusions based on these experimental findings, respectively.
CHAPTER II

CHEMISTRY OF ETCHING UTILIZING HYDROFLUORIC ACID

2.1 Hydrofluoric Acid

Hydrofluoric acid (HF) is very commonly used in microfabrication as it is an excellent etchant of various oxides such as silicon dioxide (SiO₂). This is important because SiO₂, which is native to the silicon wafers used as substrates in the manufacture of microelectronics, has a wide variety of uses including functioning as an isolation material, interdielectric material, or gate oxide, for example. Hydrofluoric acid, with or without the addition of ammonium fluoride (NH₄F), is used almost exclusively for the wet chemical etching of SiO₂. The addition of NH₄F to HF yields a so-called buffered HF (BHF) which attacks photoresist less readily and maintains pH level via replenishment of HF by,

\[ \text{NH}_4\text{F} \rightarrow \text{NH}_3 + \text{HF}. \]  \hspace{1cm} (1)

Basic chemical etch by HF is quite complex and dependent on the ionic strength, the solution pH, and etchant composition which determine the available quantities of solution species including HF²⁻, HF, F⁻, H⁺, and various fluoride polymers [2]. The chemical structure of liquid HF acid resembles the zigzag chainlike species shown in Figure 4. Note the linearity of the [F-H-⋯F] system. Such linearity is presumably caused by the electrostatic repulsion between the bond-pair clouds surrounding the H atom [29].
2.2 Silicon Dioxide and Hydrofluoric Acid

One of the most widely used etching processes is the wet etching of SiO$_2$ in dilute solutions of HF acid [38] described by Equations 2 and 3. Equation 4 shows the overall reaction.

\[
\text{SiO}_2(s) + 4\text{HF}(aq) \rightarrow \text{SiF}_4(g) + 2\text{H}_2\text{O}(aq)
\]  

(2)

\[
\text{SiF}_4(g) + 2\text{HF}(aq) \rightarrow \text{H}_2\text{SiF}_6(aq)
\]  

(3)

\[
\text{SiO}_2(s) + 6\text{HF}(aq) \rightarrow \text{H}_2\text{SiF}_6(aq) + 2\text{H}_2\text{O}(aq)
\]  

(4)

Since the bond dissociation enthalpy (the bond strength) for the H-F bond is very high (+560 kJ·mol$^{-1}$), the equilibrium lies much more to the left, giving a weaker acid. The hydrogen bonding between the HF molecules is also very strong due to the large dipole moment.

The etch rate of various silicate glass films in popular HF solutions is shown in Table 2 below [2].

2.3 Metals and Hydrofluoric Acid

The reaction between metals and HF can be described as typical oxidation and reduction phenomena. In most cases, the process is one of reduction of hydrogen to molecular

\footnote{Compositions of the concentrated aqueous solutions HF and HNO$_3$ are 40% and 70%, respectively.}
Table 2: Bulk Silicate Glass Etch Rates at 25°C (μm/min)

<table>
<thead>
<tr>
<th>SiO₂ Type</th>
<th>HF·H₂O</th>
<th>20HF·14HNO₃·66H₂O</th>
<th>454gNH₄F·654mlH₂O·163mlHF</th>
</tr>
</thead>
<tbody>
<tr>
<td>CVD SiO₂</td>
<td>1.8</td>
<td>0.44</td>
<td>0.48</td>
</tr>
<tr>
<td>Thermal SiO₂</td>
<td>0.3</td>
<td>0.11</td>
<td>0.11</td>
</tr>
<tr>
<td>Fused SiO₂</td>
<td>0.29</td>
<td>0.15</td>
<td>0.12</td>
</tr>
</tbody>
</table>

hydrogen, while the fluorine combines with the metal to form metallic fluorides [31] as in Equations 5, 6, and 7.

\[
6\text{HF(aq)} + 2\text{Al(s)} \rightarrow 2\text{AlF}_3(s) + 3\text{H}_2(g) \quad (5)
\]

\[
12\text{HF(aq)} + 2\text{Ti(s)} \rightarrow 2[\text{TiF}_6]^{3-}(\text{aq}) + 3\text{H}_2(g) + 6\text{H}^+(\text{aq}) \quad (6)
\]

\[
4\text{HF(aq)} + 2\text{Ni(s)} \rightarrow 2\text{NiF}_2(s) + 2\text{H}_2(g) \quad (7)
\]

In industrial applications, the corrosion of metals in HF can be shown by the increase of air pressure in a closed system (with the reduction of hydrogen) [32]. The rate of corrosion is usually quantified by the weight loss of the material over time. Nearly all metals form protective films or scales which decrease the initial high corrosion rates of these materials. After the formation of the scale, the rate of diffusion of HF through the scale and the rate at which scales delaminate from the substrate surface play larger parts in the rate of corrosion than the reaction rate of the metal with HF.

Metallic Thin Films

With metallic thin films, one must also take into account the etch rate of any native oxide on the metal surface. Metals that form native oxides have different initial etch rates, as the oxides must first be removed by the etchant prior to the etching of the underlying metals. Such oxide etching steps are shown in Equations 8, 9, and 10.

\[
6\text{HF(aq)} + \text{Al}_2\text{O}_3(s) \rightarrow 2\text{AlF}_3(s) + 3\text{H}_2\text{O(aq)} \quad (8)
\]

13
<table>
<thead>
<tr>
<th>Material</th>
<th>Reactivity with Hydrofluoric Acid</th>
</tr>
</thead>
<tbody>
<tr>
<td>Aluminum</td>
<td>Concentrated hydrofluoric acid is not an excellent etchant of aluminum. Dilute solutions of HF can, however, be used as an Al etchant [33]. In particular, nitric acid-hydrofluoric acid mixtures such as 50mL/L,7 40% HF and 250mL/L,7 40% nitric acid is recommended, for example, as an etchant for aluminum thin films [34]. Exposure to HF causes thin film fluorination of aluminum films (see Equation 5). The resulting aluminum fluoride film can be 200Å thick and greater than 500Å fluorine [35].</td>
</tr>
<tr>
<td>Copper</td>
<td>Exposure to HF causes an approximately 100-500Å thick fluoride film [35].</td>
</tr>
<tr>
<td>Molybdenum</td>
<td>Molybdenum, in particular when an anode, is dissolved by anhydrous HF at such a high rate that this reaction can be utilized for preparing molybdenum fluoride films [36].</td>
</tr>
<tr>
<td>Nickel</td>
<td>Nickel is actually recommended as materials for the transport and storage of hydrofluoric acid, since the etch rate at room temperature remains under 2000Å/min [97].</td>
</tr>
<tr>
<td>Platinum</td>
<td>It is reported that platinum is not attacked at room temperature in 40% HF [38] or higher concentrations [39]. In addition, platinized titanium has been shown to be a good electrode material in electrolytes which contain HF [40].</td>
</tr>
<tr>
<td>Titanium</td>
<td>Hydrofluoric acid strongly attacks Ti. The resulting titanium fluoride creates significant residues [35].</td>
</tr>
</tbody>
</table>

Table 3: Survey of HF Attack of Select Metallic Materials

\[
4\text{HF(aq)} + \text{TiO}_2(s) \rightarrow \text{TiF}_4(s) + 2\text{H}_2\text{O(aq)}
\]  \hspace{1cm} (9)

\[
2\text{HF(aq)} + \text{NiO}(s) \rightarrow \text{NiF}_2(s) + \text{H}_2\text{O(aq)}
\]  \hspace{1cm} (10)

Survey of HF Attack of Selected Metallic Materials

The attack of HF on many metallic materials has been studied by many researchers. A survey of these studies is shown in Table 3 for reference.
CHAPTER III

TECHNICAL FOCUS AND MATERIAL CONSIDERATIONS

3.1 Thin Film Performance During Etch

Thin film resistance to chemical attack requires good initial film quality, strong adhesion to the substrate, and superior chemical etch resistance to the etchant.

Film Quality

The deposition of the film in a manner that provides for strong film quality is vital for subsequent film performance under etch conditions. It is strictly required that the film is free of cracks or pinholes that would cause non-uniform etch characteristics. Factors that may affect film quality include the introduction of contaminants during film deposition or uneven spatial power/temperature deposition.

Adhesion

Proper adhesion between the substrate and thin film during etch processing is crucial. Properties of adhesion with respect to a selected thin film is strictly substrate dependent. Adhesion loss usually occurs in one of two ways: 1) edge attack at the interface by the etchant 2) failure over a large area (e.g. lifting, peeling, crazing). It is important to use an uncontaminated initial substrate, as a poor interface between substrate and film is often a result of substrate surface contamination prior to deposition.

Chemical Resistance to Etchant

The film should exhibit strong chemical resistivity against the etchant. The etch rate of the film in the etchant should be as low as possible, preferably many times lower than the target etch material to provide for good etch selectivity. Pitting and cracking, frequently
encountered varieties of localized corrosion, should not compromise this film integrity during etch. It should be noted that a complete understanding of the reasons for pit initiation at specific spots on a metal surface continues to be lacking despite several decades of experimental data accumulated and published in the area [41]. Instances of localized corrosion on the substrate surface are noted and presented in micrographs in the Thin Film Experimental Results chapter.

3.2 Application to Microelectronic/MEMS Integration

An important step in MEMS-first microelectronic/MEMS integrative processes is the release of polysilicon MEMS structures by the sacrificial etching of silicon dioxide. Indeed, this process is the most-widely used finishing key step in surface micromachining [42]. The protection of circuitry during this release step is crucial in microelectronic/MEMS integrated processes that fabricate MEMS utilizing surface micromachining techniques.

3.3 Material Considerations

Substrate

The substrate to be used for testing is a < 100 > Si test-grade wafer. It is therefore required that the thin film adhere well to both Si and SiO₂, silicon's native oxide.

Structural and Sacrificial Materials

The release of polysilicon MEMS structures via the etch of SiO₂ utilizing HF solutions is a vital process in surface micromachining. It is important to distinguish between the different ways in which silicon dioxide can be grown. Wet and dry oxidations are both growth processes where silicon dioxide is grown on a silicon wafer surface in a high temperature process with or without the presence of water vapor (hence the names wet and dry). The way in which oxide is introduced to the silicon wafer surface determines such properties as oxide density. The sacrificial silicon dioxide used in this work is grown by a wet oxidation process. This type of oxide, which is less dense than dry oxide, etches very quickly in 49% HF [ > 1 μm/min¹ ] and exhibits high thickness uniformity across the wafer surface.

¹Experimental finding, page 29
Table 4: Protective Material Candidates

<table>
<thead>
<tr>
<th>Material</th>
</tr>
</thead>
<tbody>
<tr>
<td>Aluminum</td>
</tr>
<tr>
<td>Chromium</td>
</tr>
<tr>
<td>Copper</td>
</tr>
<tr>
<td>Molybdenum</td>
</tr>
<tr>
<td>Nickel</td>
</tr>
<tr>
<td>Photoresist</td>
</tr>
<tr>
<td>Platinum</td>
</tr>
<tr>
<td>Silicon Nitride</td>
</tr>
<tr>
<td>Silver</td>
</tr>
<tr>
<td>Tantalum</td>
</tr>
<tr>
<td>Tungsten</td>
</tr>
</tbody>
</table>

Etchant

As mentioned previously, HF is often used to etch SiO₂ in surface micromachining applications. Various concentrations of HF are utilized for this purpose and a buffering agent may or may not be used in conjunction with the HF etch solution. In this work, 49% HF without buffering agent will serve as the etchant of interest.

Protective Material Candidates

The thin films shown in Table 4 were selected to be evaluated in this study. All of these materials are able to be deposited using low temperature processes (<400°C), thus they are compatible with post-microelectronics from a thermal-budget standpoint. It should be noted that a microelectronics-compatible selective removal process is also required for each of the candidate protective films, but investigation in this latter area is beyond the scope of this work. The research herein focuses upon the resistance of films to hydrofluoric acid and the protection of microelectronics against HF.

Metals are deposited by DC sputtering, photoresist by spinning, and silicon nitride by Plasma Enhanced Chemical Vapor Deposition (PECVD). The deposition of silicon nitride requires some additional commentary and is provided here.

1The type of photoresist studied is not necessarily a thin film at 27,000Å, but included for completeness.
Silicon Nitride

Silicon Nitride is often deposited by way of Chemical Vapor Deposition (CVD). Low Pressure CVD (LPCVD) Si$_3$N$_4$ films have a relatively high density and thus a low etch rate in HF, however they are unsuitable for post-microelectronics processing due to their high temperature characteristic. LPCVD processes have typical deposition temperatures between 700 and 900°C which exceeds the melting point of most metalization (e.g. Al, 660.38°C).

Plasma Enhanced CVD (PECVD) silicon nitride processes operate at only 300 to 400°C. While films deposited in this manner are known to have a relatively higher etch rate in HF (910-1050Å/min), they are within the thermal budget for most post-micro electronic processing.
CHAPTER IV

ANALYTICAL TECHNIQUES AND EXPERIMENTAL METHODS

The overall goal of this series of experiments is to discover which materials can withstand long HF etch steps, i.e. processes such as MEMS release steps. Maintenance of film integrity is of critical importance in this application as a strong acid barrier is required to protect underlying microelectronic circuitry. Descriptions of various experiments which were performed to evaluate the resistance of select thin films against HF attack are given.

4.1 Etch Resistance Test

To test adhesion, a bare <100> Si test-grade wafer and one with 5000Å layer of wet-SiO₂ was growth are uniformly coated with the selected protective thin film. The wafers are then immersed with agitation in a 49% HF:H₂O solution. Signs of delamination are noted and micrographs provided.

The etch rate of the protective material on a bare silicon substrate when exposed to 49% HF was then measured. Since the etch rate of pure silicon in HF is virtually negligible, any thickness reduction in the protective layer film can be solely attributed to protective layer etch when using profilometry to measure film thickness.

To calculate the thickness of each of the metallic thin films, the sheet resistivity of the sputtered film was measured using a Veeco Instruments FPP6000 four-point probe. The sheet resistivity, \( R_S \), of a film is given by

\[
R_S = \frac{\rho}{t}
\]

where \( \rho \) is the material's electrical resistivity and \( t \) is the film thickness [43]. Table 5 shows the resistivities for various metallic thin films [44].
<table>
<thead>
<tr>
<th>Metal</th>
<th>Resistivity (μΩ-cm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Aluminum</td>
<td>2.65</td>
</tr>
<tr>
<td>Chromium</td>
<td>12.7</td>
</tr>
<tr>
<td>Copper</td>
<td>1.7</td>
</tr>
<tr>
<td>Molybdenum</td>
<td>5.0</td>
</tr>
<tr>
<td>Nickel</td>
<td>7.0</td>
</tr>
<tr>
<td>Platinum</td>
<td>10.6</td>
</tr>
<tr>
<td>Silver</td>
<td>1.6</td>
</tr>
<tr>
<td>Tantalum</td>
<td>13.0</td>
</tr>
<tr>
<td>Titanium</td>
<td>40.0</td>
</tr>
<tr>
<td>Tungsten</td>
<td>5.0</td>
</tr>
</tbody>
</table>

Table 5: Select Metal Thin Film Electrical Resistivities

Solving for \( t \), the result is

\[
 t = \frac{\rho}{R_\theta} .
\]  

Thus combining the values for \( \rho \) in Table 5 with the four point probe sheet resistivity data collected, the thin film thickness is easily computed.

### 4.2 Barrier During HF Attack Test

In this test, the protective properties of each thin film against hydrofluoric acid were quantified. The electrical resistance of an underlying titanium film was measured over time. Titanium, which is etched extremely quickly in HF, was covered first with a dielectric and then with the selected thin film to provide protection against the HF.

**Test Structure Fabrication**

A 2100Å layer of titanium was sputtered/block patterned onto a silicon wafer as shown in Figure 5. The top region of the wafer was then covered (Figure 6) and a 1000Å layer of silicon nitride was deposited via PECVD followed by the sputtering of 5000Å of the select thin film. The cover was then removed exposing the Ti pads at the top of the wafer (Figure 7). The initial electrical resistivity of this test structure is \( \approx 100\,\Omega \).
Figure 5: Titanium test pattern (shown shaded) on a silicon wafer.

Figure 6: Top portion of wafer covered to partially block subsequent deposition.

Figure 7: Completed HF barrier test structure.

Test Procedure

The exposed titanium pads were connected with alligator clips to a Keithley 2000 Digital Multimeter (DMM). A software application was written in National Instruments LabView to communicate with the DMM through a General Purpose Interface Bus (GPIB) connection and sample resistance data then display it graphically as well as store the raw data into a
The wafer was half-submerged vertically (utilizing the test wafer holder shown in Figure 8) such that the bottom two-thirds of the wafer was immersed in HF, while the contact pads were in air.

![Experimental Test Wafer Holder](image)

The resistance across the pads of the test structure was recorded over time. Sudden spikes in resistance indicate the critical attack of the Ti metal lines by HF due to etch-through or delamination of the protective film, while gradual resistance increases indicate pinholes or small cracks in the protective film.

The DIM parameters relating to the electrical resistance measurement are shown in Table 6. [45]
<table>
<thead>
<tr>
<th>Range</th>
<th>Resolution</th>
<th>Test Current</th>
</tr>
</thead>
<tbody>
<tr>
<td>10Ω</td>
<td>100μΩ</td>
<td>1 mA</td>
</tr>
<tr>
<td>1kΩ</td>
<td>1 mΩ</td>
<td>1 mA</td>
</tr>
<tr>
<td>10kΩ</td>
<td>10 mΩ</td>
<td>100 μA</td>
</tr>
</tbody>
</table>

Table 6: Keithley 2000 resistance test specification.

4.3 Circuitry Protection Test

Lateral and Vertical Etch Penetration.

This series of tests quantifies damage to metal lines beneath the protective layer material when exposed to the concentrated HF etch solution. The design in Figure 9 was constructed using the Cadence Virtuoso design layout tool. The layout includes three types of test structures (referred to as Test structure 1, 2, & 3).

![Cadence layout of test structure design](image)

Figure 9: Cadence layout of test structure design

23
Test structure 1, shown in Figures 10 and 11, was developed to test the vertical etch penetration of the acid (i.e. diffusion of the acid through the protective material). The test structure is comprised of a 15µm wide serpentine pattern occupying a 5mm x 5mm square area.

![Test structure 1](image1)

**Figure 10: Test structure 1**

![Test structure 1 closeup](image2)

**Figure 11: Test structure 1 closeup**

We can calculate the resistance of the pattern with

\[
R = \rho \frac{L}{t \cdot W},
\]

where \( \rho \) is the electrical resistivity, \( t \) is the thickness of the film, and \( L \) and \( W \) are the length and width of the metal line. We will assume a 2100Å thick Ti film and estimate

24
the resistance of the test pattern by considering only the resistance contribution of the serpentine pattern. We calculate the length of the serpentine metal lines by

\[ L = \frac{5\text{mm}}{50\mu\text{m}} \cdot 5\text{mm} = 83.3\text{cm}, \]

(14)

and solve for \( R \) in Equation 13 yielding

\[ R = \frac{40\mu\Omega \cdot \text{cm}}{2100\AA} \cdot \frac{83.3\text{cm}}{15\mu\text{m}} = 185k\Omega. \]

(15)

Test structure 2, shown in Figure 12, was developed to test the lateral etch penetration of the acid (i.e. acid attack at the substrate/protective material interface). Notice in the figure that the protective material overlaps the underlying metal lines, but that the surface distance from the edge of the protective material to the metal line is relatively small (in this drawing only 50\( \mu \)m). Three different overlap distances (10, 25, and 50 \( \mu \)m) were included to test the linearity of interface attack.

![Figure 12: Test structure 2](image)

The comb tooth structure, test structure 3 shown in Figures 13 and 14, was developed to test the functionality of the test structures. Discontinuity between the two pads of this test structure ensures the completion of the Ti etch process during test structure fabrication.
**Test Structure Fabrication**

The test structures described in the previous section were fabricated (see Figure 10) utilizing the steps shown in Table 7.
1. Sputter Ti; 30 min @ 3.5% power, yielding an approximately 2100Å thick film
2. Coat PR; Shipley 1827 @ 5000 RPM, 2600 r/s, 30 sec
3. Softbake; 115°C for 115 seconds
4. Expose; 10 seconds using Constant Intensity Channel 2
5. Develop; MF319 for 45 seconds
6. Hardbake; 120°C for 30 minutes
7. Etch Ti; Reactive Ion Etch utilizing a BCl₃,Cl₂,CHCl₃ chemistry
8. Remove PR; 1165 Remover @ 80°C for 5 minutes
9. Cover pads using cleaved wafer section
10. Deposit PECVD Si₃N₄; ≈1000Å
11. Sputter 5000Å of the protective material
12. Remove pad cover
13. Coat PR; Shipley 1827 @ 5000 RPM, 2600 r/s, 30 sec
14. Softbake; 115°C for 115 seconds
15. Expose; 10 seconds using Constant Intensity Channel 2
16. Develop; MF319 for 45 seconds
17. Hardbake; 120°C for 30 minutes
18. Protective Material Etch; (bottom half of wafer only)
19. Remove PR; 1165 Remover @ 80°C for 5 minutes

Table 7: Underlying microelectronic metallisation test structure fabrication run sheet
CHAPTER V

EXPERIMENTAL RESULTS

5.1 Test Structure and Sacrificial Material Etch Resistance

The test structure material and sacrificial material are Ti and SiO₂, respectively. The etch resistance to concentrated 49% HF is presented.

Silicon Dioxide

The etch rate of silicon dioxide (grown by the wet oxidation method) in 49% HF is computed in the following figure and shown to be more than 12,700 Å/min.

![Figure 16: SiO₂ film thickness vs. time for concentrated HF immersion test.](image)

Titanium

It is known that titanium film etch extremely rapidly in concentrated hydrofluoric acid solutions. Titanium films of various thickness were tested with 49% HF. Etches proceeded at such a high rate, that the exact etch rate could not be accurately determined. For
example, a 6000Å Ti film was etched in less than three seconds.

5.2 Protective Material Etch Resistance

Etch rate of various protective material in concentrated 49% HF are given, surface damage is noted, and images are provided.

It should be noted that the measured etch rate of the metallic protective films is done by way of four point probe, so pinholing and cracking of the film subsequent to etch may slightly artificially increase the measured etch rate with respect to the actual height of film if measured by profilometry, for example. Pinholing and cracking both undermine the protective capabilities of the film against the etchant.

Aluminum

A 9870Å layer of aluminum was sputtered onto the surface of a silicon wafer with 5000Å of wet oxide growth. Subsequent HF etch proceeded at approximately 1059Å/min (Figure 17). The surface was attacked evenly with no cracks or pitting.

![Figure 17: Al film thickness vs. time for concentrated HF immersion etch test.](image)

30
Chromium

A 4023Å layer of chromium was sputtered onto the surface of a silicon wafer with 5000Å of wet oxide growth. Subsequent HF etch proceeded at approximately 528Å/min (Figure 18). Surface attack can be described as pinholing and is shown in Figures 19-22. Both the chromium and underlying silicon dioxide film are being etched in the figures. No loss of adhesion was found on either a silicon or silicon dioxide substrate.

Figure 18: Cr film thickness vs. time for concentrated HF immersion etch test.
Figure 19: The chromium-coated wafer subsequent to 6 minute etch.

Figure 20: Chromium film surface after 2 minutes of hydrofluoric acid attack.
Figure 21: Chromium film surface after 4 minutes of hydrofluoric acid attack.

Figure 22: Chromium film surface after 6 minutes of hydrofluoric acid attack.
Copper

A thin 5000Å layer of copper was applied to the surface of a silicon wafer with 5000Å of wet oxide growth via DC sputtering. The wafer was subjected to a 49% HF etch for over ten minutes and no change in film thickness was detected. The surface of the film was completely unattacked, but partial delamination at the film/substrate interface did occur. Extended testing with copper proved that copper is relatively inert in HF. With agitation over a several hour period, the copper film delaminated intact. The copper foil still showed no signs of surface attack, however, when observed under microscope.

Molybdenum

A thin 5912Å layer of molybdenum was applied to the surface of a silicon wafer with 5000Å of wet oxide growth via DC sputtering. The wafer was subjected to a 49% HF etch for 15 minutes. The resulting Mo etch rate was approximately 19Å/min. The Mo film did not delaminate, but signs of HF penetration were discovered after about 10 minutes as shown in Figure 24. No delamination of the Mo film occurred for silicon or silicon dioxide coated silicon substrates even after extended tests lasting 90 minutes.

![Graph: Mo film thickness vs. time for concentrated HF immersion etch test.](image)

Figure 23: Mo film thickness vs. time for concentrated HF immersion etch test.
Figure 24: Molybdenum film surface after 15 minutes of hydrofluoric acid attack; some pinholes have formed.

Nickel

A thin 7348Å layer of nickel was applied to the surface of a silicon wafer with 5000Å of wet oxide growth via DC sputtering. Subsequent HF etch proceeded at approximately 2632Å/min (Figure 28). The film surface subsequent to etch exhibits both pinholing and cracking (Figures 26-28). Minor losses of adhesion occurred at the edge of the wafer with both silicon and silicon dioxide coated wafers.
Figure 25: Ni film thickness vs. time for concentrated HF immersion etch test.

Figure 26: The nickel-coated wafer subsequent to 30 seconds etch.
Figure 27: Nickel film surface after 30 seconds of hydrofluoric acid attack; pinholes have formed.

Figure 28: Nickel film surface after 30 seconds of hydrofluoric acid attack; cracks have formed near the edge of the wafer.
Photoresist

Shipley SC1827 positive photoresist was applied to a wafer and spun at 5000 rpm, 2500 r/min to yield a 27,000Å film. The photoresist was then set on a 115°C hot plate and soft-baked for 115 seconds. A small amount of acetone was applied to the end of a cotton swab and was used to remove photoresist from a small area of the wafer surface. The wafer was finally inserted into a 120°C oven for 30 minutes to hard-bake the polymer. This removal of photoresist by the cotton swab provided a step profile such that subsequent photoresist HF etch could be detected with profilometry.

To test the HF resistance of the film, the wafer was dipped in concentrated 49% HF solution for 30 minutes. The wafer was removed once every minute and the step height recorded (i.e., the photoresist thickness). Even after an hour, neither delamination nor a significant change in photoresist thickness had occurred.

The same photoresist application process was then applied to a silicon bare with 5000Å of wet oxide growth. After a few minutes of 49% HF immersion, the photoresist began to delaminate in small flakes across the entire wafer surface. This shows the HF was penetrating the photoresist and etching the underlying silicon dioxide. An accurate etch rate could not be recorded.

Platinum

A thin 5000Å layer of platinum was applied to the surface of a silicon wafer with 6000Å of wet oxide growth via DC sputtering. The wafer was subjected to a 49% HF etch for over ten minutes without any detectable change in film thickness. Etch rate testing was halted due to gross macro-scale penetration of the film surface as shown in Figures 29-31. Little delamination occurred with either silicon or silicon dioxide coated wafers, despite significant cracking. It is believed an adhesion layer may help to alleviate this effect.

38
Figure 29: The platinum-coated wafer subsequent to etch 10 minute etch.

Figure 30: Platinum film surface after 10 minutes of hydrofluoric acid attack. Circular crack-like features have formed.
Figure 31: Platinum film surface after 10 minutes of hydrofluoric acid attack. Cracks in the film are easily seen here at the edge of the wafer.

Silicon Nitride

A 1200Å layer of silicon nitride was deposited on a silicon wafer with 5000Å of wet oxide growth utilizing a low temperature Plasma Enhanced Chemical Vapor Deposition (PECVD) process. The wafer was subsequently etching with 49% HF. Within 30 seconds, nearly 800Å of silicon nitride was removed from the wafer surface (see Figures 32-34). The film was found to adhere well to both silicon and silicon dioxide for the short time the nitride survived the HF etch.
Figure 32: Si₃N₄ film thickness vs. time for concentrated HF immersion etch test.

Note that the etch rate was not uniform across the wafer surface as depicted in Figure 33, but was found to etch at a rate of approximately 1566 Å/min.

Figure 33: The silicon nitride-coated wafer subsequent to 30 seconds HF etch.
Figure 34: Silicon nitride film surface after 30 seconds of hydrofluoric acid attack. The film uniformity subsequent to etch is poor and has a standard deviation of over 200Å.

Silver

A thin 5000Å layer of silver was applied to the surface of a silicon wafer with 5000Å of wet oxide growth via DC sputtering. The wafer was subjected to a 40% HF etch for over ten minutes and no change in film thickness was detected. Surface attack did occur in the form of delamination at the film/substrate interface (Figure 35) and across the wafer surface in the form of circular surface features (Figure 36). These circular features can be attributed to pinholes in the silver film surface which cause underlying silicon dioxide etch.
Figure 35: The silver-coated wafer subsequent to 10 minute HF etch.

Figure 36: Silver film surface after 10 minutes of hydrofluoric acid attack. Large areas which have partially delaminated from the substrate are visible.
Tantalum

A thin 662Å layer of tantalum was applied to the surface of a silicon wafer with 5000Å of wet oxide growth via DC sputtering. The wafer was subjected to a 49% HF etch for six minutes and had an etch rate of approximately 88 Å/min (see Figure 37).

![Figure 37: Ta film thickness vs. time for concentrated HF immersion etch test.](image)

The attack at the interface between the Ta film and the silicon wafer was substantial, leaving only a small central section of the wafer with intact Ta film at the end of the etch (see Figures 38 and 39).
Figure 38: Tantalum wafer subsequent to 6 minute etch. The Ta film has been etched at the interface, leaving a small circle of film behind.

Figure 39: Tantalum film surface after 6 minutes of hydrofluoric acid attack. Here the edge of the remaining Ta film is shown.
Tungsten

A thin 470Å layer of tungsten was applied to the surface of a silicon wafer with 5000Å of wet oxide growth via DC sputtering. The wafer was subjected to a 49% HF etch for fifteen minutes and had an etch rate of approximately 8Å/min (see Figure 40). The W film exhibited great adhesion with both silicon and silicon dioxide (most similar to Mo in this respect).

![Graph showing W film thickness vs. time for concentrated HF immersion etch test.](image)

**Figure 40.** W film thickness vs. time for concentrated HF immersion etch test.

The amount of visual surface attack of the W film was minimal (see Figure 41).

46
Figure 41: Tungsten wafer subsequent to 15 minute etch. Pinholes have formed, but the film is free of cracks and signs of delamination.

Figure 42: Tungsten film surface after 5 minutes of hydrofluoric acid attack. Here pinholes have formed.
Figure 43: Tungsten film surface after 15 minutes of hydrofluoric acid attack; pinholes are abundant.

5.3 Concentrated HF Barrier Performance

Each of the protective thin film in the previous section were tested as a HF barrier as described previously. The film are 5000Å thick, with the exception of photore sist which is 27,000Å thick. All of these films, including silicon nitride, have a 1000Å SiO2 underlying dielectric layer to provide for electrical isolation from the Ti film. The results of these experiments are presented here.
Figure 44: Continuous resistance measurement vs. time for Ti test structure protected by photosist during 49% HF immersion.

Figure 45: Continuous resistance measurement vs. time for Ti test structure protected by silicon nitride during 49% HF immersion.
Figure 46: Continuous resistance measurement vs. time for Ti test structure protected by aluminum during 49% HF immersion.

Figure 47: Continuous resistance measurement vs. time for Ti test structure protected by copper during 49% HF immersion.
Figure 48: Continuous resistance measurement vs. time for Ti test structure protected by chromium during 49% HF immersion.

Figure 49: Continuous resistance measurement vs. time for Ti test structure protected by molybdenum during 49% HF immersion.
Figure 50: Continuous resistance measurement vs. time for Ti test structure protected by platinum during 49% HF immersion.

Figure 51: Continuous resistance measurement vs. time for Ti test structure protected by silver during 49% HF immersion.
Figure 52: Continuous resistance measurement vs. time for Ti test structure protected by tungsten during 49% HF immersion.

5.4 Protection For Underlying Microelectronics Application

In previous HF barrier test the Mo film performed best, lasting more than ten minutes longer to reach a resistance of 5000Ω than its closest competitor (Pt). For this reason, Molybdenum was selected to be used as a protective material for underlying microelectronic metallization.

The titanium test pattern coated with silicon nitride was fabricated as described in the Analytical Techniques and Experimental Methods chapter. The pads still covered, 5000Å of Mo was sputtered onto the wafer. To etch the Mo film, a solution of the chemical composition 1H2SO4, 1HNO3, 5H2O was used. This solution is reported to etch Mo at a rate of about 12 μm/minute at 25°C, but was found to etch more slowly, requiring 0.1 minutes to etch through the 5000Å of Mo. Note other Mo etch chemistries could have also been used: [11g K3Fe(CN)6, 10 g KOH, 150H2O] or [5H3PO4, 2HNO3, 4CH3COOH, 150 H2O] or [5H3PO4, 3HNO3, 2 H2O].

The wafer was half-submerged in HF for thirty-second intervals until a discontinuity
between the pads was recorded. A summary of the findings are shown in Table 8.

<table>
<thead>
<tr>
<th>Test Structure</th>
<th>Time to Discontinuity (mins)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>13</td>
</tr>
<tr>
<td>2.10μm</td>
<td>15</td>
</tr>
<tr>
<td>2.25μm</td>
<td>19.5</td>
</tr>
<tr>
<td>2.50μm</td>
<td>17</td>
</tr>
</tbody>
</table>

Table 8: Test structure vs. time to discontinuity (mins).
CHAPTER VI

CONCLUSIONS

The goal of the project was to evaluate the ability of various thin films to withstand long etches in hydrofluoric acid. To this effect, the adhesion to silicon and silicon dioxide-coated substrates were studied and etch rates of the films in concentrated HF were recorded. These findings are summarized in Table 9 and Figure 53.

![Etch Rate Graph]

Figure 53: Etch rate is concentrated HF vs. protective thin film. Silicon nitride is excluded, but has an etch rate of 1569 Å/min. The exact etch rates of photore sist, platinum, copper, and silver could not be determined.

The next part of the project examined the ability of each thin film studied earlier to act as a barrier to hydrofluoric acid. A ‘failure’ is defined here to mean an electrical resistance of more than 5kΩ. A summary of these results is shown in Figure 54.

The general trend of the data shows that materials which were found to be etched by pitting/pinholing also showed generally better protection performance against HF. A notable except is platinum, which was shown to crack subsequent to prolonged HF immersion.

55
<table>
<thead>
<tr>
<th>Film</th>
<th>Silicon</th>
<th>Silicon Dioxide</th>
</tr>
</thead>
<tbody>
<tr>
<td>Aluminum</td>
<td>n/a</td>
<td>n/a</td>
</tr>
<tr>
<td>Chromium</td>
<td>n/a</td>
<td>n/a</td>
</tr>
<tr>
<td>Copper</td>
<td>10 minutes</td>
<td>8 minutes</td>
</tr>
<tr>
<td>Molybdenum</td>
<td>n/a</td>
<td>n/a</td>
</tr>
<tr>
<td>Nickel</td>
<td>4 minutes</td>
<td>4 minutes</td>
</tr>
<tr>
<td>Photore sist</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>Platinum</td>
<td>4 minutes</td>
<td>3 minutes</td>
</tr>
<tr>
<td>Silicon Nitride</td>
<td>n/a</td>
<td>n/a</td>
</tr>
<tr>
<td>Silver</td>
<td>3 minutes</td>
<td>2 minutes</td>
</tr>
<tr>
<td>Tantalum</td>
<td>n/a</td>
<td>n/a</td>
</tr>
<tr>
<td>Titanium</td>
<td>n/a</td>
<td>n/a</td>
</tr>
<tr>
<td>Tungsten</td>
<td>n/a</td>
<td>n/a</td>
</tr>
</tbody>
</table>

Table 9: Time to first sign of adhesion loss of selected films to silicon and silicon dioxide when exposed to hydrofluoric acid.

The film provided good protection in the barrier test despite its each mode. Platinum thin film when used for acid protection may benefit from adhesive under layers.

![Graph](image)

Figure 54: Time to failure vs. protective thin film.

In the final portion of the project, a layout was designed in Cadence to act as underlying ‘fragile’ microelectronics with a select thin film acting as a protective barrier to HF. This test structure was fabricated with a Mo protective film and empirical results were presented. A 5000Å thick film of Molybdenum proved to protect underlying titanium (which is etched
quickly in HF) for almost 15 minutes in concentrated 49% HF. It was found that the 10, 25, and 50 μm overlap of the protective material, with respect to the underlying titanium, did not play an important role as the time to discontinuity was actually longer for the 25 μm overlap structure than it was for the 50 μm overlap structure. This is due to the fact that the etchant was vertically penetrating the film before a lateral etch failure at the film-substrate interface could occur.

In the 13 minutes before the titanium test structures were destroyed by the etchant, 16-17 μm of sacrificial silicon dioxide could have been etched, sufficient in common MEMS release applications which require less than 5 microns of SiO2 underetch. This makes the Mo film a good candidate to serve as a protective layer during the MEMS release step in MEMS-first microelectronic/MEMS integrated processes and for other applications which require strong protective barriers against hydrofluoric acid.

6.1 Suggestions for Future Work

In this study, only the protection of underlying microelectronics from hydrofluoric acid was considered. Follow up work could include the removal of the protective film without damaging the underlying microelectronics (this would be etalization dependent). Also, contamination of microelectronics by the protective film may be an issue if the film is not removed completely. Adding an intermediary layer such as a thin silicon nitride film could act as a contamination barrier, if needed.
REFERENCES


58


[38] Corrosion of compact noble metals in various reagents under air access and at temperatures of 20 and 100°C. *Edelmetall-Taschenbuch*, Degussa, page 46, 1967.


