Sea of Leads Electrical-Optical Polymer Pillar Chip I/O Interconnections For Giga-scale Integration

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Sea of Leads Electrical-Optical Polymer Pillar Chip I/O Interconnections For Gigascale Integration

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Dedicated to

my parents, Saed and Suha,

and

my two brothers, Tariq and Basil,

for their endless support
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Summary

Wafer-level integrated electrical and optical chip input/output (I/O) interconnection technologies are developed. The terminology used to describe the interconnection technologies is Sea of Leads (SoL). Two distinct generations of SoL are developed and opportunities for a third generation are described. The need for SoL is driven by the long term performance and integration requirements of gigascale integration (GSI) as well as the expected high costs of packaging and testing of such chips. SoL offers electrical I/O interconnections that provide mechanical compliance in the x-y-z axes, high electrical performance, and ultra-high density. Similarly, the optical I/O interconnections developed exhibit high performance, robustness against mechanical offsets, and ultra-high density. The use of a single I/O interconnection lead to provide simultaneous electrical and optical interconnections, or a dual-mode I/O, is also developed. SoL fabrication technology also accommodates the fabrication of RF I/O interconnections based on near-field capacitive couplers and microfluidic micropipe I/O interconnections for heat removal. A critical requirement is that the fabrication of the various I/O interconnection technologies must be implemented in an integrated manner, meaning that all interconnection functions must be batch fabricated at the wafer-level with the lowest number of masking steps possible. In addition, the integrated I/O fabrication technology must be implemented using low-temperature materials and processes to be compatible with structures fabricated by semiconductor front-end and back-end processes as well as with optoelectronic devices. Finally, the integrated I/O interconnection technologies must also facilitate wafer-level testing and burn-in.
Chapter 1

Introduction and Previous Work

1.1 Introduction

Opportunities for gigascale integration (GSI) will be governed by a hierarchy of limits [1.1]. At these levels of integration, the most restrictive limits in this hierarchy will not be imposed by transistors performing computational functions but rather by interconnect networks performing communication functions [1.1-1.4]. A key interconnection level that will be severely challenged by GSI is the chip-to-module interconnection that integrates the chip into the system, as illustrated in Figure 1.1. A gigascale system-on-a-chip (SoC) demands the development of new and cost-effective integrated input/output (I/O) interconnect solutions that use high-performance integrated electrical, optical, and radio frequency (RF) approaches to meet all of the I/O requirements of the 45 nm to 22 nm International Technology Roadmap for Semiconductors (ITRS) technology nodes [1.5]. Meeting these challenges is essential for the semiconductor industry to transcend known limits on interconnects that would otherwise decelerate or halt the historical rate of progress toward GSI and beyond. In general, power, clock, and signal I/O functions will be met by the selective integration of fine pitch electrical, optical, and RF I/O interconnect technologies. These high-density integrated I/O interconnections will be especially important for novel 3D chip structures.
as well as for high current (>400 A) and high bandwidth (>40 Tbps) applications. To investigate the above issues, attention must be given to overcoming long-range and fundamental barriers in chip-to-module interconnects by advancing fine-pitch compliant electrical, optical, and RF interconnections and wafer-level testing and burn-in.

Figure 1.1: A schematic illustration of the chip-to-module interconnection level.

In traditional electronic systems, the role of I/O interconnections is to provide electrical and mechanical interconnections between the die and the module/board. Due to the performance limitations of electrical interconnects however, not only have optical interconnects replaced electrical interconnects for long distance communication, but optical interconnects are being developed for chip-to-chip communication [1.6-1.14]. Today, providing electrical/mechanical I/O interconnections is both difficult and complex [1.5, 1.15]; introducing the new requirement of optical I/O interconnection adds new constraints and introduces new problems. Some of the key attributes an integrated electrical and optical I/O interconnection technology must possess are the following: a relatively simple and low cost method of fabrication at the wafer level; high performance and high reliability; high tolerance to offsets that may be induced by either coefficient of
thermal expansion (CTE) mismatches between the chip and the module/board or misalignment due to assembly; compatibility with wafer-level testing and burn-in; and be implemented using low-temperature materials and processes to ensure process compatibility with structures fabricated by traditional semiconductor front-end and back-end processes.

The importance of developing a new I/O interconnection technology is not only necessary to facilitate the performance requirements of GSI chips but to also dramatically change the packaging and testing processes, which can be redundant and time consuming. Conventional chip manufacturing is divided into front-end, back-end, and tail-end processing. Front-end processing refers to the fabrication of transistors, while back-end processing refers to wafer metallization. Tail-end processing refers to the packaging of the individual die. Conventionally, the final back-end wafer-level process step is the fabrication of vias through a passivation layer to expose the underlying pads on the die. These pads provide the electrical interface between the die and the package. Each individual die, while still part of the wafer, then undergoes wafer-sort after which die singulation is performed. Next, the die are individually placed in temporary packages for burn-in. The dice that pass this test (the known good die (KGD)) are then individually packaged and retested for functionality. This final step concludes tail-end processing, and the packaged dice are finally ready for system assembly.

1.2 Compliant Electrical Chip I/O Interconnections

CTE mismatch between silicon (CTE ≈ 5 ppm/°C) dice and printed wiring boards (PWB) (CTE ≈ 17 ppm/°C) is a common cause of reliability failure in electronic
components. This is especially important for chip-to-module I/O interconnects because as area-array solder bumps replace surface-mount packages with perimeter leads [1.16, 1.17], the CTE mismatch between the chip and the PWB induces high stress on the solder balls that can cause them to fracture and thus fail. A common solution to this CTE mismatch problem is the use of underfill [1.16, 1.17]. However, underfill is time-consuming to process, does not allow easy chip rework, is expensive, and degrades the electrical performance of high-frequency signal interconnects [1.18, 1.19]. The need for underfill can be eliminated by augmenting the solder bumps with compliant leads. The compliant leads are fabricated between the die pads and their respective solder bumps. Compliant I/O interconnections are designed to compensate for the different thermo-mechanical behaviors of the chip and the PWB by providing stress absorbing interconnect structures that undergo strain during thermal cycling. Thus, as the pad on the PWB changes spatial location during thermal cycling, the compliant lead easily and elastically changes shape. A current area of ongoing research is the investigation of how to package chips with low-k interlayer dielectrics without inducing any damage as a result of the packaging process [1.5, 1.20, 1.21]. This is an area where compliant interconnects can provide very promising solutions. Unlike wire bonding, for example, the fabrication of most compliant interconnections does not require the application of a high force load on the chip. Instead, the compliant interconnections are defined by lithography, followed by other standard microfabrication techniques. In addition, the compliant interconnects help to mechanically decouple the die and the board by undergoing strain during thermal cycling. As a result, this minimizes the stress created at the die pads and the surrounding low-k interlayer dielectric during thermal cycling.
There are several compliant wafer-level I/O interconnection technologies, including off-surface curved leads (Figure 1.2) [1.22, 1.23], microspring-like structures (Figure 1.3) [1.24, 1.25], suspended pads that can move in all axes, or floating pads, (Figure 1.4) [1.26, 1.27], stress-engineered metals that curl off the surface (Figure 1.5) [1.28-1.30], helix-like interconnects (Figure 1.6) [1.31, 1.32], coil-like interconnects (Figure 1.7) [1.33], and off-surface three-dimensional beams [1.34]. These compliant interconnect technologies differ in their electrical and mechanical performances, size, cost, fabrication, and I/O density. Compliant interconnects have been used in surface-mount packages with peripheral I/O distribution, such as tape automated bonding (TAB) and quad flat packages. However, these package structures are neither wafer-level nor chip-scale (a chip-scale package is defined as a package whose area is no more than 1.2 times larger than that of the die). The compliance that can be attained from various lead shapes for surface-mount packages has been studied [1.35]. Thus, the above mentioned wafer-level compliant interconnect technologies extend the concept of mechanical compliance from surface-mount packages with peripheral I/O distribution to packages that are chip-scale, fabricated at the wafer-level, and have an area-array I/O distribution. Moreover, the compliance is intended to enable wafer-level testing and burn-in [1.36-1.38].
Figure 1.2: Schematic of the compliant WAVE I/O interconnection structure [1.22, 1.23].

Figure 1.3: FormFactor's compliant microspring-like interconnections [1.24, 1.25].
Figure 1.4: Schematic of floating, or compliant, pads [1.26, 1.27].

Figure 1.5: SEM micrograph of the compliant stress-engineered interconnect structures [1.28-1.30].
Figure 1.6: SEM micrograph of helix-like compliant I/O interconnections [1.31, 1.32].

Figure 1.7: SEM micrograph and schematic of coil-like compliant interconnects [1.33].
1.3 Patel's Compliant Wafer-Level Package

The first part of this thesis represents an extension of Patel's research [1.39-1.41]. Patel proposed a new chip I/O interconnection technology called Compliant Wafer-Level Package (CWLP). As the name implies, CWLP provides the capability to batch fabricate compliant electrical interconnections at the wafer level. The compliant interconnects are generally s-shaped and lay on a low-modulus polymer, as shown in Figure 1.8. The compliant leads are either Cu or Au plated and are typically 10 μm thick. Patel fabricated two prototype chips using the fabrication process shown in Figure 1.9. The first prototype chip contained 126 pairs of different lead shapes distributed across a 1 cm x 1 cm area. The second prototype chip contained approximately 1,000 (on a 325 μm area-array pitch) compliant leads of identical geometry distributed across a 1 cm x 1 cm area. A portion of the second prototype chip is shown in Figure 1.8. In both chips, the compliant leads were interconnected with short wires on the silicon surface to facilitate measurements. The electrical parasitics of the compliant leads (i.e., resistance, capacitance, and inductance) were experimentally measured and simulated using the 3D parameter extractor Raphael (published by Technology Modeling Associates). The simulated electrical parasitics were 20 mΩ, 0.005 pF, and 0.14 nH at 5 GHz for the lead geometry shown in Figure 1.8. Low frequency electrical measurements, in addition, were performed, and the results agreed well with the calculated values.
Figure 1.8: SEM micrographs of Patel's CWLP. The leads shown are approximately 55 μm wide and 250 μm long. The I/O density of the chip is approximately 1x10⁹/cm².
Figure 1.9: Schematic of Patel's CWLP fabrication process. (a) The fabrication promptly begins after the fabrication of vias in the chip's passivation layer to expose the die pads. (b) A compliant polymer is spin coated. (c) Vias are etched to expose the die pads. (d) The compliant leads are next electroplated on the wafer. (e) Finally, the bumps are plated on the tail end of the leads.

The mechanical flexibility of various lead shapes was characterized using two methods. In the first method, the leads were mechanically tested in the lateral direction using a microneedle attached to a manual probe station. The probe station, however, could not measure the applied lateral force, and thus, it was not possible to attain the force-displacement characteristics of the leads. Only the lateral displacement of the leads was measured. All the different leads on the first prototype chip were tested in this
manner. The maximum lateral displacement of each lead shape was recorded, and the lead geometry shown in Figure 1.8 provided the most displacement (approximately 50 μm). Beyond this displacement, the tested leads broke. The location of the fracture on the leads was a function of their shape.

In the second method of testing, the first prototype chip was flip-chip bonded on an FR4 board with a CTE of ~ 17 ppm/°C. The assembled system (chip with the prototype leads bonded on the FR4 board) was placed into a -55°C – 125°C air-to-air thermal cycling chamber. The dwell time at the two temperature extremes was 5 min, and the transition time between the two temperature extremes was 1 min. The same electrical interconnects on the Si surface that were used for the electrical testing were also used to determine the mechanical integrity of the leads during the reliability testing. Since the different lead shapes were each interconnected in pairs on the chip, the substrate layout provided electrical paths to the leads' bumps to monitor the change in resistance of each of the pair of leads. After every 100 thermal cycles, the electrical resistance of the different lead pairs was measured. A pair of leads was considered a failure if the change in resistance after the reliability testing was greater than 20% of the initial (pre-test) value. Based on the results of the first testing method, it was shown that many of the leads would quickly fail because they did not provide the needed lateral displacement under the described thermal cycling conditions. A minimum displacement of approximately 30 μm was needed from the leads to compensate for the CTE mismatch between the chip and board under the -55°C – 125°C temperature range. After performing the above test on several prototype chips, the lead shape shown in Figure 1.8 underwent 1500 thermal cycles, on average, before attaining a 20% change in electrical
resistance. This experiment demonstrated that underfill was not required for CWLP, which is one of the key advantages of this interconnection technology.

Patel also performed heat removal and cost analysis on the CWLP. Models describing the routing of board-level interconnects were also developed. In addition, preliminary experiments were conducted in fabricating short (~10 μm) embedded air-gaps within the polymer film that the leads are fabricated above, as shown in Figure 1.10. The function of the embedded air gap was to increase the compliance of the leads in the out-of-plane axis.

Figure 1.10: SEM micrograph of a CWLP with an embedded air gap.
1.4 Summary of Research Goals

To date, none of the above listed compliant wafer-level electrical I/O interconnection technologies have demonstrated the ability to integrate optical I/O interconnections, which is a key interconnection technology for GSI. As a result, the primary objective of this Ph.D. thesis is to fabricate and characterize integrated electrical and optical wafer-level chip I/O interconnections, as illustrated in Figure 1.11. The terminology used to describe all interconnection technologies developed in this thesis is Sea of Leads (SoL). A critical requirement of this research is that the fabrication of the high density and high performance electrical and optical I/O interconnection technologies must be implemented in an integrated manner. This means that all interconnect technologies must be batch fabricated at the wafer level with the lowest number of masking steps possible. In addition, the integrated electrical and optical I/O fabrication technologies must be implemented using low-temperature materials and processes such that structures fabricated by semiconductor front-end and back-end processes as well as optoelectronic devices are not damaged. Finally, the integrated I/O interconnection technologies must facilitate wafer-level testing and burn-in in order to fully realize the economic benefits of wafer-scale processing.

![Diagram of primary focus of research]

Figure 1.11: A schematic of the primary research focus of this Ph.D. thesis.
1.5 Organization of the Thesis

The organization of the research in this thesis is described in this section. Chapters 2, 3, and 4 describe results in the first generation of SoL, while Chapters 5, 6, and 7 describe results in the second generation of SoL. Finally, Chapter 8 is an extensive discussion of future prospects of SoL and opportunities for a third generation of SoL. Below is a summary of the research organization in bullet format.

1.5.1 First Generation SoL

- Chapter 2: This chapter describes the fabrication of SoL chip I/O interconnections. This work represents an extension of Patel's CWLP.
- Chapter 3: This chapter describes the mechanical and electrical measurements (and modeling) performed to analyze the performance of the compliant leads.
- Chapter 4: This chapter primarily describes the process integration of SoL I/O interconnections with an Intel chip. The objective of this chapter is to highlight the issues involved in reconciling the fabrication requirements of SoL with existing semiconductor front-end and back-end processes as well as standard industry chip assembly processes.
1.5.2 Second Generation SoL: Sea of Polymer Pillars

- Chapter 5: This chapter describes the various electrical and optical I/O interconnection configurations possible through the use of highly compliant polymer pillars. Opportunities for RF and thermal I/Os are also described. The fabrication details of all I/O interconnect technologies are also described in this chapter.

- Chapter 6: This chapter describes the lateral (in-plane) and transverse (out-of-plane) mechanical characteristics of the polymer pillars.

- Chapter 7: This chapter reports a set of optical measurements made to demonstrate the various polymer pillar optical interconnect configurations proposed in Chapter 5. In addition, the process integration and performance of an optical subsystem that uses the polymer pillars is described. The optical subsystem consists of polymer pillars fabricated on metal-semiconductor-metal (MSM) photodetectors.

1.5.3 Third Generation SoL

- Chapter 8: This chapter is an extensive discussion of future prospects of SoL and opportunities for a third generation of SoL, which can be described as off-surface and curved microphotonic interconnections.

1.6 Conclusion

The cost, performance, reliability, and size of a high performance system are a function of the chip I/O interconnections and associated packaging. To this end, it is
important to develop an integrated electrical and optical chip I/O interconnection technology that makes use of wafer-level batch fabrication and testing to enhance the above listed attributes. The goal of this Ph.D. thesis is primarily to conceive and fabricate integrated electrical and optical chip I/O interconnection technologies. All interconnect structures proposed in this thesis fall under the umbrella of Sea of Leads (SoL) chip I/O interconnection technology. Two generations of SoL are proposed, fabricated, and partially characterized. Opportunities for a third generation of SoL are also described.
Chapter 2

First Generation Sea of Leads Fabrication

This chapter describes the fabrication of the first generation of Sea of Leads (SoL) chip I/O interconnection technology. The fabrication processes described in this chapter represent an extension of the fabrication processes that Patel developed for his Compliant Wafer-Level Package (CWLP) [2.1]. A schematic and an SEM micrograph of a SoL chip are shown in Figure 2.1 and Figure 2.2, respectively. SoL is fabricated at the wafer level to extend the economic benefits of semiconductor front-end and back-end wafer-level batch fabrication to include chip I/O interconnects, packaging, and wafer-level testing and burn-in [2.1-2.4]. A representative fabrication process of SoL is illustrated in Figure 2.3. The leads can be fabricated with a polymeric backbone to enhance their compliance and facilitate wafer-level solder reflow. Moreover, the fabrication of partially slippery leads, or leads that partially adhere to the overcoat polymer, enables the compliant leads to move freely, as needed, during thermal cycling. The complete SoL fabrication process consists of four major process steps [2.2-2.4]. The four major process steps are the patterning of the sacrificial material [2.5-2.10], the fabrication of vias in the overcoat polymer, the fabrication of leads, and the fabrication of solder bumps on the tips of the leads. Each of the just mentioned four major process steps requires a single photolithographic step. The objective of this chapter is to describe the fabrication details.
of the first generation of SoL. The fabrication of the embedded air gaps, vias, partially slippery leads, and metallic leads with a polymer backbone are described in the first four sections, respectively, of this chapter. In addition, the fabrication of planar optical waveguides within a SoL chip is described in last section of this chapter.

![Figure 2.1: A cross-sectional schematic of a SoL chip. X-y-z axes mechanically flexible I/O interconnections (compliant leads) are batch fabricated across dices at the wafer level. In essence, SoL extends wafer-level batch processing of on-chip multilayer interconnect networks to include the chip I/O leads.](image)

2.1 Embedded Air Gap Fabrication

Once semiconductor front-end and back-end processes are complete and the die pads are exposed through the passivation layer (Figure 2.3a), SoL chip I/O interconnection fabrication immediately follows. The first process step in SoL fabrication is to deposit and pattern a sacrificial polymer that will later form the embedded air gaps.
The fabrication of these micro air-gap structures has been demonstrated through the use of the sacrificial polymers Unity400 and Unity200 (Promera, LLC.) that thermally decompose at 400°C and 200°C, respectively [2.5-2.10].

Figure 2.2: SEM micrographs showing compliant leads fabricated on a polymer film with embedded air gaps. The I/O density of this chip is approximately $3 \times 10^7$/cm$^2$.  

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Figure 2.3: SoL fabrication process: (a) wafer with front-end and back-end processes complete: the die pads are exposed, (b) the sacrificial polymer film is applied and patterned, (c) the overcoat polymer is deposited and encapsulates the sacrificial polymer layer, (d) the sacrificial material is thermally decomposed to form air gaps by placing the wafer in a furnace with appropriate temperature profile (<400 °C maximum temperature) [2.5-2.10], (e) vias are etched in the overcoat polymer to expose the die pads, (f) the compliant leads are electroplated after proper seed layer deposition and resist patterning, (g) the chip solder bumps are fabricated.
First, the Unity polymer is spin-coated on the wafer and placed on a hotplate for a soft bake. The thickness of the Unity polymer film (i.e., ultimately the height of the air gap) is controlled by both the weight fraction of the polymer in solution as well as the spin speed [2.5-2.10]. Next, a metal film is deposited on the polymer film to function as a hard mask during reactive ion etching (RIE). This metal film must exhibit high etch selectivity over the Unity polymer during RIE. Moreover, the metal film must be highly etch selective over the metal used for the die pads. This is important because once the sacrificial polymer has been patterned, the hard mask must be etched. If the etchant used to etch the hard mask also etches the exposed die pads, then the pads, and consequently the dice, will be permanently damaged. The hard mask used during RIE was a 0.2 μm thick Al film. In addition, all die pads were Cu. However, special exceptions to this fact are described in Chapter 4. Once the sacrificial material has been patterned into the desired shapes, the Al hard mask is etched. In order to preserve the adhesion between the patterned sacrificial polymer and the underlying surface, a wet etch is not used. Instead, the Al is removed through a dry etch (using the RIE). This process step concludes the patterning process of the sacrificial polymer. At this stage in the process, the wafer resembles the schematic shown in Figure 2.3b. Photodefinable sacrificial polymers may be used instead to simplify the patterning process.

An encapsulating polymer is next blanket coated onto the wafer (Figure 2.3c). It is desirable for the polymer to have a low tensile modulus to allow the compliant leads to deflect as needed during wafer-level testing and assembly. Following encapselation, the sacrificial polymer is thermally decomposed by placing the wafer in a horizontal tube furnace at the proper decomposition temperature and time duration (Figure 2.3d). For a
successful decomposition, the proper temperature conditions, including ramping rates, have to be selected. The use of incorrect temperature conditions either causes the sacrificial polymer to partially decompose or causes the overcoat polymer to collapse. When the decomposition is implemented correctly, the decomposition products diffuse through the overcoat material leaving a virtually residue-free hollow structure. The overcoat polymer, its permeability properties, and the decomposition conditions will determine if the resulting embedded air gaps are dome or flat shaped. The above described issues have been thoroughly investigated and characterized in [2.5-2.10]. A cross-sectional view of the flat and dome-shaped air gaps are shown in Figure 2-4. The decomposition is performed before the fabrication of the compliant leads in order to prevent stressing or distorting the leads, which may occur during the decomposition process.
Figure 2.4: SEM micrographs showing cross-sections of the highly compressible embedded air gaps (flat and dome-shaped) overcoated with polyimide, i.e., process step (d) in Figure 2.3. Air-gap thickness and width can be varied across a wide range of values [2.5-2.10].
2.2 Via Fabrication

The next set of process steps are implemented to fabricate vias in the overcoat polymer, as shown in Figure 2.3e. The purpose of the vias is to permit electrical contact to the underlying die pads through the overcoat polymer. The vias are etched in the encapsulating polymer using either RIE [2.1, 2.4, 2.11] or photodefinition [2.1, 2.4, 2.12-2.14]. Photodefinition is a process in which a pattern is transferred from a mask directly into a photosensitive polymer film by ultraviolet (UV) irradiation. Following polymer developing, the regions of the polymer film that were not UV treated dissolve away to leave behind the UV treated polymer regions (for negative tone polymers). No hard mask is needed for photodefinition.

Some of the important considerations in the fabrication of vias are the aspect ratio, sidewall angle, and sidewall surface roughness. It is important to fabricate the vias such that the final structures can attain high aspect ratio, positively sloped sidewall angles, and a rough sidewall surface. The ability to fabricate vias with relatively high aspect ratios is necessary to facilitate the fabrication of high density I/O interconnections. Positively sloped sidewall angles are desirable to minimize problems associated with poor (metal) step coverage [2.15]. Poor metal coverage on the sidewalls of the vias ultimately causes the leads to be mechanically weak at the via's neck. Finally, rough sidewall surface is desirable to enhance the adhesion between the deposited metal and the polymer film. The above discussion is not valid, however, when the vias are filled with a metal prior to the fabrication of the compliant leads, as shown in the schematic of Figure 2.5. Such a process would planarize the surface and mitigate most of the problems listed above.

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Figure 2.5: Schematic of a process to planarize the surface of the polymer after via fabrication. The planarization is accomplished by filling the via with a metal.

2.2.1 Via Aspect Ratio

When the vias are fabricated using photodefinition, via aspect ratio plays a key role in the process. The ability to resolve the pattern is a function of the via aspect ratio. For example, it is much easier to resolve a feature that is 50 μm tall and 500 μm wide (aspect ratio of 1/10) than a feature that is 500 μm tall and 50 μm wide (aspect ratio of 10/1). Figure 2.6 illustrates a set of vias that was fabricated through photodefinition using the polymer Avatrol 2000P. The use of similar polymers for the fabrication of vias using photodefinition has been demonstrated previously [2.12-2.14]. The vias shown in Figure 2.6 were fabricated as follows: first, the polymer was spin coated to a 20 μm thickness on a Si wafer with a silicon-nitride passivation. After a 20 min soft bake on a 100°C hotplate, the polymer was irradiated with a 365 nm UV light through a mask containing
circular features. For this polymer film thickness, the most successful vias were fabricated at an energy dosage of ~300 mJ. Higher energy dosage distorted the sidewall profile of the vias by yielding more negatively sloped sidewalls. Next, the Si wafer was placed in a 100°C nitrogen-purged oven for 20 min for a hard bake. Following the hard bake, the wafer was cooled down on an insulating surface for 3-5 min. Finally, the polymer was spray developed using the developer BioAct EC-7R. Following spray developing, the wafer was rinsed with isopropanol (IPA) and dried with a nitrogen gun. For best results, the wafer should be oriented 45° with respect to the spray developer stream. The vias shown in Figure 2.6 are approximately 55 µm wide and 20 µm tall. Thus, the aspect ratio is approximately 0.36. The SEM micrographs show almost perfect vertical sidewall angle. On the other hand, Figure 2.7 illustrates an SEM micrograph of a 30 µm wide and 20 µm tall via fabricated through photodefinition using the same polymer. Thus, the aspect ratio is approximately 0.67. The fabrication process was similar to the one described for the 55 µm wide vias. In this SEM micrograph, the via sidewall is clearly seen to have a little kink at the neck and exhibits a negative slope. The negative slope is expected from this polymer since it is a negative tone polymer. Changing the process conditions (exposure dosage) did not substantially improve the via geometry. It should be noted that the uniformity of the vias across the wafer for both sets of samples was poor. This is probably due to the simple spray developing setup used in the cleanroom: the width of the spray stream was not wide enough to provide uniform coverage across the wafer.
Figure 2.6: SEM micrograph of a set of vias fabricated using the photodefinable polymer Avatrel 2000P. The vias are approximately 55 μm wide and 20 μm tall. Thus, the aspect ratio is approximately 0.36.
Figure 2.7: SEM micrograph of a via fabricated using the photodefinable polymer Avatrel 2000P. The via is approximately 30 μm wide and 20 μm tall (0.67 aspect ratio).

The key point in this discussion is that it is difficult to use a single polymer material for the photodefinition of vias with a wide range of aspect ratios. The larger the aspect ratio, the more difficult it is to resolve the desired features. With RIE, however, as long as the hard mask can be patterned into the desired features, the exposed polymer film can be etched. As a result, plasma etching is more forgiving and tolerant to changes in via aspect ratio.

2.2.2 Via Sidewall Angle

Controlling via sidewall angle is potentially easier with a dry etch than a wet etch. Figure 2.6 and Figure 2.7 clearly demonstrate that the polymer Avatrel 2000P yields
either near right-angle or negatively sloped via sidewall angles (this point will become 
important again in Chapter 5, which describes the second generation of Sol: Sea of 
Polymer Pillars). While the polymer’s contrast curve can potentially be designed to yield 
the desired sidewall angle, plasma etching offers greater control of via sidewall angle. 
Figure 2.8 is a pair of SEM micrographs showing vias fabricated using RIE at relatively 
high pressure to induce undercutting and thus, sloped sidewalls. This dry etch as well as 
all other dry etches in this thesis were performed using a PlasmaTherm RIE. The 
parameters of the recipe used to etch these vias are 300 mtorr pressure, 300 W power, 45 
scm of O2, and 5 scm of CHF3. The vias have the same dimensions as the via shown in 
Figure 2.7, and thus, they have an aspect ratio of 0.67. The thickness of the Al hard mask 
was 0.2 μm. The reader should note that it is very important that a polymer cleaning 
process be completed before etching any samples in the PlasmaTherm RIE. The clean 
process is essential to minimize cross-contamination between different users. This will 
ultimately give better and repeatable etch results.

It is possible to fabricate vias with multi-angled sidewalls using RIE. Figure 2.9 is 
an SEM micrograph of a via where the initial pressure set point was decreased midway 
through the process to yield a via with a sidewall angle that is high at the via’s neck and 
low at the via’s knee. The initial pressure set point was 300 mtorr, and the final pressure 
set point was 200 mtorr. Such a via structure is significant because this sidewall profile 
enhances plating uniformity (i.e., increases thickness) at the via sidewalls (especially at 
the via’s neck) since electroplating is typically biased to surfaces that are parallel to the 
anode. As a result, the increase in plating uniformity potentially enhances the reliability 
of the leads. Figure 2.10 illustrates a set of SEM micrographs showing photodefined vias 

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after Cu electroplating. The SEM micrographs vividly illustrate the poor and unreliable sidewall plating in vias with vertical sidewall angles.

![SEM micrograph of Cu pad](image1)

**Figure 2.8:** Cross-sectional SEM micrographs of vias fabricated using a PlasmaTherm RIE at a pressure of 300 mtorr, a power of 300 W, and gas flow rates of 45 sccm O₂ and 5 sccm CHF₃.
Figure 2.9: SEM micrograph illustrating a via sidewall profile obtained as a result of a two-part RIE etch process. The initial pressure set point of 300 mtorr was decreased midway in the process to 200 mtorr to yield a via that attains higher sidewall angle at the via's neck and lower sidewall angle at the via's knee. The benefits of such a via structure include enhanced via sidewall plating as well as reduced undercutting at the via's knee, which can cause the polymer to delaminate and prevent seed layer continuity.

Figure 2.10: SEM micrograph of a set of photodefined vias and the subsequent electroplating of Cu into the vias. The SEM micrographs vividly illustrate the poor and unreliable sidewall plating.
2.2.3 Via Sidewall Roughness

Finally, when the photodefined vias and vias fabricated by RIE are compared, it is clear that the vias fabricated by RIE exhibit greater sidewall surface roughness. As a result, it is expected that the metal films to be deposited in the next set of process steps will adhere better to those vias due to their rough side-wall surface. Thus, when the two methods of fabricating vias using the polymer Avatrel 2000P are compared, it appears that the use of RIE yields vias with the most desirable geometrical attributes.

2.3 Fabrication of Partially Slippery Leads

Once vias have been fabricated, the next step is to fabricate the leads, as shown in Figure 2.3. Two possible lead structures can be fabricated. The first is a purely metallic lead, and the second is a metallic lead with a polymer backbone. The benefits of each will be discussed later. The attainable compliance from a lead is not only a function of the geometry of the lead [2.1], but is also a function of the adhesion of the lead to the overcoat polymer [2.2-2.4]. Thus, there is an opportunity to enhance the compliance of the leads by controlling their adhesion to the overcoat polymer.

The general fabrication sequence of the metallic leads is as follows: a seed layer is first deposited. The importance of the seed layer with respect to adhesion is described later. Next, a resist layer is spin coated on the wafer and patterned into the shapes of the leads, as shown in Figure 2.11. The resist acts as a mold during the plating process. Once the resist has been patterned, the leads are electroplated. The Au or Cu leads are plated to a typical thickness of 10 μm. The leads are then covered with a non-wettable surface to
prevent solder from alloying with their surface. This can be accomplished by either plating a Ni layer on the leads and then oxidizing it or depositing Ti or Cr on the leads.

Figure 2.11: Three-dimensional topology of a patterned NR9-8000 resist film.

2.3.1 Fabrication of Partially Slippery Leads: Method 1

The leads should be fabricated such that they are only anchored at and around the via. The remainder portion of the lead should be fabricated such that it is not adhered, or slippery, to the surface of the overcoat polymer. Two methods of fabricating partially slippery leads were developed and are shown in Figure 2.12. In method 1 of Figure 2.12, the adhesion of the leads to the overcoat polymer is controlled by seed layer selection. For strong adhesion, a Ti/Au/Ti (300 Å/0.2 μm/300 Å) seed layer is sputter deposited. The bottom Ti film increases the adhesion between the Au film and the overcoat polymer.
Figure 2.12: Sea of leads fabrication process when slippery leads are desired: (a) back-end-of-the-line processing is complete, (b) deposition and patterning of sacrificial material, (c) application of overcoat polymer, (d) sacrificial polymer is decomposed to form air gaps, and (e) via fabrication in overcoat polymer to expose die pads. The wafer at this stage in the process is ready for lead fabrication. Method 1: (1f) Au seed layer is deposited, (1g) Au leads are electroplated, (1h) Au seed layer is etched, and (1i) solder bumps are fabricated on the leads. Method 2: (2f) Ti/Cu/Ti seed layer is deposited, (2g) Au leads are electroplated, (2h) solder bumps are fabricated, and (2i) seed layer is selectively etched to release the leads from the polymer's surface.
while the top Ti film increases the adhesion of the resist to the Au film, which is essential during the electropolishing of the leads. For poor adhesion to the underlying overcoat polymer (slippery leads), Au/Ti (no bottom Ti film) can be sputter deposited on the wafer. Figure 2.13 is a micrograph illustrating how easily the leads fabricated on such a seed layer move. However, this process yields leads that are very poorly adhered, which makes subsequent processing and alignment very difficult.

![7µm Displacement](Image)

Figure 2.13: Micrograph illustrating slippery leads. The lead on the left is shown to have moved by approximately 70 µm after the application of a lateral force. This pair of slippery leads was fabricated using Method 1 of Figure 2.12 (Au/Ti seed layer was used). The I/O density of this chip is approximately 1x10^3/cm².

As described above, it is desirable to fabricate the leads such that they are only anchored at the via end. This was demonstrated with the following process: a Ti film (300 Å) was first deposited and patterned such that Ti islands remained and covered the portions of the lead near the via. Next, a Au/Ti (6.2 µm/300 Å) seed layer was sputter deposited above the Ti islands. A relatively thick (12 µm) film of the negative tone resist NR9-8000 (Futurrex, Inc.) was next spin coated on the wafer. The process conditions of

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the resist are the following: the resist is spin coated for 40 s at 2000 rpm with an acceleration of 500 rpm/s. The wafer is next placed on a 100°C hotplate for 15 min for a soft bake. Next, the resist is UV irradiated through a mask containing the lead shapes. The total energy dosage for this thickness of resist is 250 mJ. The wafer is next placed on a 100°C hotplate for 2 min for a hard bake. Following the hard bake, the wafer is placed on an insulating surface for a slow cool down. Next, the wafer is placed in a dish containing the developer RD-6 (Futurrex, Inc.) and is agitated, by gently shaking the dish, for approximately 90 s. Following a DI water rinse and drying with a nitrogen gun, the wafer is placed in a PlasmaTherm RIE for 30 s in an O₂ plasma for a descum.

Following the application and patterning of the resist layer, the exposed regions of the Ti layer were etched using buffered oxide etchant (BOE). With little agitation, the etch time is approximately 20 s. The leads were next plated at a current density of ~2 A/dm² for 90 min using a Au cyanide plating solution [2,16]. Following the plating process, the wafer was rinsed with DI water. Acetone was used next to remove the resist film. Finally, BOE and KI based solution were used to etch the top Ti and Au layers, respectively. Since the Au seed layer has poor adhesion to the overcoat polymer, so do the plated leads. Thus, this fabrication method allows each lead to be anchored at the die pad end while the remainder of the lead is free to move, as needed, during thermal cycling. Instead of Ti, electroless Ni can be deposited on the Cu die pads to enhance adhesion between the Au seed layer and the Cu die pads. The Ni would also function as a diffusion barrier.

The quickest method of testing the adhesion of the leads to the underlying surface is with a peel test. Once the leads have been fabricated and the seed layer has been
etched, a piece of tape is rubbed onto the surface of the wafer with the fabricated leads. Next, the tape is peeled off the wafer. The wafer and the tape are then visually examined under an optical microscope for evidence of lead delamination. When this test method was applied on a wafer with leads electroplated on a Ti/Au/Ti seed layer, none of the leads peeled off. However, when the leads were electroplated on a Au/Ti seed layer, almost all the leads peeled off. The leads that peeled off were fully intact (no segment of the individual leads remained on the wafer). However, when the leads were electroplated above a Au film that was above the Ti islands, a smaller portion of the leads peeled off. Few of the leads that peeled off were fully intact. However, most of the leads that peeled off were the segments that were not adhered to the polymer film: the segments of the individual leads above the Ti islands remained attached to the wafer. These results demonstrate that the above described processes can control the adhesion of the leads to the underlying surface.

2.3.2 Fabrication of Partially Slippery Leads: Method 2

The second method (Method 2 in Figure 2.12) of fabricating the partially slippery leads is to plate the Au leads on a seed layer that is selectively etched once the leads are ready to be released from the surface. This fabrication method was demonstrated by plating Au leads on a Ti/Cu/Ti (300 Å/0.2 μm/300 Å) seed layer. The exact same photolithography and electroplating conditions described under the first method were used for this method. Following the fabrication of the leads, the Cu seed layer was first selectively etched using a 29% dilute nitric acid solution. Next, the bottom Ti adhesion layer was etched using BOE. It is important for the success of this fabrication method that
either the via side of the lead be much larger than the underlying via or a mask is placed around the via end of the lead to prevent the undercutting of the seed layer between the Au lead and the die pad.

A warning about the electroplating process to the reader; it is very important to rinse the wafer thoroughly with DI water (without drying) before placing it in the plating solution. This is important to ensure good surface wettability. If the surface is dry, bubbles will likely form in the resist openings once the wafer is placed in the plating solution. Such bubble formation prevents electro deposition. While not necessary, the plating can take place in an ultrasonic bath to remove the bubbles that form. Overuse of ultrasonic pulse during plating, however, will cause the photoresist to peel off during the plating process. More importantly, however, the wafer should be thoroughly rinsed with DI water to thoroughly remove any acids from the surface of the wafer. This is important from a safety perspective: mixing acid with a cyanide Au plating solution releases cyanide gas into the environment, which can be fatal if inhaled. In fact, any surface or object (beaker, anode, tweezers, gloves, etc.) that makes contact with the plating solution should be thoroughly rinsed with DI water.

The previously shown SEM micrographs were of SoL chips with an I/O density equal to approximately $1 \times 10^3$/cm$^2$ and $3 \times 10^3$/cm$^2$. However, these processes can be extended to higher I/O density. Figure 2.14 and Figure 2.15 are SEM micrographs of a SoL chip with $12 \times 10^3$ leads/cm$^2$. The leads are Au plated and are fabricated on a Ti/Au/Ti seed layer.

Finally, the last process step is to fabricate solder bumps on the tips of the compliant leads. The process steps required to fabricate the solder bumps are similar to
those required to fabricate the leads. Following the deposition of the seed layer, a resist layer is spin coated and patterned into the shapes of the solder bumps. The same photoresist recipe used during the fabrication of the leads can be used. Although, a thicker resist layer may be desirable (this depends on the desired thickness and volume of the solder). The plating solution used to fabricate the bumps was a commercially available plating solution from Shipley-Ronal. Since then, a new plating solution (60/40 SnPb) from Technic, Inc. has been used successfully. Figure 2.16 is an SEM micrograph of electroplated solder bumps (60/40 SnPb) on an 80 μm pitch. Since the leads are Au plated, it is very important to protect the Au surface from solder since solder dissolves Au. While it was previously stated that a non-wettable layer can be directly fabricated on the surface of the leads, details of such a process are described in Chapter 4.

Figure 2.14: SEM micrograph of one quadrant (~3x10^6 leads) of a SoL chip with 12x10^6 leads per cm^2.
Figure 2.15: SEM micrograph of a portion of a SoL chip with $12 \times 10^3$ compliant I/O interconnects per cm².

Figure 2.16: SEM micrograph of a set of high-density solder bumps fabricated on a wafer ($12 \times 10^3$/cm²). The bumps are electroplated 60/40 Sn/Pb. The pitch of the bumps is 80 µm.
2.4 Fabrication of Metallic Leads with Polymer Backbone

An alternative to purely metallic leads is metallic leads with a polymer backbone [2,4]. The polymer backbone provides a convenient non-wettable solder surface. In addition, such leads have lower stiffness and provide higher compliance than purely metallic leads of the same thickness. This point deserves further discussion. The Young's modulus of Au (~80 GPa) is approximately 160 times greater than that of the Avatrel 2000P polymer (~0.5 GPa). As the thickness of a metallic lead increases, the lead becomes stiffer and thus less mechanically compliant. As a result, it becomes desirable to have thin metallic leads that provide higher compliance. However, it is highly unlikely that a SoL chip with 1 µm or 2 µm thick leads would be very reliable. The leads would be very susceptible to any shear stress. As a result, it becomes important to provide the thin and highly compliant leads with higher mechanical stability. High mechanical stability was attained in Patel's CWLP by fabricating thick leads [2,1]. Patel used approximately 10 µm thick Au leads. However, a 2 µm thick Au lead is expected to provide higher compliance than a 10 µm thick Au lead. As a result, the tradeoff here is compliance versus mechanical integrity and reliability. However, by using a polymer backbone to enhance the mechanical integrity of the thin leads, no such tradeoff is foreseen. This is because the metallic film with the two orders of magnitude higher modulus will dictate the mechanical behavior of the composite lead.

The fabrication process of this type of lead is illustrated in Figure 2.17. Following via fabrication, a relatively thick metal film (1-3 µm) is deposited on the wafer (Figure
2.17(b)). Next, a polymer film is spin coated on the wafer (Figure 2.17(c)) and patterned into the shapes of the leads (Figure 2.17(d)). The bump side of the lead in this case has a via though the polymer film to allow electrical interconnection to the underlying metal film. The polymer may be patterned using either RIE or photodefinition. Both methods have been demonstrated. For this experiment, the polymer Avatrel 2000P was used. The polymer film was spin coated to a thickness of 12 μm. The spin cycle required for this thickness is 5000 rpm for 40 s with an acceleration of 1000 rpm/s. Following a 20 min soft bake on a 100°C hotplate, the polymer was flood exposed with a 365 nm wavelength light. This, according to the polymer's manufacturer (Promerus, LLC), enhances the mechanical performance of the polymer. The energy dosage used was 1000 mJ. Next, a 0.2 μm thick Al film was deposited on the polymer film using a Unifilm de sputter. The Al layer functions as a hard mask for the subsequent RIE. Using photolithography, the Al layer was patterned into the shapes of the leads (which should contain the via at the bump side). Next, a PlasmaTherm RIE was used to etch the polymer using process conditions similar to those described earlier. Figure 2.18 illustrates a set of metallic leads with the patterned polymer backbone. The polymer on the metallic lead is 12 μm thick. Figure 2.19 is an SEM micrograph of a metallic lead with a polymer backbone and with a via at its bump side. While it is ideal to simultaneously pattern the lead and the via at its tip, such a mask was not available at the time of the experiments. Thus, the leads and the vias were patterned using two masking steps. The fabrication processes used to fabricate vias at the tips of the leads are identical to those used to fabricate vias in the overcoat polymer. A single pressure set point was used during RIE. Following this process step, the underlying metal film can be used as a seed layer to electroplate solder bumps within
the vias located at the tips of the leads (Figure 2.17(e)). Following the fabrication of the bumps, the underlying metal film is etched to electrically isolate the leads. No resist pattern is used during the etch of the metal film because the polymer backbone acts as an etch mask. The adhesion at the polymer/metal interface is critical and can be enhanced.

![Diagram](image)

**Figure 2.17:** A schematic of the process used to fabricate leads with polymeric backbone. This process is carried out following the fabrication of the vias in the overcoat material that is shown in Figure 2.3c. For simplicity, air gaps are not drawn in the above figure. (a) Vias are fabricated, (b) a metal film (1-3 μm) is deposited on the overcoat polymer to yield either slippery or non-slippery leads, (c) a polymer film is deposited on the wafer, (d) the polymer is patterned into the shapes of the leads using either RIE or photodefinition, (e) under bump metallization and solder are plated at the vias located at the tip of the leads, (f) the metal film deposited in process step (b) is etched.
Figure 2.18: SEM micrographs of a set of metallic leads with a polymer backbone.
Figure 2.19: SEM micrograph of a lead with a polymer backbone and an etched via at the tip of the lead.

2.5 Planar Optical Waveguides Embedded Within a SoL Chip

Thus far, the discussion has been limited to the fabrication of electrical interconnections. Figure 2.20 is the micrograph of a SoL chip with embedded planar optical waveguides. There are approximately thirty 9 mm long polymer waveguides on the chip. The cladding of the polymer waveguides is an air gap [2.3, 2.17, 2.18]. The air cladding was fabricated using a thermally decomposable polymer [2.17]. The I/O density of the electrical compliant leads in Figure 2.20 is approximately 1x10^5/cm^2. The waveguides were fabricated within the SoL chip in the following manner: a polymer film,
was spin coated and patterned into 9 mm long channels to function as the waveguide core [2,17]. Next, a photosensitive thermally decomposable sacrificial polymer was spin coated and patterned into ~9 mm long channels above the core. The width of the channels was twice as wide as the core. From this point forward, the processing described previously follows, beginning with the spin coating of the overcoat polymer. This is because once the sacrificial polymer has been patterned, the wafer is essentially at the process step shown in Figure 2.3b. Figure 2.21 illustrates higher magnification micrographs of the embedded planar optical waveguides within the SOI chip. The fabrication of preferential-order focusing volume grating couplers on the polymer waveguides provides surface-normal optical coupling and thus, optical I/O interconnection [2.3, 2.17].

Figure 2.20: Die micrograph of a SOI chip with optical waveguides embedded within air gap channels.
Figure 2.21: Higher magnification micrographs showing the optical waveguides fabricated within an air-gap (cladding) in a SoL chip.

2.6 Conclusion

This chapter described the fabrication details of the first generation of Sea of Lords (SoL). SoL fabrication requires four major process steps. The first major process step is the fabrication of the embedded air gaps. The air gaps are formed by thermally decomposing a patterned sacrificial polymer that is overcoated with low modulus
polymer film [2.5-2.10]. The second major process step is the fabrication of vias in the overcoat polymer. The vias are fabricated either by a dry or a wet etch. Using the polymer Avatrel 2000P (Pramerus, LLC.), vias were fabricated using both processes. It was shown that the vias fabricated by a dry etch attained the most desirable attributes: positively sloped sidewall angles, rough sidewalls, and a fabrication method that is not dependent on via aspect ratio. The third major process step is the fabrication of the leads. Leads with and without a polymer backbone that are fully or partially adhered to the underlying overcoat polymer have been fabricated. The polymer backbone provides a convenient non-wettable solder surface. In addition, leads with a polymer backbone have a lower stiffness and provide higher compliance than purely metallic leads of the same thickness. Partially adhered, or slippery, leads can be fabricated by simply selecting/modifying the seed layer that is used to electroplate the leads. In general, the degree to which the leads adhere to the overcoat polymer is directly dependent on the adhesion of the seed layer to the underlying overcoat polymer. Slippery leads were shown to easily move in the lateral direction. The fourth major process step is the fabrication of the solder bumps. Apart from selecting the proper under bump metallisation (UBM) and the non-wettable surface on the leads, the fabrication of the bumps involves the use of commercially available and thus, standard solder plating solutions. Finally, the fabrication of planar optical polymer waveguides within a SoL chip has been demonstrated. Based on the above discussion, SoL chip I/O interconnections are less than 70 µm in thickness (thickness of air gaps, overcoat polymer, leads, and solder bumps) and weigh less than 100 mg/cm² providing an ultra-thin and lightweight chip I/O interconnection technology for hand-held as well as high-performance applications.
Chapter 3

Sea of Leads Mechanical and Electrical Measurements and Analysis

This chapter presents some mechanical and electrical measurements that demonstrate the performance of the first generation of Sea of Leads (SoL). The reported mechanical measurements describe the compliance of polymer films with and without embedded air gaps. In addition, the effects of an encapsulating metal film and metallic lead on the polymer film with embedded air gaps are reported.

An electrical analysis describing some of the limitations of distributing high dc current density is presented. In addition, some two-port microwave measurements are described. The measurements were made to gain insight into the high frequency performance of the compliant interconnections. While the analysis is not comprehensive, it does yield good initial insight into the high frequency performance of the compliant leads.

The chapter will begin, however, by describing a method of distributing different size and shape leads across a chip to increase its I/O density.
3.1 A Method of Increasing the I/O Density of a SoL Chip

The I/O density of a SoL chip is constrained by the amount of in-plane compliance (offset) required to compensate for the coefficient of thermal expansion (CTE) mismatch between the chip and the printed wiring board (PWB) [3.1, 3.2]. The higher the CTE mismatch, the larger the offset a lead must compensate for. In general, the length of a compliant lead increases as the value of mismatch increases. However, as the length of the leads increases, the I/O density of the chip decreases. Even if the die and the board are CTE matched, the leads cannot approach zero in size (i.e., just bumps) because they would provide no z-axis compliance. The CTE mismatch between the die and PWB may be expressed by

\[ \mu = \Delta T(\alpha_{\text{PWB}} - \alpha_{\text{chip}})x, \]

where \( \mu \) [in units of \( \mu m \)] is the maximum offset a lead must compensate for, \( \alpha \) [in units of ppm/°C] is the CTE of the component noted in subscript (PWB or chip), \( \Delta T \) [in units of °C] is the maximum change in temperature, and \( x \) [in units of \( \mu m \)] is the radial distance from the center of the die [3.3]. The three material and process dependent parameters of the above equation are \( \alpha_{\text{chip}}, \alpha_{\text{PWB}}, \) and \( \Delta T \). Because Si is the dominant semiconductor material for GSI [3.4], the die is assumed to be Si with a CTE of \(-3\) ppm/°C. In addition, because organic boards pose the highest CTE mismatch to Si dice, the board is assumed to be organic with a CTE of \(-16\) ppm/°C. The maximum temperature that both the die and PWB are exposed to is assumed to be 125°C, the highest temperature of a shock..
reliability test. Thus, relative to room temperature (25°C), \( \Delta T \) is assumed to be 100°C in this analysis.

Based on the above analysis, the I/O density of the SoC chip shown in Figure 3.1 was increased. The application of the above equation proceeds as follows: first, a 3 cm x 3 cm chip area was partitioned into three different regions, as shown in Figure 3.2. The choice of the chip area is based on the 35 nm technology node high-performance ITRS projections [3.5]. The exact dimensions of each of the three regions were somewhat arbitrarily selected. However, the dimensions of each of the regions were adjusted such that the final chip contained at least two different lead sizes to demonstrate a method of increasing the I/O density. The maximum displacement difference between the die and wafer in each region was calculated using the above equation, and the results are shown in Figure 3.2. For example, to calculate this value in region 3 of Figure 3.2, the following values were used: \( \Delta T = 100°C \), \( x = \frac{1}{2} \times 1.5 \text{ cm (diagonal distance from the center of the die to the corner of region 3)} \), and \( \alpha_{wib-wa} = 13 \text{ ppm/°C} \). Following an iterative process, two different lead lengths of approximately 60 \( \mu \text{m} \) and 110 \( \mu \text{m} \) were chosen, the former being distributed on an 80 \( \mu \text{m} \times 80 \mu \text{m} \) square I/O lattice at the inner region of the chip, and the latter being distributed on an 80 \( \mu \text{m} \times 160 \mu \text{m} \) rectangular I/O lattice at the edges of the chip, as shown in Figure 3.1. A schematic and an SEM micrograph illustrating the two different I/O distributions are shown in Figure 3.3 and Figure 3.4, respectively. The shape and size of the selected leads were based on the relatively simple models that were derived by Patel [3.6 (Chapter 6)]. The radius of curvature of the leads was the primary design parameter. It was shown in [3.6] that the radius of curvature is approximately proportional to the needed elongation and compression from the leads.

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Figure 3.1: SEM micrograph of one quadrant (~3x10^3 leads) of a SoL chip with 12x10^3 leads per cm^2. The chip contains short (~60 μm) leads distributed on an 80 μm x 80 μm square I/O lattice at the inner region of the chip and long (~120 μm) leads distributed on an 80 μm x 160 μm rectangular I/O lattice at the periphery of the chip. This distribution increased the I/O density.
Figure 3.2: Chip partitioning into three regions (R1, R2, R3). This will later allow the design of short (less compliant) leads in R1 and R2 and long (more compliant) leads in R3. As a result, the I/O density of the chip is increased. The approximate maximum displacement needed from the leads in each region is indicated in the figure. The numbers in the parentheses are the dimensions of each of the three regions before down scaling to a 1 cm x 1 cm chip area.

Figure 3.3: A schematic of the two different lead distributions in the SoL chip shown in Figure 3.1. The leads at the periphery of the chip (region 3 of Figure 3.2) were distributed on an 80 μm x 160 μm rectangular I/O lattice. The leads in regions 1 and 2 of Figure 3.2 were distributed on an 80 μm x 80 μm square I/O lattice.
Next, the three regions were scaled downward to fit into a 1 cm x 1 cm area in order to meet our (Georgia Tech’s) in-house reticle mask making capability. The final result is an area-array distribution of $10^6$ leads in the two inner regions (the first and second regions), and an area-array distribution of $2 \times 10^3$ leads at the edges of the chip (third region).

The leads in the chip under consideration were oriented approximately perpendicular to the contours of chip expansion for a higher degree of compliance, flexing outward during thermal cycling. Figure 3.5 is an SEM micrograph illustrating the approximate perpendicular orientation of the leads with respect to the chip’s contours of expansion at the chip’s neutral region (center).
3.2 Out-of-Plane Compliance Measurements

The design procedure for z-axis compliance in SoL differs from the design procedure for in-plane compliance [3.1, 3.2, 3.6]. This fact can be understood by noting, once again, that the motivation for each is different: in-plane compliance compensates for the CTE mismatch between the chip and the PWB while out-of-plane compliance provides the ability for two non-planar structures to make reliable electrical contact during wafer-level testing and burn-in as well as during assembly. Wafer-level testing and burn-in requires approximately 50 \( \mu \text{m} \) of z-axis deflection [3.7]. The leads can achieve high out-of-plane compliance as long as the material/structure under the leads is very compliant. In the following subsections, the results of a set of experiments that was conducted to demonstrate that polymer films with embedded air gaps provide greater
compliance than polymer films without embedded air gaps are described. In addition, the effects of fabricating a metallic structure on the polymer film with embedded air gaps are described.

3.2.1 Polymer Films and Embedded Air Gaps – No Metal

3.2.1.1 Blanket Polymer Film

A set of experiments was implemented to compare the attainable compliance of polymer films with and without embedded air gaps [3.1, 3.2]. The experimental setup used for the polymer films without embedded air gaps is described first. Two Si wafers were spin coated with two different thicknesses of the polymer Avatrel 2000P. The manufacturer specified tensile modulus of the polymer is ~0.5 GPa. After polymer cure, the thickness of the polymer films on the first and second wafers was 18 μm and 35 μm, respectively. The polymer was cured in a nitrogen-purged furnace for 2 hrs at 200°C. Using a Hysitron Tribolindenter equipped with a low-force head, the force-displacement characteristic curves of the two polymer films were measured. For this measurement, a 10 μm wide 60° conical tip was used. A trapezoidal force load function with a 10 s ramp to 8 mN, 30 s hold at 8 mN, and a 10 s downward ramp to zero force was used. The maximum recorded displacement (compression) of the 35 μm thick polymer film at 8 mN was approximately ~2.5 μm, as shown in Figure 3.6. A similar measurement was made on the wafer with the 18 μm thick polymer film, and the recorded maximum displacement at 8 mN was approximately 1.6 μm. Following visual inspection, no permanent indents on the polymer’s surface were observed for both samples indicating
that the polymers underwent primarily elastic deformation during the indentations. However, the unloading curve of the measurement shown in Figure 3.6 shows some plastic deformation (the unloading curve is nonlinear). Based on these measurements, if we restrict the elastic region to 10% strain for this polymer (1.6 μm displacement for 18 μm thick polymer film), then the polymer film must be 500 μm thick to provide 50 μm of displacement at 5 mN. A polymer film that thick would complicate fabrication, especially of vias, alignment, and probably increase the fabrication cost of Sol.

3.2.1.2 Polymer Film with Embedded Air Gaps

The second method of attaining z-axis compliance is by fabricating embedded air gaps within the polymer film as described in Chapter 2. To compare the two methods, a similar experiment was conducted where 30 μm tall air gaps with 5 μm thick polyimide overcoat (with an approximate modulus of 4.7 GPa) were fabricated on a wafer. One of the patterned air-gap geometries on the wafer was the 190 μm x 190 μm square shown in Figure 3.7a. The force-displacement characteristic curve of this structure at its center is shown in Figure 3.8. The measurement illustrates that the structure undergoes primarily elastic deformation since the unloading curve is both linear and returns to the origin. The structure was compressed by 30 μm at 55 mN. Thus, the compliance of this structure is the ratio of the displacement (limited to the elastic region) and the applied force, and is equal to 30 μm/55 mN = 0.55 μm/mN. At forces beyond 55 mN, the tip makes contact with the substrate (Si) causing the spike shown on the curve. The same air-gap structure after the indent is shown in Figure 3.7b. The image clearly illustrates that the overcoat polymer did not puncture following the indent. The black spot is the deformation of the
overcoat polymer once the indenter tip reached the substrate's surface. A similar indent was made on a rectangular-shaped air gap with dimensions of 9 mm x 190 μm. The force-displacement characteristic curve of this structure at its center is shown in Figure 3.9. The measurement, once again, illustrates elastic deformation. This air-gap structure attains a maximum displacement of 75 μm at 15 mN of force. Thus, the compliance of this structure is 2.33 μm/mN. The force-displacement ratio of this structure is much lower than that of the square-shaped air gap shown in Figure 3.8: both air-gap geometries attained approximately 30 μm of displacement at substantially different force values. This result indicates that air-gap geometry plays an important role in the design of out-of-plane compliance in SoL. In addition, air-gap thickness, overcoat polymer thickness, and the modulus of the overcoat polymer also influence the attainable z-axis compliance.

When the two different methods of attaining z-axis compliance are compared, it is clear that polymer films with embedded air gaps provide substantially higher compression and higher values of compliance than polymer films without embedded air gaps. At 8 mN, the polymer film with embedded air gaps yielded approximately 18 μm of displacement compared to the 2.8 μm displacement yielded by the 35 μm thick polymer film without embedded air gaps. However, since two different indenter tip sizes were used to measure the polymer films with and without the embedded air gap, it is difficult to exactly quantify the compliance differences between the two sets of measurements.
Figure 3.6: Force-displacement characteristic curve of a 35 μm thick Avatrel 2000P polymer film. For this measurement, a 10 μm wide indenter tip was used. In addition, a trapezoidal force load function was used.

(a)  
(b)

Figure 3.7: A 30 μm tall air gap embossed within a 5 μm thick overcoat polymer. (a) The air gap before the indent. (b) The same air gap after a 30 μm indentation.
Figure 3.8: Force-displacement characteristic curve of the air-gap structure shown in Figure 3.7a. The attained $z$-axis compliance is 30 μm at 55 mN. At forces higher than 55 mN, the overcoat membrane contacts the wafer's surface causing the spike. The thin overcoat polymer did not puncture following the measurement. For this measurement, a 20 μm wide indenter tip was used. In addition, a triangular force load function was used.
Figure 3.9: Force-displacement characteristic curve at the center of an embedded air gap with rectangular dimensions of 9 mm x 190 µm. This structure attained a lower force-displacement ratio than the structure shown in Figure 3.7a. For this measurement, a 20 µm wide indenter tip was used. In addition, a triangular force load function was used.
The key point in this section has been to experimentally verify that polymer films with embedded air gaps provide substantially higher compliance and undergo almost 100% air-gap thickness compression. Polymer films without embedded air gaps provide substantially smaller compression (less than 10%) and compliance. The above out-of-plane measurements were made on embedded air gaps without leads fabricated above them, and therefore, the measurements represent the intrinsic compliance of the embedded air gaps.

3.2.2 Embedded Air Gaps with a Metallic Layer on their Surface

3.2.2.1 Blanket Metal Films on the Embedded Air Gaps

The compliance of an embedded air gap with metal partially or fully covering the surface of the overcoat polymer is of prime interest. This is obvious because a metallic lead will ultimately be fabricated above the overcoat polymer, as was described in Chapter 2. In order to characterize the effects of a metallic film on the highly compliant embedded air gaps, Ti/Cu/Ti (300 Å/5 μm/300 Å) and Ti/Au (300 Å/5 μm) films were each sputter deposited on two Si wafers containing several air-gap geometries. A schematic of the embedded air gaps after the deposition of either metal layers is shown in Figure 3.10. For this set of measurements, a 50 μm radius conical tip was used. A summary of the forces required for various out-of-plane displacements for various air-gap geometries is show in Table 3.1. The table shows the results for both metalization layers. The air-gap structures with the Ti/Cu/Ti coating after indentation and their respective
force-displacement characteristic curves are shown in Figure 3.11 (ellipses), Figure 3.12 (circles), Figure 3.13 (squares), Figure 3.14 (short channels), and Figure 3.15 (long channels). As can be seen from the SEM micrograph, the overcoat polymer permanently deformed after the indents. This can be attributed to the stiff metallic layer. Because of this plastic deformation, when the structures were indented again, the force required to attain the same displacement was substantially higher.

**Figure 3.10:** Schematic of an embedded air gap with a metal coating. Such structures were indented at their center.
Table 3.1: Table summarizing the peak force-displacement values of a set of air gaps with different shapes when Ti/Cu/Ti (300 Å/5 μm/300 Å) and Ti/Au (300 Å/5 μm) films are sputter deposited on the overcoat polymer. Due to the plastic deformation of the metal film, the air gaps lose their compliance linearity, i.e., the force required to displace the embedded air gaps does not scale linearly with displacement. The numbers in the parentheses under the values of force are the actual measured displacements under the quoted force. All air gaps were approximately 50 μm tall. The dimensions of the various air gap geometries are shown in parentheses.

<table>
<thead>
<tr>
<th>Air-Gap Shape</th>
<th>Displacement</th>
<th>Ti/Cu/Ti (300 Å/5 μm/300 Å)</th>
<th>Ti/Au (300 Å/5 μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>μm</td>
<td>5 μm</td>
<td>15 μm</td>
</tr>
<tr>
<td>Ellipse (190 μm x 230 μm)</td>
<td>45.7 mN</td>
<td>84.7 mN</td>
<td>119.2 mN</td>
</tr>
<tr>
<td>Circle (190 μm diameter)</td>
<td>58.2 mN</td>
<td>91 mN</td>
<td>117.1 mN</td>
</tr>
<tr>
<td>Square (190 μm x 190 μm)</td>
<td>56.0 mN</td>
<td>90.4 mN</td>
<td>115.6 mN</td>
</tr>
<tr>
<td>Short Channel (190 μm x 590 μm)</td>
<td>49.1 mN</td>
<td>94.4 mN</td>
<td>148.2 mN</td>
</tr>
<tr>
<td>Long Channel (190 μm x 9 mm)</td>
<td>52.2 mN</td>
<td>96.9 mN</td>
<td>152 mN</td>
</tr>
</tbody>
</table>

As shown in Table 3.1 and Figure 3.16, the difference between the forces required to indent the Cu and Au coated embedded air gaps is significant. This is due to the fact...
that Au has a much lower Young's modulus (E). The Young's modulus is equal to the stress (σ) divided by the strain (ε) [3,8], or

\[ E = \frac{\sigma}{\varepsilon} \]

Under the same strain (same indent depth), the Young's modulus and the stress on the Au coated air gaps (E_{Au}, \sigma_{Au}) and the Cu coated air gaps (E_{Cu}, \sigma_{Cu}) can be related with

\[ \frac{\varepsilon_{Au}}{\varepsilon_{Cu}} \rightarrow \frac{\sigma_{Au}}{E_{Au}} = \frac{\sigma_{Cu}}{E_{Cu}} \rightarrow \frac{\sigma_{Cu}}{\sigma_{Au}} = \frac{E_{Cu}}{E_{Au}} \]

The resulting equation indicates that the ratio of the two stresses is equal to the ratio of the Young's modulus of the two metals. The Young's modulus of Cu and Au are approximately E_{Cu} = 120 GPa and E_{Au} = 79 GPa. As a result,

\[ \frac{\sigma_{Cu}}{\sigma_{Au}} = \frac{E_{Cu}}{E_{Au}} = \frac{120}{79} = 1.52 \]

From the measured results shown in Figure 3.16, the ratio of the applied forces (or stress) for the same air-gap geometries under elastic strain (linear portion of the loading curve) is almost equivalent to the calculated value of 1.52. The ratio of the applied force on the Cu and Au coated elliptical-shaped air gaps is approximately equal to 1.62.

The key point in this section is that metal degrades the mechanical characteristics of the embedded air gaps. Not only has the force-displacement ratio of the embedded air gaps decreased, but the metal films have caused the structures to undergo plastic deformation. This is expected since the deposited metal thickness is approximately equal to the thickness of the overcoat polymer, and thus, the metal film will dictate the overall mechanical characteristics of the structure.
Figure 3.11: Elliptical-shaped embedded air gaps after indentation and their force-displacement characteristic curves. From left to right, the embedded air gaps after being indented by 15 μm, 30 μm, 50 μm, and 5 μm.
Figure 3.12: Circular-shaped embedded air gaps after indentations and their force-displacement characteristic curves. From left to right, the embedded air gaps after being indented by 15 μm, 30 μm, 50 μm, and 5 μm.
Figure 3.13: Square-shaped embedded air gaps after indentation and their force-displacement characteristic curves. From right to left, the embedded air gaps after being indented by 15 μm, 30 μm, 50 μm, and 5 μm.
Figure 3.14: Short-channel shaped embedded air gaps after indentation and their force-displacement characteristic curves. From left to right, the embedded air gaps after being indented by 15 \mu m, 30 \mu m, 50 \mu m, and 5 \mu m.
Figure 3.15: Long-channel shaped embedded air gaps after indentation and their force-displacement characteristic curves. From left to right, the embedded air gaps after being indented by 15 µm, 30 µm, 50 µm, and 5 µm.
Figure 3.16: The force-displacement characteristic curves of an elliptical shaped air gap as a function of encapsulating metal. The plot shows the results for Ti/Cu/Ti (upper curve) and Ti/Au (lower curve) film coatings.

3.2.2.2 Au Leads on the Embedded Air Gaps

The final set of measurements was made on a set of embedded air gaps with compliant Au leads fabricated above them. Figure 3.17 is an SEM micrograph of the shape of the structures tested. The leads were 20 μm wide and Au plated to a thickness of 5 μm. The air gaps were 60 μm x 100 μm in size and 50 μm thick. Using a 20 μm conical diamond tip, the force-displacement characteristic curve of the structure was measured. The force was applied on the circular tip of the lead (the bump location). The forces required to yield 10 μm and 35 μm of compression are 22.9 mN and 50 mN, respectively.

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The lead, and consequently the air gap, demonstrated some plastic deformation after the measurements.

Figure 3.17: SEM micrograph of a Au lead (5 μm thick and 20 μm wide) fabricated on an embedded air gap. All indented embedded air gaps with metallic leads were of this shape.

3.3 Electrical Analysis and Measurements

Not only is it important for the compliant leads to exhibit high mechanical performance, but it is also important for them to exhibit high electrical performance. This section partially describes the electrical performance of the compliant leads.
3.3.1 DC Analysis

The dc resistance ($R_d$) of a lead is proportional to the length ($L$) of the lead divided by its cross-sectional area ($A$), i.e., $R_d = \rho L / A$, where $\rho$ is the resistivity of the metal. Figure 3.18 is a plot of the dc resistance as a function of the lead's length and cross-sectional area. The resistance is seen to vary from 1 m\(\Omega\) to 60 m\(\Omega\). A typical lead is 200 \(\mu\)m long and 30 \(\mu\)m x 10 \(\mu\)m in cross-section. Thus, the typical value of resistance is approximately 20 m\(\Omega\). In addition, because the leads are short, their self-inductance is less than 0.1 nH [3.6]. Low resistance is desirable to minimize power dissipation and heat generation in the leads. Low parasitics at dc are also important for chip power distribution.

Figure 3.18: The dc resistance of a compliant Au lead as a function of the lead's cross-sectional area and length.
The highly compressible air-cavities can also reduce the lead's electrical parasitics. The effective dielectric constant coupling the lead to the top most global wiring level can be reduced with the fabrication of the embedded air gaps. Considering the cross-sectional view of the lead-polymer-air gap structure shown in Figure 3.19 and using Gauss's law and electromagnetic boundary conditions across the two dielectric media (the overcoat polymer and the air gap), the effective capacitance coupling the lead to the top-most global wiring level (assuming a ground plane) can be approximated with

\[
\varepsilon_{\text{eff}} = \frac{\varepsilon_{\text{poly}} A_{\text{bottom}}}{\varepsilon_{\text{poly}} A_{\text{poly}} + \varepsilon_{\text{airgap}}}
\]

where \(A_{\text{bottom}}\) is the lead's in-plane surface area, \(t_{\text{poly}}\) and \(t_{\text{airgap}}\) are the thickness of the overcoat polymer and air-gap, respectively. \(\varepsilon_{\text{poly}}\) and \(\varepsilon_0\) are the polymer's dielectric constant and permittivity of free space, respectively. This equation clearly demonstrates that the capacitance decreases with increasing air-gap thickness.

Figure 3.19: A cross-sectional schematic of a lead above a polymer film with an embedded air gap.
3.3.2 DC Current Distribution

In this section, the number of die pads needed to deliver the ITRS projected values of current drain for high performance chips is estimated as a function of technology node. The current density per power/ground (pwr/gnd) die pad is equal to the current per pad divided by the area of the pad. Moreover, the aggregate current density of a chip is equal to the chip's current drain divided by one-half of the chip’s net surface area devoted to the pwr/gnd pads. If the net area occupied by 10 pwr/gnd pads is equal to the net area occupied by 1,000 pwr/gnd pads, then the current density per pad are equal. Figure 3.20 illustrates this principle schematically.

\[
I_2 = 0.25 I_1
\]

Current density = \( I_2/A_2 \)

\[ = (0.25 I_1)(0.25 A_1) \]

\[ = I_1/A_1 \]

Area = A_1

Area = A_2 = 0.25 A_1

Figure 3.20: A schematic illustrating that current density is a function of the aggregate current and pad area.

Electromigration is a function of current density. At a current density greater than \( 10^4 \) A/cm², electromigration in solder becomes problematic [3.9-3.11]. At such a high current density, voids begin to form in the region of the intermetallic compound (IMC) at

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the cathode side while hillocks begin to grow at the anode side. This ultimately leads to the formation of electrical opens and shorts and thus, failure of the chip.

A summary of the ITRS [3.12 (pp. 45-47), 3.13 (pp. 109)] projections is shown in Table 3.2. The projected total current drain ($I_{\text{total}}$) for high performance chips is projected to increase from 118 A at the 130 nm technology node to 720 A at the 22 nm technology node. The number of pwr/gnd pads ($n_{\text{pwr-gnd pads}}$) is projected to remain constant until the 65 nm technology node where it increases from 2048 to 2944 at the 22 nm technology node [3.12 (pp. 45)]. Thus, the number of pads increases by a factor of approximately 1.5. The current per pad ($I_{\text{pad}}$) can be calculated using

$$I_{\text{pad}} = \frac{I_{\text{total}}}{0.5n_{\text{pwr-gnd pads}}}.$$  

While $n_{\text{pwr-gnd pads}}$ is projected to increase, the pitch between the pads ($P_{\text{pitch}}$) is projected to decrease from 290 µm at the 130 nm technology node to 50 µm at the 22 nm technology node for area-array flip chip [3.13 (pp. 109)]. If the pads are assumed to be square in geometry and have a width ($P_{\text{width}}$) equal to half the pad pitch, then the total chip surface area allocated for the pwr/gnd pads ($A_{\text{pwr-gnd pads total}}$) can be calculated using

$$A_{\text{pwr-gnd pads total}} = n_{\text{pwr-gnd pads}} \left(\frac{0.5P_{\text{pitch}}}{2}\right)^2 = n_{\text{pwr-gnd pads}} \left(\frac{P_{\text{width}}}{2}\right)^2.$$  

The total pad area is projected to decreases from 20.49 mm² at the 130 nm technology node to 1.84 mm² at the 22 technology node. This immediately raises a red flag because while the total current drain is increasing, the net area allocated for the pwr/gnd pads is decreasing. As a result, the current density ($J$) is essentially sky rocketing. The current density is equal to

$$J = \frac{I_{\text{total}}}{0.5A_{\text{pwr-gnd pads total}}}.$$  

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The current density is seen in Table 3.2 to increase from $1.51 \times 10^3$ A/cm² (at the 130 nm node) to $7.8 \times 10^3$ A/cm² (at the 22 nm node). This is primarily due to the fact that the rate of increase of the number of pads is much slower than the rate of decrease of the pad pitch. The area of the pads decreases from 100 μm x 100 μm to 25 μm x 25 μm; the pad area decreases by a factor of 16. However, the number of pads only increases by a factor of 1.5. In addition, what matters worse is that the current drain of the chip is projected to increase by a factor of 6.

Table 3.2: Summary of the ITRS projections for high-performance chips.

<table>
<thead>
<tr>
<th>Year</th>
<th>2001</th>
<th>2002</th>
<th>2003</th>
<th>2004</th>
<th>2005</th>
<th>2006</th>
<th>2007</th>
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<td>90</td>
<td>80</td>
<td>70</td>
<td>60</td>
<td>50</td>
<td>40</td>
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<tr>
<td>Power (mW)</td>
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<td>186</td>
<td>100</td>
<td>60</td>
<td>37</td>
<td>27</td>
<td>20</td>
<td>17</td>
<td>13</td>
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<td>1.3</td>
<td>1.4</td>
<td>1.6</td>
<td>1.6</td>
<td>1.8</td>
<td>2.0</td>
<td>2.2</td>
<td>2.4</td>
</tr>
<tr>
<td>Current (A)</td>
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<td>108</td>
<td>100</td>
<td>90</td>
<td>80</td>
<td>70</td>
<td>60</td>
<td>50</td>
<td>40</td>
</tr>
<tr>
<td>ITRS Total number of Pads</td>
<td>30772</td>
<td>30772</td>
<td>30772</td>
<td>30772</td>
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<td>30772</td>
</tr>
<tr>
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<td>29488</td>
<td>29488</td>
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</tr>
<tr>
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<td>0.63</td>
<td>0.63</td>
<td>0.63</td>
<td>0.63</td>
<td>0.63</td>
<td>0.63</td>
</tr>
<tr>
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<td>0.58</td>
<td>0.58</td>
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<td>0.58</td>
<td>0.58</td>
<td>0.58</td>
<td>0.58</td>
</tr>
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<td>ITRS and J (A/cm²)</td>
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<td>0.008</td>
<td>0.008</td>
<td>0.008</td>
<td>0.008</td>
<td>0.008</td>
<td>0.008</td>
<td>0.008</td>
<td>0.008</td>
</tr>
<tr>
<td>Current (A/cm²)</td>
<td>0.008</td>
<td>0.008</td>
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<tr>
<td>Current (A/cm²)</td>
<td>0.008</td>
<td>0.008</td>
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Figure 3.21 plots $A_{\text{pervag}, \text{pad}}$ vs. $J$ versus technology node. It is evident in the figure that the $10^4$ A/cm² critical value will be met at approximately the 70 nm technology node. The ITRS states that it assumes that most of the pads will be distributed in an area-array pattern on the first few rows at the periphery of the chip. This is primarily to enhance the ability to route the I/O interconnections on the PWB and to minimize the number of interconnect layers on the PWB [3.13 (pp. 108, pp. 100), 3.14 (pp. 11 and pp. 14-18)] to minimize the costs of board fabrication.

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Now that the ITRS projections have been analyzed, the next step is to derive the optimum number of power/gnd pads and the total die surface area needed for the power/gnd pads to deliver the projected current drain. The first assumption is to limit the current density to $10^4$ A/cm². This is the critical current density value of solder at which electromigration becomes very problematic. Based on the projected current drain and the current density limit, the required area for the power/gnd pads ($A_{\text{power/gnd needed}}$) is

$$A_{\text{power/gnd needed}} = \frac{2I_{\text{max}}}{J}.$$  

This value is seen to increase in Table 3.3 from 2.36 mm² (at the 130 nm node) to 14.42 mm² (at the 22 nm node). With respect to on-chip IR drop constraints, the total power/gnd pad area needed were calculated [3.15, 3.16], and the values are shown in the table: they decrease from 7 mm² (at the 130 nm node) to 5.625 mm² (at the 22 nm node). As a result, the total area required for the power/gnd pads in each technology node is equal to the largest value calculated by the ITRS, values in [3.15, 3.16], and the area required to meet the current density limit. These values are plotted in Figure 3.22.
Figure 3.21: The ITRS projections for current density and total area of the pwr/gnd pads as a function of technology node.

Table 3.3: Summary of various parameters needed for high quality current distribution.

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<td></td>
<td></td>
</tr>
<tr>
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<td>160</td>
<td>180</td>
<td>200</td>
<td>220</td>
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<td>320</td>
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<td>0.5</td>
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<td>0.0</td>
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</tr>
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<td>190.50</td>
<td>240.69</td>
<td>290.89</td>
<td>340.06</td>
<td>390.20</td>
<td>440.33</td>
<td>490.46</td>
<td>540.59</td>
<td>590.72</td>
<td>640.85</td>
<td>690.98</td>
<td>741.11</td>
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<td>Total ITRS pwr/gnd pad area (mm²)</td>
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<td>40.33</td>
<td>45.02</td>
<td>50.59</td>
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<td>61.53</td>
<td>66.00</td>
<td>71.47</td>
<td>76.94</td>
<td>82.42</td>
<td>87.89</td>
<td>93.36</td>
<td>98.83</td>
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<td>(D) &amp; (P) pitch (mm)</td>
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<td>256</td>
<td>256</td>
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<tr>
<td>Max allowed Area (mm²)</td>
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<td>10000</td>
<td>10000</td>
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<td>10000</td>
<td>10000</td>
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<td>Total pwr/gnd area for H. Dur. (mm²)</td>
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<td>11.52</td>
<td>11.52</td>
<td>11.52</td>
<td>11.52</td>
<td>11.52</td>
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<td>11.52</td>
</tr>
<tr>
<td>MAX area ITRS, St. Dev., Current density (mm²)</td>
<td>30.49</td>
<td>35.57</td>
<td>40.33</td>
<td>45.02</td>
<td>50.59</td>
<td>56.06</td>
<td>61.53</td>
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<td>76.94</td>
<td>82.42</td>
<td>87.89</td>
<td>93.36</td>
<td>98.83</td>
</tr>
<tr>
<td>Total number of pwr/gnd pads needed</td>
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<td>7000</td>
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Figure 3.22: A plot of the total area of the pwr/gnd pads needed for high quality on-chip power distribution and for a maximum current density of $10^7$ A/cm$^2$. The ITRS projections are also plotted.

Figure 3.23 plots the total die-surface area needed for the pwr/gnd pads. These values simultaneously satisfy the IR drop (on-chip) and solder electromigration constraints. This set of data is summarized in Table 3.3 in the row labeled "MAX". Note that if the current density limit is increased to $10^7$/cm$^2$, electromigration no longer becomes the limiting factor for the 70 nm and beyond technology nodes. Rather, the area need for acceptable on-chip IR drop as calculated in [3.15, 3.16] becomes the limiting factor.
Figure 3.23: A plot of the needed die surface area for the pwr/gnd pads to simultaneously satisfy the on-chip IR drop constraints as well as the electromigration current density limit.

Finally, in order to calculate the needed number of pwr/gnd pads ($n_{pwr\_gnd\_pads\_needed}$) that meets the above on-chip IR drop and solder electromigration constraints, the following equation is used

$$n_{pwr\_gnd\_pads\_needed} = \frac{A_{pwr\_gnd\_needed}}{(0.5P_{\text{pitch}})^2}.$$  

The pad pitch used in the equation is equal to the ITRS projections. The number of pads needed is presented in both Table 3.3 and in Figure 3.24. The number of pads far exceeds the ITRS projections for the 70 nm and beyond technology nodes. Once again, if the
current density can be increased to $10^3$/cm$^2$, then the total number of pads needed is shown in Table 3.3 in the row labeled 'Number of pwr/gnd pads for IR Dist.' [3.15, 3.16], which is projected to be approximately 9,000 at the 22 nm technology node.

![Graph showing the total number of pwr/gnd pads needed](image)

**Figure 3.24:** A plot of the total number of pwr/gnd pads needed to simultaneously satisfy the on-chip IR drop constraints and the solder electromigration limit. The figure also plots the projected number of pads by the ITRS.

### 3.3.3 Microwave Measurements

Due to their short lengths, the compliant leads exhibit good electrical performance. Using an HP8510C network analyzer with 150 µm pitch ground-signal-
ground (GSG) coplanar probes, two-port measurements of the SoL chip show in Figure 3.1 were performed at the wafer-level. The measurements were performed in the 5-40 GHz frequency range.

GSG two-port measurements were performed on a pair of leads interconnected by a 100 µm long Cu trace fabricated on the wafer’s passivation layer (silicon-nitride). As shown in Figure 3.25, this measurement characterized signal propagation through the aggregate physical path that is composed of a compliant lead, polymer via, on-chip Cu trace, back up a second polymer via, and finally through the second lead. In this measurement, the compliant leads were Au and 10 µm thick, the polymer was 15 µm thick, and the Cu trace was 1 µm thick. The width of all interconnect structures was approximately 20 µm. The measurement was made for both the long and short compliant leads, and the results for both sets of data are shown in Figure 3.26. [S11], as measured, is the magnitude of the ratio of the reflected voltage and the incident voltage at port 1. In order to achieve high signal transmission, [S11] should be as small as possible. [S21] is the magnitude of the ratio of the transmitted voltage from port 1 to port 2 and the incident voltage at port 1. It is desirable for this value to be as high as possible.

The total physical length of the measured electrical path, including the on-chip Cu trace, is approximately 330 µm for the long lead pair and 210 µm for the short lead pair. These results do not include the effects of solder bumps. However, it is expected that the solder bumps compliant with SoL dimensions will add minimal parasitics. No embedded air gaps were fabricated in the tested SoL chip. In addition, a Ti adhesion layer was used between the Au leads and the underlying polymer film.
Figure 3.25: Two-port microwave ground-signal-ground (GSG) probe setup used to characterize signal propagation through the aggregate physical path that is composed of a compliant lead, polymer via, on-chip Cu trace, back up a second polymer via, and finally through the second lead. The solid arrows refer to the signal probes and the striped arrows refer to the ground probes.
Figure 3.26: Two-port microwave measurements of both the long and short compliant lead pairs that are shown in Figure 3.1. The solid line refers to the measurements of the long lead pair, and the dashed line refers to the measurements of the short lead pair. In this measurement, the compliant leads were 10 µm thick, the polymer was 15 µm thick, and the Cu trace was 1 µm thick. No embedded air-gaps were fabricated. The plotted data is valid from ~5 GHz to 40 GHz. Data outside of this frequency range is not valid.

Crosstalk between adjacent parallel leads was measured to be less than -30 dB at ~40 GHz as shown in Figure 3.27. The tested sample consisted of leads fabricated on a polymer film. No vias were fabricated in the polymer film, and thus, the leads were
electrically isolated. Crosstalk between orthogonal leads was approximately -40 dB or 10 dB lower than parallel leads.

![Graph](https://via.placeholder.com/150)

**Figure 3.27:** Crosstalk measurement between the long Au leads when they are parallel to each other (60 µm apart). In this measurement, the leads were 15 µm thick and fabricated on a 15 µm thick polymer layer.

Similar microwave measurements for other packaging technologies exist in the literature, and they are summarized in Figure 3.28 [3.17]. Although some of these measurements take into account the effects of the board material when the packages are flip-chip mounted and the above measurements do not (since all measurements were made at the wafer-level), it is seen that the SoL measurements rank high in the figure. This suggests that SoL exhibits relatively high frequency performance.
Figure 3.28: A summary of insertion-loss versus frequency for BGA, flip-chip, and wirebond packages (original figure is reproduced from [3.17]). The dotted line is the approximate representation of the SoL measurements shown in Figure 3.26 (the insertion-loss of signal propagation into- and out-of the chip using the long leads). It should be noted that some of the measurements plotted for the other packages take into account the effects of the board while the SoL measurements do not (all measurements were made at the wafer-level).

3.4 Conclusion

First, this chapter described a method of increasing the I/O density of a Sea of Leads (SoL) chip. This was accomplished by fabricating relatively long, more compliant, leads at the periphery of the chip and relatively short, less compliant, leads at the inner region of the chip. Second, it was shown experimentally that polymer films with embedded air gaps provide substantially higher compliance and compression than
polymer films without embedded air gaps. It was also shown that when the embedded air gaps were coated with a metallic film, the compliance of the air gaps decreased and they plastically deformed following indentation. Third, this chapter described some of the issues involved in distributing high dc current. Solder electromigration was identified as potentially the key limiter to high pad current density (>10^4 A/cm^2). It was also shown that the total surface area needed for the power and ground pads was a function of the maximum allowable pad current density and the aggregate chip current drain. The conclusion of the analysis is that a substantially larger number of power and ground pads are needed than is projected by the International Technology Roadmap for Semiconductors. Finally, some preliminary high frequency measurements that demonstrate that the leads have low insertion loss up to 40 GHz were reported.
Chapter 4

Sea of Leads Process Integration with an Intel Chip

All Sea of Leads (SoL) interconnect structures considered thus far were fabricated on plain Si wafers. The wafers contained only short Cu traces to interconnect the leads in pairs for testing purposes. In order to demonstrate the process compatibility of SoL with standard front-end-of-the-line (FEOL) and back-end-of-the-line (BEOL) processes, SoL was process integrated with two chips at the wafer-level. The first chip was fabricated at Georgia Tech, and the second chip was fabricated at Intel Corporation. The goal of this chapter is not only to demonstrate the ability to fabricate SoL on those chips, but to also describe the numerous problems encountered during the process integration. By doing so, insight is attained into the process integration problems that SoL may face when integrated in a semiconductor foundry. Such insight helps to improve SoL technology because previously unknown problems are identified and are resolved. In short, this chapter describes how to reconcile SoL fabrication requirements with semiconductor FEOL and BEOL processes as well as standard industry assembly processes. In some instances, easy solutions were not found at the time of writing this thesis.
4.1 SoL Process Integration with a Georgia Tech

CMOS Chip

SoL was first process integrated with a CMOS chip fabricated by the CMOS Group at the Georgia Institute of Technology [4.1]. The circuit functionality of the chips was pre-determined by the CMOS Group. As a result, the chips that were used for SoL process integration were not selected because of their functionality, but rather for their immediate availability. The chips were fabricated using a two-metal and two-poly 1.3 μm process. Moreover, the chips used a CMOS FEOL and an Al BEOL processes.

The fabrication processes demonstrated in Chapter 2 were used here. However, no embedded air gaps were fabricated, and the purely metallic leads were fabricated. SoL was fabricated on the CMOS chips in the following manner: a 13 μm thick film of the polymer Avatrel 2000P was spin coated on the wafer. A soft bake (20 min on a 100°C hotplate), ultraviolet (UV) flood exposure (1000 mJ at 365 nm), and a polymer cure followed next. The polymer cure was performed in a nitrogen-purged furnace for 2 hrs at 200°C. The next process step was to deposit a hard mask on the polymer film to ultimately facilitate the fabrication of the vias using reactive ion etching (RIE). As described in Chapter 2, Al is typically used as the hard mask. However, it was not possible to use Al with these chips because the on-chip interconnects were Al. Figure 4.1 is a schematic illustrating the problem. Once the vias are etched, the hard mask must be removed. If the hard mask is the same metal as the die pads, then etching the hard mask will also cause the die pads to be etched. As a result, a new hard mask material that exhibits high etch selectivity against Al had to be selected. This task proved to be more
difficult than originally anticipated. The first candidate was Cu. However, Cu exhibits poor adhesion to the polymer film. Moreover, nitric acid, which is one of wet etchants of Cu, is also reactive with Al. The next metal to be tested was Cr. However, when Cr is sputter deposited on a polymer film, the Cr film tends to quickly show signs of stress by cracking during subsequent processing. Ti is a poor hard mask for this polymer because the gases (O₂ and CHF₃) used to etch the polymer in the RIE attack the Ti layer. Specifically, CHF₃ etches Ti. Au, on the other hand, exhibits excellent etch selectivity against Al. However, it suffers from poor adhesion to the polymer (and is expensive). Thus, a 300 Å thick layer of Ti was sputter deposited between a 4000 Å thick Au film and the polymer to increase adhesion. While Au would probably never be used as a hard mask in a semiconductor foundry, it was acceptable to use it for this academic demonstration. Non-metallic hard masks, such as silicon nitride or oxide, can potentially be used.

Figure 4.1: Schematic illustrating the need to select a hard mask that exhibits high etch selectivity against the metal used for the die pads.
Photolithography was used next to pattern the Ti/Au hard mask into circular vias. A KI based solution and buffered oxide etchant (BOE) were used to etch the Au and the Ti layers, respectively. Next, the exposed regions of the polymer film were etched using a PlasmaTherm RIE. The recipe used in the RIE was 300 W, 280 mtorr, 45 sccm of O₂, and 5 sccm of CHF₃. Following the etch, the Au and Ti hard mask films were etched. This time, however, an EDTA based solution was used to etch the Ti film since the HF based BOE solution attacks the underlying Al pad and the surrounding SiO₂, which was used as the on-chip interlayer dielectric. Figure 4.2 is an optical micrograph of a portion of the chip following the RIE of the vias and the removal of the hard mask. Next, a Ti/Au/Ti (200 Å/0.2 μm/300 Å) seed layer was sputter deposited, and Au leads were plated. The process steps used for the fabrication of the leads are identical to those described in Chapter 2. Figure 4.3 is a die micrograph of a CMOS chip with SoL, and Figure 4.4 is a higher magnification image. It should be noted that the yield of the fabricated structures was not high. In many instances, there were holes at the via side of the leads. The voids become visible after the seed layer was etched. Figure 4.5 is a micrograph illustrating this defect. This can potentially be attributed to the lack of a passivation layer on the surface of the CMOS chips that were used for this set of experiments. It appears that the use of BOE to etch the bottommost Ti film of the seed layer also attacked the interface between the Al pads and the SiO₂ interlayer dielectric. The lack of a chip passivation meant that nothing protected the Al interconnects and the interlayer dielectric. Since no chip passivation process was available at the time these experiments were made, no further work was pursued.
Figure 4.2: A CMOS chip with etched vias through the polymer Avatrel 2000P.

Figure 4.3: Die micrograph of a CMOS chip with SoL.
Figure 4.4: Higher magnification image of a CMOS chip with SoL.

Figure 4.5: Micrograph illustrating a die pad delaminating from the via end of a lead.
4.2 SoL Process Integration with an Intel Chip

SoL has also been process integrated with a chip fabricated by Intel Corporation at the wafer level [4.2]. Due to Intel's confidentiality policy towards their microchip fabrication details, not much is known about the chips. The chips, however, are one of Intel's test chips used to characterize the reliability of various solder interconnections. The on-chip interconnects were Cu, and the uppermost layer on the chips was a polymer. The top most Cu interconnects were approximately 1 μm thick, and the die pad pitch was approximately 200 μm. The square-shaped vias through the chip's passivation layer were approximately 30 μm x 30 μm in size. The chips were fabricated on eight-inch Si wafers. No other (relevant) details are available about the chips.

Before the results of integration are presented, it is appropriate at this time to describe the overall goal of this research collaboration between Georgia Tech and Intel Corporation. The primary goal was for Intel Corporation to investigate the feasibility of using SoL I/O interconnections while our (Georgia Tech's) primary goal was to be part of the transitioning process of SoL from academia to industry and to learn from the overall experience.

4.2.1 Cost Analysis

The very first task was to estimate the cost of SoL chip I/O interconnections. Using the fabrication processes described in Chapter 2, the cost of SoL technology was estimated internally by Intel Corporation. The calculated costs were compared to Intel's present C4 process cost. No assembly costs were included in the analysis. In addition, the
costs of the non-wetting/barrier layers for solder were not included because these are essentially standard processes and are indifferent to the use of compliant interconnections. Thus, the costs associated with these added steps may cancel for both Intel’s present interconnect technology and the compliant leads.

The added cost for Intel to use SoL interconnections without the embedded air gaps is about 5% of the baseline C4 cost. The four most expensive process steps relative to the total cost are summarized in Table 4.1. The table illustrates that 15% of the added 5% total cost is from the electroplating process (the leads are assumed to be Cu). Wet etching, polymer and resist spinning, and developing each account for 10% of the total added 5% cost.

SoL with embedded air gaps is about 90% more expensive to fabricate than Intel’s current C4 cost. As shown in Table 4.1, the spin coating of the polymers, adhesion promoters, and resists account for 30% of the total added costs. Developing of the resists, metal sputtering, and wet etching account for 15%, 10%, and 10%, respectively, of the total added costs. The size of error in this cost analysis was estimated by Intel to be as high as 50%. The presented costs only account for lead fabrication and do not include any assembly costs as stated earlier. As a result, these numbers are potentially biased against SoL since the reduction in costs associated with underfill dispensing and curing are not subtracted from the costs of SoL. According to Intel [4.2], it is unlikely that a compliant interconnect technology that is 10% more expensive than its current I/O interconnection technology would be adopted.

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Table 4.1: Table summarizing the costs of the four most expensive process steps relative to the total cost of the entire fabrication process. The table summarizes the results for SoL with and without embedded air gaps. The cost increase relative to Intel's present C4 cost is about 5% for SoL without embedded air gaps and about 90% for SoL with embedded air gaps.

<table>
<thead>
<tr>
<th>Step</th>
<th>Step cost/total cost (%)</th>
<th>Step</th>
<th>Step cost/total cost (%)</th>
</tr>
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<tbody>
<tr>
<td>Lead electroplating</td>
<td>15</td>
<td>Spin on</td>
<td>30</td>
</tr>
<tr>
<td>Wet etch</td>
<td>10</td>
<td>Developing</td>
<td>15</td>
</tr>
<tr>
<td>Spin On</td>
<td>10</td>
<td>Sputtering</td>
<td>10</td>
</tr>
<tr>
<td>Developing</td>
<td>10</td>
<td>Wet etching</td>
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4.2.2 Fabrication Details

The details of SoL fabrication on the Intel wafers is described in this section. Intel supplied several 8" Si wafers. Each 8" wafer was sawed into rectangular pieces that were approximately 2" x 3.5" (4" diagonal). This was necessary to accommodate the substrate size limitation of the mask aligners in the Microelectronics Research Center's cleanroom at Georgia Tech. SoL (without embedded air gaps) was fabricated on the Si pieces using the processes described in Chapters 2. However, there were some important differences. First, the only polymer film under the leads was the Intel polymer. The polymer Avatrel 2000P was not used with these samples to simplify fabrication. Thus, the first process step was to sputter a seed layer. All but one Si piece was coated with a Ti/Au/Ti (300 Å/0.2 μm/300 Å) seed layer using a Unifilm dc sputter. The other Si piece was coated
with a seed layer that yielded slippery leads. The method used to fabricate the slippery leads is identical to one described in Chapter 2 where Ti islands were first patterned over the vias followed by Au blanket coating. Following seed layer deposition and resist patterning, the leads were electroplated. The process details of photoresist patterning are identical to those described in Chapter 2. The total thickness of the leads was 10 μm. The leads were electroplated Au and Ni. The Au layer was 8 μm thick, and the Ni layer was 2 μm thick. This was accomplished by first electroplating Au to an 8 μm thickness. Next, Ni was electroplated to a 2 μm thickness. The same photoresist layer (or mold) used to electroplate the Au layer was used to electroplate the Ni layer. This fabrication process yielded Au leads with Ni coating only at their upper surface. Ni was not plated on the sidewalls of the leads. The significance of this will be observed in the section describing the details of assembly. The purpose of the Ni layer was to ultimately provide a non-wettable surface for the solder and thus, contain the solder during reflow and assembly. After the leads were plated, the rectangular Si pieces were placed in the RIE and exposed to an O2 rich plasma for approximately 10 min. This process heavily oxidized the Ni layer making it a good non-wettable solder layer. The seed layer was not etched prior to this step. This is important because the seed layer protected the chip’s underlying polymer passivation during RIE. Figure 4.6 is a die micrograph of the Intel chip after the leads were electroplated, and Figure 4.7 is a higher magnification micrograph of one region on the chip.
A 12 μm thick layer of the photoresist NZ9-8000 was spin coated next on the rectangular Si pieces and patterned such that vias were fabricated at the bump end of the leads. The process details of photoresist patterning are identical to those described in
Chapter 2. Next, the Ni oxide layer was etched using a HCl based solution. Following the etch, the samples were placed in a solder plating solution where 60/40 Sn/Pb solder bumps were plated to an approximate height of 30 μm. Following the plating process, the seed layer was etched. Figure 4.8 and Figure 4.9 are SEM micrographs of the leads with solder bumps on their tips.

Figure 4.7: Higher magnification micrograph of an Intel chip with SoL.
Figure 4.8: SEM micrograph of a portion of an Intel chip with solder bumps on the tips of the leads.

Figure 4.9: Higher magnification image of a lead with a solder bump on an Intel chip.
4.2.3 Selection of Correct Flux

The fabrication of the leads on the Intel chip was not a difficult task, although tremendous amount of time was devoted to perfecting the fabrication process of SoL using this mask set on dummy wafers before its fabrication on the fully functional Intel wafers. Once SoL was fabricated, the Si pieces were shipped back to Intel where dicing of the individual chips and assembly took place. The first task was to experiment with solder reflow. A successful solder reflow process requires the use of a correct flux. If the flux is too aggressive, the oxide on the Ni will be removed, and the solder will wick the entire lead. Thus, it is important to select the correct flux for SoL interconnections when Ni oxide is used as the non-wettable surface around the solder bumps. Figure 4.10 is a micrograph of a set of leads after being placed in a reflow oven when no flux was dispensed on the sample. The bumps do not show evidence of a good reflow. On the other hand, Figure 4.11 is a micrograph illustrating the bumps when an organic flux was used during the reflow process. Intel did not disclose any details about that flux. The bumps form spherical balls and are confined to the tips of the leads, as desired. Finally, Figure 4.12 is a micrograph illustrating the consequences of using a more aggressive flux. Once again, the details of the flux chemistry were not disclosed. It is clear that the new flux is too aggressive to be used with the fabricated SoL interconnections because it managed to remove the nickel oxide layer from the Ni surface. This caused the solder to wick most of the lead. Such a scenario would prevent the successful assembly of chips.

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Figure 4.10: Micrograph of solder bumps on the tips of the leads after reflow. No flux was used in this case.

Figure 4.11: Micrograph of solder bumps on the tips of the leads after reflow. An organic flux was dispensed on the sample prior to reflow. It is clear that the solder is contained at the tips of the leads.
Figure 4.12: Micrograph of solder 'bumps' on the tips of the leads after reflow. A more aggressive flux was dispensed on the sample prior to reflow. It is clear that the solder wets most of the lead.

Even when the more aggressive flux was only coated on the printed wiring board (PWB), after assembly, the solder somehow managed to wick most of the lead. Figure 4.13 and Figure 4.14 are micrographs of the chip and the board, respectively, after assembly and subsequent die detachment from the board. It is clear from the micrographs that the solder wicked the leads. This effect caused essentially no solder bumps to make contact with the pads on the PWB. Another important factor that contributed to the poor contact between the chip and the PWB is height variation (non-uniformity) of the organic board. Because of these factors, the assembled SoL chip detached from the board with very little shear force.
Figure 4.13: Assembled die showing clear evidence of solder wicking due to the use of a flux that is too aggressive.

Figure 4.14: Micrograph of a portion of the PWB after chip detachment (Figure 4.13). The image illustrates that most of the Cu pads on the board made little to no contact with solder on the leads.
4.2.4 Compatibility with Wafer Sawing

Once the proper flux was selected, the next issue was dicing: how to dice a wafer when compliant leads are fabricated on the surface of the wafer. The challenge is that high pressure deionized (DI) water is used during the sawing process. As a result, it was important to somehow protect the leads from such a high pressure water stream. This led to the idea of encapsulating the leads with a material during the sawing process. This material had to meet the requirements of being transparent to mitigate the alignment of the saw to the saw streets on the wafer. Moreover, the material had to facilitate easy removal. Some of the thick resists used in typical MEMS fabrication were the first candidates for use as the encapsulation material. However, most were not sufficiently transparent to the vision system used on the sawing equipment. In addition, most could only be removed through a dry etch.

Figure 4.15 is a schematic illustrating how the dice were sawed after being encapsulated. First, the saw was used to cut through most of the encapsulating material. Next, the saw was used to scribe 70 μm into the wafer. Finally, a third saw singulated the dice. Figure 4.16 illustrates a set of micrographs that show the effects of the sawing process on a 130 μm thick encapsulating layer of GerTak. It is clear that the sawing process had caused damage to the encapsulation material. Thus, it was important to also select a material that is soft enough to absorb the stress induced during the sawing process. Figure 4.17 compares the results of sawing on two different encapsulating materials. The material shown on the right in the figure was selected as the best material to encapsulate the wafer with.
Recall in Chapter 2 that several types of leads were described, including adhered and partially slippery leads. Based on these experiments, it was determined that the encapsulating material was not needed for the 'adhered' leads but was essential for the partially slippery leads. When the encapsulating film was not used, the slippery leads 'disappeared' following wafer dicing; the leads delaminated off the wafer.

Figure 4.15: Wafer sawing details.
Figure 4.16: The effects of wafer sawing on the encapsulating material as a function of saw direction.
Figure 4.17: This figure illustrates the importance of selecting the proper encapsulating material during wafer sawing. The figure on the left illustrates the results from using GenTak. It is clear that severe damage was caused to the material. The figure on the right illustrates the results of sawing using a different material.

4.2.5 Saw Street Reduction Problem

Another problem with the use of compliant leads compared to solder bumps is the problem associated with saw street reduction. This problem is illustrated in Figure 4.18 and can be described as follows: the compliant leads at the edges of the die extend beyond the active region of the die. As a result, they extend well into the saw streets between the dice. This problem was discovered during the sawing process. As a result, it was not possible to compensate for it during layout design. The position of the saw streets were slightly shifted to compensate for this effect as schematically illustrated in Figure 4.19. Figure 4.20 is a micrograph of the sawed streets after being shifted.
Figure 4.18: Schematic illustrating the saw street reduction problem.

Figure 4.19: Schematic of the final saw streets.
4.2.6 Assembly Related Challenges

Now that the solder reflow process was optimized, and the wafer sawing process was established, the next challenge was assembly. There were two types of boards used for SoL attachment (one with and one without solder bumps). The height variation of the solder bumps on the board was on the order of 20 μm. Even the boards without solder bumps were non-planar. As a result, when the chips were flip-chip bonded (with no applied force during solder reflow), only a few leads managed to make contact with the solder/pads on the board. This yielded the poorly bonded sample shown in Figure 4.14 and Figure 4.21. In order to overcome this problem, thermo-compression bonding was used. The assembly flow diagram of this process is shown in Figure 4.22. First, the organic flux described previously was coated on the PWB, which contained the solder
bumps. Next, the SoL chips were bonded using thermo-compression. The SoL chips used for this experiment contained leads without solder bumps on their tips. Instead, a patch of Au film equal in width to the bump was fabricated on the tips of the leads. A proper bonding profile, which consists of both temperature and force, had to be identified. As a result, two different bonding profiles were tested and are shown in Figure 4.22. The difference between the two profiles is the time duration at the peak temperature.

Figure 4.21: Micrographs illustrating the problem associated with solder bump height non-uniformity on the organic board. In the left image, the bump on the left makes good contact to the tip of the compliant lead while the bump on the right does not. The image on the right is a higher magnification image of the bump that did not make contact. Note how large the bump size of the compliant lead is relative to the on-chip Cu interconnects, which appear as a sea-of-tiny-dots.
Figure 4.22: Schematic illustrating the process flow diagram of thermo-compression bonding and the two bonding profiles used.

In order to characterize the mechanical interconnection of the leads and thus, the chip to the solder bumps on the PWB, a shear force was applied on the chips following their attachment. Figure 4.23 illustrates a micrograph of the board after the chip was detached for each of the two bonding profiles. Under both profiles, the leads broke into two halves. Under the first profile, however, a larger segment of each lead remained attached to the solder bumps on the board. Under the second profile, a smaller segment of each lead remained attached to the solder bumps. This is probably due to the fact that under the first bonding profile, the bonding time at the peak force was longer, and thus, each solder bump was able to make contact with a larger segment of each lead. Figure 4.24 illustrates the dice after detachment from the boards shown in Figure 4.23. It is clear that most of the leads are no longer intact.

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Another problem encountered with the assembly process is that the bonding quality was a function of location on the die. At the corners of the chips, the solder seems to spread out more than at the center. Figure 4.25 illustrates the solder spreading problem for each of the two bonding profiles. The micrographs clearly suggest that the second bonding profile yielded less solder spreading. This is expected because the second bonding profile has a smaller hold time at the peak temperature. Because of solder spreading, the solder dissolved the Au leads (since the sidewalls of the leads were not covered with Ni) at some locations. This is shown in Figure 4.26.

4.3 Conclusion

This chapter primarily described the process integration of Sea of Leads (SOL) chip I/O interconnections with an Intel chip. The leads were fabricated using the process recipes described in Chapter 2. Au leads with a nickel oxide non-wettable top surface were fabricated to confine the solder bumps to the tips of the leads. It was experimentally verified that the use of the proper flux during solder reflow and assembly was essential in preventing solder from alloying the entire surface of the leads. In addition, it was shown that the leads fabricated on the edges of a die tend to extend beyond the active region of the die. This problem was mitigated by shifting and reducing the width of the saw streets. The use of an encapsulating film over the leads during wafer sawing was determined to be essential for the slippery leads. When no encapsulating film was used, most of the slippery leads delaminated or broke during wafer sawing. Non-slippery leads did not require the encapsulating film. Finally, it was shown that when the sidewalls of the leads were not covered with a non-wettable solder surface, solder partially dissolved the Au
leads during thermo-compression bonding. This problem was slightly reduced by decreasing the time duration at the peak force during thermo-compression bonding.

The research collaboration between Georgia Tech and Intel signaled the end of major research relating to the first generation of SoL at Georgia Tech. However, some research effort in assembly/reliability was still ongoing. While the Intel project was at its climax, new research opportunities for high density and highly process integrated electrical and optical chip I/O interconnections were being pursued at Georgia Tech (there has been no convincing demonstration of an integrated electrical and optical chip I/O interconnection technology yet). This work ultimately became the second generation of SoL and is described in the following chapter.
Figure 4.23: Micrographs of the boards after assembly and application of shear force on the assembled dice under the two bonding profiles of Figure 4.22. The micrographs illustrate that under both bonding profiles, a segment of each lead remained attached to the bumps on the PWB after the dice were sheared off.
Figure 4.24: Micrographs of the dice after assembly and detachment under the two bonding profiles of Figure 4.22. Since segments of the leads remained adhered to the solder bumps on the PWB, it is no surprise to see that most of the leads were no longer intact.
Figure 4.25: Micrographs illustrating one of the corners of the board (after detachment) under the two bonding profiles of Figure 4.22. The images suggest that the solder was less spread out under the second bonding profile.
Figure 4.26: Micrographs of the leads at the corners of the dice (after detachment) under the two bonding profiles of Figure 4.22. Due to solder spreading, many of the leads, which have exposed Au sidewalls, were consumed by the solder.
Chapter 5

Sea of Polymer Pillars:

I/O Configurations and Fabrication

In Chapters 2, 3, and 4, the first generation of Sea of Leads (SoL) was described. This SoL technology generation offered s-like leads above a polymer film with embedded air gaps. As a result, the first generation of SoL provided compliant input/output (I/O) interconnections that are parallel (in-plane) to the surface of the wafer. This fact implies that the design space of the first generation of SoL is confined to the subspace spanned by the x-y axes, as schematically illustrated in Figure 5.1. The design of in-plane compliant leads requires a relatively large amount of surface area and thus, potentially limits the I/O density of the chip. This motivates the development of surface-normal compliant I/O interconnections, or pillar-like I/O interconnections. A pillar interconnect would occupy the least amount of surface area and thus, would facilitate the fabrication of very fine pitch interconnections. Indeed, the second generation of SoL is based on the concept that pillar-like interconnects are used as the chip's I/O interconnections. Figure 5.1 illustrates the design space of the second generation of SoL.
The key question to address was the choice of material to use for the fabrication of the pillar interconnections. Polymers were the primary candidate due to their very low modulus and high mechanical flexibility. Polymers are also relatively easy to process. Finally, polymers are widely used for the fabrication of planar optical waveguides on the printed wiring/waveguide board (PWWB). As a result, a polymer pillar, in principle, can be used as an optical waveguide between the chip and the PWWB. In addition, by metallizing their sidewalls, the polymer pillars can provide electrical I/O interconnection. More significantly, however, it became clear that there were opportunities of combining the electrical and optical interconnect functions into a single polymer pillar. Because of the above listed polymer pillar interconnect opportunities, the second generation of SoL was termed Sea of Polymer Pillars (SoPP) [5.1-5.3].

Figure 5.2 is a schematic illustrating the basic principles of SoPP. The fundamental idea behind SoPP is to fabricate a set of highly compliant (mechanically flexible) polymer pillars, or polymer pins, on the die (at the wafer level), and depending on what structures are fabricated above them, the polymer pillars can be used to provide
electrical, optical, dual-mode electrical-optical, or RF interconnections, as illustrated in Figure 5.3. A dual-mode polymer pillar (Figure 5.3) is a single I/O interconnection that provides simultaneous electrical and optical interconnections. On the PWWB, polymer sockets are batch fabricated to hold and align the polymer pillars to the board, as shown in Figure 5.2. For clarity, Figure 5.4 illustrates a set of polymer pillars, and Figure 5.5 illustrates a set of polymer sockets. The primary focus of the research in this chapter, in general, is on the electrical and optical I/O interconnections. However, the fabrication processes developed for the integrated electrical and optical I/O interconnections also accommodate the fabrication of near-field capacitive couplers (RF I/O interconnections) and the fabrication of microfluidic polymer/metallic micropipes between the die and the board. The microfluidic I/O interconnections can be used for heat removal as well as for potential biological applications. While the RF and thermal I/O interconnects are described, little to no attempt has been made to realize them. Based on the above discussion, SoPP, in essence, extends wafer-level batch fabrication of semiconductor front-end and back-end multilayer interconnect networks to include wafer-level batch fabrication of high-density electrical, optical, RF, and microfluidic chip I/O interconnections, packaging, and testing and burn-in.

This chapter first describes the various electrical, optical, and dual-mode I/O interconnect configurations possible through SoPP. Methods of implementing RF and microfluidic I/O interconnections are also discussed. The second part of this chapter describes the fabrication details of the polymer pillars and the polymer sockets as well as the electrical, optical, and dual-mode I/O interconnections. Potential fabrication methods for the microfluidic I/O interconnections are also described.
Figure 5.2: Schematic illustration of the basic principles of SoPP chip I/O interconnection technology.

Figure 5.3: Schematic of a set of polymer pillars that provide electrical, optical, RF, and dual-mode I/O interconnections.
Figure 5.4: SEM micrograph of a set of polymer pillars. The pillars are 100 μm tall and 55 μm wide.

Figure 5.5: SEM micrograph of a set of polymer sockets. The sockets are approximately 13 μm tall.
5.1 SoPP I/O Interconnect Configurations

In the following subsections, the details of the various chip I/O interconnect configurations possible through SoPP are described. While some SEM micrographs of the fabricated interconnect structures are illustrated for clarity, the fabrication details are not described until Section 5.2.

5.1.1 Electrical I/O Interconnections

When a metal film is deposited on the surface of the polymer pillars, the pillars can be used for electrical interconnection. The sidewall surface area of the polymer pillars may be fully or partially metallized. The electrical and mechanical performance constraints will dictate the type and thickness of the metals that may be deposited on the polymer pillars. For example, the selected metal films (e.g., Ti/Cu versus Ti/Au) and their thicknesses must be selected such that the highly compliant nature of the polymer pillars is not degraded. This constraint potentially requires relatively thin metallic films. The mechanical considerations may also require that only a portion of the sidewall surface area of the polymer pillars be covered with the metal films (Figure 5.3). A potentially competing requirement is that the metal films must provide a low parasitic electrical interconnection. This constraint potentially requires a relatively thick layer of a metallic film to be deposited on the polymer pillars. As a result, the choice of the metals and the thickness of the metals are important. This issue has not yet been thoroughly investigated. The potential tradeoffs between the electrical and mechanical performance constraints are
reminiscent of the issues discussed in Chapter 3, where the impact of metallic films on the compliance of the polymer film with embedded air gaps was described.

Ideally, the metal films on the polymer pillars should be relatively thin (1-3 \( \mu \)m, total). Figure 5.6 is an SEM micrograph of a pair of polymer pillars metallized by Au electroplating. Since the pillars are compliant, underfill may be precluded during assembly of SoPP chips. The benefits of not requiring underfill include easier chip rework and cheaper and higher assembly throughput, as described in Chapter 1. Solder is assumed to be fabricated within the polymer sockets on the board.

Figure 5.6: SEM micrograph of a pair of polymer pillars metallized by Au plating.
5.1.2 Optical I/O Interconnections

5.1.2.1 Various Configurations

The polymer pillars also provide optical I/O interconnection. A polymer pillar is a transverse (perpendicular to the chip) optical waveguide: each polymer pillar acts as the waveguide core with the air surrounding it acting as the waveguide cladding. In order to facilitate optical coupling between the polymer pillars and the board-level optical planar (slab) waveguides, mirrors or grating couplers are fabricated either on the tips of the polymer pillars or within the board-level planar waveguides. The polymer pillars may be directly fabricated on photodetectors (to be described in Chapter 7) or optical sources, such as VCSELs and LEDs, as well as optical elements such as mirrors, grating couplers, and lenses.

Unlike electrical interconnections, optical interconnections do not easily tolerate right-angle bends and thus, optical devices that mitigate right-angle bends are needed at those interfaces. This is true for both within-plane and out-of-plane right-angle bends. In this research, surface-normal right-angle bends are investigated. Right-angle bends in optical interconnections can be mitigated with the use of mirrors and grating couplers. Figure 5.7 is an SEM micrograph of a polymer pillar fabricated on a mirror, and Figure 5.8 is an SEM micrograph of a set of polymer pillars fabricated on a photopolymer [5.4] with a prefabricated volume grating coupler. The corresponding schematic of Figure 5.8 is shown in Figure 5.9.

Figure 5.10 is a schematic illustrating the ability to fabricate mirrors and volume/surface relief grating couplers at either the tips of the polymer pillars or within the planar polymer waveguides on the board. The latter has been demonstrated in the
literature [5.5]. The primary advantage of fabricating grating couplers directly on the tips of the polymer pillars is that nanolithography is readily available at the wafer level due to the lithography requirements of semiconductor front-end and back-end devices. Thus, the fabrication of nanoresolution optical devices directly on the polymer pillars potentially offers significant cost advantages over the fabrication of such devices on the board-level planar waveguides.

In addition, both spherical and diffractive lenses may be fabricated on the tips of the polymer pillars, the former illustrated in the SEM micrograph shown in Figure 5.11. Lenses allow the pillar waveguides to focus the guided light onto locations away from their tips. Such a function may be useful when a polymer pillar must guide/focus the light onto a structure that is buried within the PWWB.

![SEM micrograph of a polymer pillar with lens](image)

**Figure 5.7:** A 100 μm tall and 55 μm wide circular polymer pillar fabricated on a 10 μm tall mirror. The slanted surface was fabricated by Si micromachining.
Figure 5.8: A set of 100 μm tall and 55 μm wide polymer pillars on strips of a photopolymer with a prefabricated volume grating coupler, as schematically illustrated in Figure 5.9.

Figure 5.9: Schematic of the SEM micrograph shown in Figure 5.8.
Figure 5.10: Possible methods of attaining electrical, optical, and dual-mode I/O interconnections through SoPP. Grating couplers and mirrors may be fabricated either on the tips of the polymer pillars or within the optical waveguides on the printed wiring/waveguide board (PWWB) to mitigate surface-normal optical coupling. Polymer sockets on the PWWB may be used to hold and align the pillars to the PWWB.

Figure 5.11: SEM micrograph of a polymer pillar with a spherical lens fabricated on its tip.
5.1.2.2 Making the Optical-Mechanical Interconnection

Optical solder-like material may be used to interconnect mechanically the polymer pillars to the waveguides located on the board. An optical solder, when needed, provides index matching between the two optical waveguides to maintain high coupling efficiency. The use of index matching material is widely used in optoelectronics [5.6].

One of the advantages of eliminating the need for underfill, as stated previously, is that chip detachment and rework become easier. Electrical solder is compatible with chip rework. Thus, in order to preserve the ability to perform chip rework, it is important for the optical adhesive to be used to make the pillar-to-waveguide mechanical interconnection to also mitigate chip rework. A potential material candidate for such a function is a polymer with a glass transition temperature \( T_g \) that is approximately equivalent to the melting temperature of the electrical solder. With such a material, when the board is heated, both the electrical and optical solders melt to mitigate chip detachment. Another potential material candidate is the thermally decomposable polymer used to make the embedded air gaps in Chapter 2. When the chip requires detachment, the board can be heated to a temperature high enough to melt the electrical solder and thermally decompose the sacrificial polymer to free the electrical and optical interconnections, respectively. The latter is illustrated in Figure 5.12. Ideally, the thermally decomposable polymer leaves behind a residue-free surface on all interfaces to make re-attachment of a new chip to the same board simple. As a result, with such an interconnection scheme, it is possible to rework chips with both electrical and optical I/O interconnections.
5.1.2.3 Mechanically Compliant Optical I/O Interconnections

Since the optical polymer pillars are fabricated using the same low-modulus polymer used for the electrical I/O interconnections, the optical I/O interconnections are also mechanically compliant [5.1-5.3]. This concept is schematically illustrated in Figure 5.13. The optical polymer pillars can undergo strain, as needed, by bending and stretching, to compensate for the chip's and board's different thermo-mechanical expansion behaviors. This is significant because the polymer pillars reduce the optical losses due to offset between the chip and the board, which is induced during thermal cycling. Without a compliant optical I/O interconnection, offsets in alignment between the chip and the PWWB can cause high optical losses. Thus, the polymer pillar waveguides help to maintain optical alignment during field service of the assembled system. This is a very significant result. The International Technology Roadmap for Semiconductors (ITRS) states that "The key mechanical issues with optoelectronic
packaging is aligning the path and maintaining this alignment under all service conditions ... [while] the main issue in assembly is how to automate the alignment process to reduce costs" [5.7 (pp.10-11)]. The polymer sockets enable interconnect self-alignment during assembly (see Section 5.2.1.4). The mechanically flexible polymer pillar waveguides help to maintain optical alignment "under all service conditions" [5.7]. However, it is not yet known if strain-induced birefringence is a concern with these compliant optical waveguides. Strain-induced birefringence is a concern in optoelectronic packaging, according to the ITRS [5.7].

Figure 5.13: This is a schematic illustrating how the polymer pillars compensate for the CTE mismatch between the board and the die to minimize optical losses due to offset. Thus, the polymer pillars can maintain optical alignment during thermal cycling.

It should be noted that the primary reason air is used as the waveguide cladding for the polymer pillars is because no underfill is required for SoPP chips since the pillars (electrical and optical) are laterally compliant. The air cladding and the resulting high index of refraction difference ($\Delta n$) between the core and the cladding has the benefit of
confining the optical signal and thus, minimizing optical crosstalk between the polymer pillars. Air cladding also has two additional benefits when compared to non-air cladding materials in this application: first, the polymer pillars can guide an optical signal through larger bends (due to large \( \Delta n \)), which means that the polymer pillars can provide higher compliance. Second, the air cladding does not impose any mechanical/physical constraints on the movement of the highly compliant polymer pillars. As a result, the use of air as a waveguide cladding is ideal for the polymer pillars due to its optical and mechanical properties; it provides the lowest index of refraction possible and the least mechanically resistant material (medium). However, the polymer pillars may be passivated with any cladding material when needed.

5.1.3 Dual-Mode I/O Interconnections

Thus far, the discussion has been limited to using each polymer pillar for a single interconnect function — either electrical or optical. However, it is possible to use a single polymer interconnection device that provides simultaneous electrical and optical interconnections (Figure 5.3). As described previously, a micromirror may be fabricated on the tips of the polymer pillars. An example of such a structure is shown in Figure 5.14. The SEM micrograph shows a polymer pillar with a partially slanted tip. If the sidewall metallization of the electrical polymer pillars is extended to the slanted region on the tips of the polymer pillars, then each polymer pillar can be used for simultaneous electrical and optical interconnections (Figure 5.15): the mirror reflects an optical signal from the board-level planar waveguide into the polymer pillar while the sidewall metallization
provides simultaneous electrical interconnection. This dual-mode electrical and optical polymer pillar, or heterogeneous I/O interconnect, allows for an intimate process integration between the electrical and optical I/O interconnections. A dual-mode polymer pillar, in essence, is an I/O interconnection device that provides two orthogonal interconnect functions for the price of one. By combining the electrical and optical interconnections so intimately, the I/O density of a chip increases because the same I/O footprint area provides both electrical and optical interconnections. The thickness of the metallic film has to be selected such that it yields low parasitic electrical interconnections without disturbing the high compliance of the intrinsic polymer pillars. Moreover, the metal has to be selected such that it provides high optical reflectivity at the wavelength of interest. The slanted tip must not be metallized, however, to act as a mirror. A total-internal reflection mirror may be used. Other possible dual-mode I/O interconnection structures include a polymer pillar with fully metallized sidewalls and a diffractive grating coupler on its tip.

Figure 5.14: SEM micrograph of ~100 μm tall and 55 μm wide polymer pillar with a 6 μm tall flat mirror on its tip.

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Figure 5.15: Schematic of a dual-mode polymer pillar before and after assembly.

It should be pointed out that some of the material requirements for conventional optical interconnects do not necessarily apply for SoPP. For example, SoPP is not restricted to using ultra-low absorption optical materials due to the short height (< 250 μm) of the polymer pillars. In addition, it is known that when metal surrounds an optical waveguide, the optical losses in the waveguide may increase. In dual-mode SoPP, however, the short pillar heights are expected to mitigate such losses. The metal layer, however, should be highly reflective at the optical wavelength of interest to minimize such losses. When these facts are coupled with the above mentioned concepts of compliance, it is noted that SoPP represents a unique class of interconnections.
5.1.4 RF I/O Interconnections

SpFP may facilitate RF I/O interconnects based on near-field capacitive couplers similar to those proposed in [5.8, 5.9]. A pillar with one of the two parallel plates forming the capacitor may be brought into very close proximity with the complementary metal plate at the board to form a near-field capacitor, as shown in Figure 5.3. A high-k material is fabricated between the two metal plates. The high-k material can either be fabricated above the metal on the polymer pillar or within the polymer socket. In order to secure the polymer pillar into the socket, some type of adhesive is required. The same metallization process used to make the electrical interconnections would also be used to metallize the RF interconnections. No attempt has been made to realize the RF polymer pillars in this thesis. This is because the primary focus of this thesis has been on the development of an integrated electrical and optical I/O interconnections.

5.1.5 Microfluidic I/O Interconnections

SpFP facilitates I/O interconnections that can guide microfluidic flow between the chip and the board. Such a structure would resemble a micropipe. The shell may either be polymeric or metallic. The latter is shown in Figure 5.16 and Figure 5.17. When these micropipes are fabricated between two planar microchannels on the chip and the board, fluid may be pumped through the two channels, as schematically illustrated in Figure 5.18. These micropipes can be used for heat removal as well as potentially for biological applications. Heat removal is a major concern for future chips, and thus, SpFP can be used in conjunction with a heat sink to remove heat from both surfaces of a chip. In
addition, these micropipes may potentially be a key enabling technology for wafer-level testing and burn-in, where heat removal is a bottleneck. In order to facilitate microfluidic flow, a slanted surface may be fabricated below and above the micropipes to mitigate microfluidic flow at right-angle bends, as shown in Figure 5.19. This idea parallels the requirements of the optical I/O interconnections. Finally, it is clear that the micropipes must be sealed once bonded to the board to prevent fluidic leakage. It is not yet fully known the best methods of accomplishing this.

**Figure 5.16:** SEM micrograph of a hollow metallic cylinder, or micropipe. The metal is approximately 8 μm thick electroplated Au. The height of the micropipe is approximately 100 μm, and its inner diameter is 55 μm wide.
Figure 5.17: Higher magnification SEM micrograph of a metallic micropipe.

Figure 5.18: A schematic illustrating how an out-of-plane microfluidic channel (or micropipe) can be used to connect two planar microfluidic channels on separate planes.
Figure 5.19: A metallic micropipe with a metallic slant at its tip to facilitate the routing of fluids at right-angle bends.

5.2 SoPP Fabrication

In the previous section of this chapter, the various I/O interconnect configurations were described. SEM micrographs of some of the fabricated interconnect structures were also shown. However, the fabrication processes were not described. In this section, details of the fabrication are presented.
5.2.1 Polymer Pillar and Polymer Socket Fabrication

5.2.1.1 Overview of the Fabrication Process

To date, the polymer pillars and polymer sockets have been fabricated using the photodefined polymer Avatrel 2000P (Promerus, LLC.). This is the same polymer that was used to fabricate the photoimaged via in the first generation of SoL (Chapter 2). A schematic of the fabrication process is illustrated in Figure 5.20. The fabrication process of the polymer pillars and the polymer sockets is similar. The general fabrication sequence is as follows: the first process step is to spin coat the polymer film (Avatrel 2000P) onto the substrate. The height of the polymer film will ultimately be the height of the polymer pillars (or sockets). If tall polymer pillars are desired, it may be necessary to spin coat multiple layers of the polymer film. The wafer is next placed on a hotplate for a soft bake. The hotplate temperature is 100°C and time duration depends on the thickness of the polymer film. The thicker the polymer film, the longer is the soft bake time duration. The proper soft bake time duration must be selected for a successful photoimaging process. A relatively short soft bake causes the final pattern to be distorted (especially the sidewalls). A relatively long soft bake, however, causes the polymer to thermally crosslink. Next, the polymer film is irradiated with a 365 nm ultraviolet (UV) light through a dark-field mask containing the cross-sectional geometry of the pillars (or sockets). Once exposed, the wafer is placed in a nitrogen-purged oven for a hard bake. All polymer films (regardless of the ultimate geometry of the structures and thickness) were subjected to an identical hard bake condition: 20 min in a 100°C nitrogen-purged oven. Following hard bake, the substrate is removed from the oven and placed on an insulating surface for a slow cool down. Next, the polymer is spray-developed using the
developer BioAct EC-7R to yield the polymer pillars (or sockets). Finally, the substrate is
placed in a nitrogen-purged furnace for a cure. The cure peak temperature is 200°C, and
the temperature ramp rate (from room temperature) is 3°C/min. The dwell time at the
peak temperature varies (as will be seen in Chapter 6). The typical dwell time is 2 hrs,
however. Once the dwell time has elapsed, the temperature of the furnace is ramped
downward to 125°C at a rate of 2°C/min. Finally, natural convection cools the furnace
down to room temperature. All polymer films (regardless of the ultimate geometry of the
structures and thickness) were subjected to the same cure profile. The only difference
between the various samples (to be discussed in Chapter 6) is the dwell time at the peak
temperature.

![Diagram](image)

**Figure 5.20:** The fabrication sequence of the polymer pillars and polymer sockets: (a) a
substrate, (b) Avatrel 2000P is spin coated to the desired thickness and placed on a
hotplate for a soft bake. The polymer film is next exposed to a 365 nm wavelength UV
light through a mask. The substrate is next placed in an even for a hard bake. Finally, (c)
the polymer film is spin-developed to yield the final structure.

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5.2.1.2 Fabrication Results

Figure 5.4 is an SEM micrograph of a set of 100 μm tall and 55 μm wide polymer pillars fabricated on a Si wafer with a silicon nitride (0.2 μm) passivation. A higher magnification SEM micrograph of one of the polymer pillars is shown in Figure 5.21. Pillars that are 180 μm tall and 55 μm wide have also been fabricated, as shown in Figure 5.22 and Figure 5.23. The polymer Avatrel 2000P adheres best to either silicon nitride or silicon dioxide. When the pillars are fabricated directly on Si, the yield is typically low due to poor adhesion, as clearly illustrated in Figure 5.24. Pillars with various aspect ratios and cross-sectional geometries have also been successfully fabricated, as shown in Figure 5.25. This is important because the polymer pillar's geometry and aspect ratio dictate their mechanical compliance and optical transmission properties. More details are presented in Chapters 6 and 7. The processes outlined in the previous section can also be used to make polymer pillars at pitches almost equal to those of the top-most chip wiring level. For example, Figure 5.26 illustrates a set of polymer pillars fabricated on a 12 μm pitch, thereby creating an area-array I/O density of ~7x10^7/cm². Pitches below 10 μm are possible, and thus, it is possible to fabricate polymer pillars with a density of greater than 10^8/cm².

The highest aspect ratio polymer pillar successfully fabricated was a 20 μm tall and 4 μm wide polymer pillar with a circular cross-section (Figure 5.2). The polymer material can resolve features with much higher aspect ratios, however. For example, Figure 5.27 is an optical micrograph of a set of 100 μm tall and 10 μm wide polymer pillars that have collapsed onto the surface of the wafer following spray developing. This demonstrates that the polymer material exhibits the remarkable ability to photoimage.
structures with an aspect ratio of 10. However, the high aspect ratio polymer pillars do not have the mechanical stability to remain standing. This imposes one of the limitations on the fabrication of high aspect ratio polymer pillars. Another important parameter that imposes a limitation on the fabrication of high aspect ratio polymer pillars is the pitch. The closer the polymer pillars are to each other, the more difficult it is to fabricate perfectly standing polymer pillars.

All polymer pillars described thus far had very smooth sidewall profile, which is an important attribute for the optical waveguides. However, it is possible to photoimage the polymer pillars such that they attain different sidewall characteristics. For example, low aspect ratio polymer pillars with sidewalls resembling gear teeth are shown in Figure 5.28.

Finally, complex three dimensional structures such as polymer steps can be fabricated, as shown in Figure 5.29. This structure was fabricated by first photoimaging and fabricating the polymer stub and then fabricating the polymer pillar above the stub. Thus, this structure required two masking steps.
Figure 5.21: Higher magnification SEM micrograph of one of the polymer pillars (100 μm tall and 55 μm wide) shown in Figure 5.4.

Figure 5.22: SEM micrograph of a set of polymer pillars that are 186 μm tall and 55 μm wide.
Figure 5.23: Higher magnification SEM micrograph of one of the polymer pillars (180 μm tall and 55 μm wide) shown in Figure 5.22.

Figure 5.24: SEM micrograph of a set of polymer pillars fabricated on a Si wafer. After an extended period of spray developing, the pillars clearly lose their adhesion to the Si surface.
Figure 5.25: SEM micrograph illustrating various shape and aspect ratio polymer pillars.

Figure 5.26: SEM micrograph of 13 μm tall and 5 μm wide circular polymer pillars distributed on a 12 μm pitch (<10 μm pitches are possible).
Figure 5.27: Micrograph of a set of 100 μm tall and 10 μm wide circular polymer pillars after spray developing. Clearly, while the features were resolved, the very high aspect ratio polymer pillars were mechanically unstable and thus, collapsed.

Figure 5.28: Pair of low aspect ratio polymer pillars that were photoimaged such that they attained the very distinctive sidewall profile shown. The gear teeth pattern was part of the cross-sectional pattern of the pillars on the mask.
Figure 5.29: Polymer pillar above a polymer stub. The polymer stub is 20 µm tall and 55 µm wide while the polymer pillar is 100 µm tall and 55 µm wide.

5.2.1.3 Details of the Process: Fabrication Recipes

The polymer spin conditions, soft bake duration, and UV energy dosage are a function of the thickness of the polymer film. The thicker the polymer film, the longer is the soft bake and the higher is the UV energy dosage. As previously demonstrated, polymer pillars and sockets with a very wide range of aspect ratio have been successfully fabricated. The spin conditions, soft bake duration, UV exposure dosage, hard bake conditions, and spray developing duration are summarized in Table 5.1 as a function of polymer thickness. The Avatrel 2000P dielectric polymer used in these experiments is dissolved in a simple hydrocarbon solvent at a concentration of 45% solids by weight. Note that the tall (100 µm and greater) polymer pillars required multiple spin cycles. For example, to fabricate the ~100 µm and 55 µm wide polymer pillars, the first polymer layer should be spin coated under the spin conditions listed under the 1st
spin cycle. Following an 8 min soft bake on a 100°C hotplate, a second layer of the
copolymer film is spin coated. The spin conditions are listed under the 2nd spin cycle. This
time, the soft bake is 45 min long. Next, the wafer is placed in a mask aligner and
irradiated with 1500 mJ of UV light at a wavelength of 365 nm. Finally, the wafer is
placed in an oven for a hard bake followed by a 90-120 s of spray developing. The use of
a polymer formulation that has a lower solvent concentration may yield thicker polymer
layers from a single spin coat. This would eliminate the need for multiple spin cycles.

The reader should note the following: since the temperature sensors on the
hotplates tend to drift and become uncalibrated with time, the temperature displayed on
the hotplate's LED is probably not the correct temperature. As a result, it is important to
measure the temperature of a hotplate before using it. In all the above experiments, the
hotplate was actually set to 108°C to attain the desired 100°C temperature.

The adhesion of the polymer films to the underlying silicon nitride or silicon
dioxide surface can be enhanced with the use of an adhesion promoter. The manufacturer
of the polymer (Promerus, LLC.) recommends the use of a 10% weight solution of 3-
Aminopropyltriethoxysilane in a 95% ethanol solution. Details of processing can be
found in the polymer's processing guide, which is supplied by Promerus, LLC..

The Avarel 2000F polymer should always be stored in a freezer (-10°C) to
maximize its shelf life. The polymer should be thawed to room temperature before using,
however. If the polymer is spin coated while it is at a temperature lower than room
temperature, the polymer will exhibit higher viscosity, and thus, the spin conditions listed
in the table will yield thicker layers. Thus, it is recommended that the polymer be taken
out of the freezer and placed at room temperature the night before it is to be used.
Table 5.1: Summary of the process conditions required to photoimage the polymer pillars using Avatrel 2000P. The table lists the spin conditions, soft bake duration, UV energy exposure dosage, hard bake duration, and spray developing duration as a function of polymer thickness. The soft bake process step is performed on a 104°C hotplate. The hard bake process step is performed in a nitrogen-purged oven at 100°C. The UV exposure wavelength is 365 nm. The substrate is assumed to be Si. Some variations in thickness may be observed.

<table>
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<th>Thickness</th>
<th>Spin cycle number</th>
<th>Spin speed (rpm)</th>
<th>Spin duration (min)</th>
<th>UV energy dosage (mJ)</th>
<th>Hard bake duration (min)</th>
<th>Spray developing duration (s)</th>
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<td>15</td>
<td>200</td>
<td>20</td>
<td>60</td>
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<tr>
<td>20 μm</td>
<td>---</td>
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<td>20</td>
<td>300</td>
<td>20</td>
<td>60</td>
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<td>---</td>
<td>1000/500/500/40</td>
<td>25</td>
<td>850</td>
<td>20</td>
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<td>8</td>
<td>---</td>
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<tr>
<td></td>
<td>2</td>
<td>1000/500/500/40</td>
<td>45</td>
<td>1500</td>
<td>20</td>
<td>90-120</td>
</tr>
<tr>
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<td>50</td>
<td>1900</td>
<td>20</td>
<td>150-180</td>
</tr>
</tbody>
</table>
5.2.1.4 Polymer Sockets: Discussion

Polymer sockets have been fabricated using the same polymer and process described above. Figure 5.5 is an SEM micrograph of various aspect ratio polymer sockets. Ultimately, polymer sockets with positively slanted sidewalls should be fabricated to provide chip-to-board self alignment during assembly: if the pillars are misaligned with respect to their intended position on the board during assembly, the positive slants on the sockets' sidewalls will cause the pillars to slide down to their intended location. This is illustrated in Figure 5.30. The height of the polymer sockets depends on the height of the polymer pillars. Ideally, only a small percentage of the pillar's height should be inserted into the socket. Moreover, the polymer used to fabricate the sockets should have a lower index of refraction than the polymer used to fabricate the pillars and the planar optical waveguides beneath. This maintains the total internal reflection criteria for both waveguides.

It is difficult to fabricate high aspect ratio sockets for reasons similar to those described in Chapter 2 since the sockets are essentially vias. Residue free polymer sockets can be easily attained at relatively small aspect ratios.

Figure 5.30: Schematic of polymer sockets with a positive sidewall profile to mitigate easier pillar insertion and assembly.

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5.2.2 Fabrication of Polymer Pillars on Grating Couplers and Mirrors

5.2.2.1 Polymer Pillars on Volume Grating Coupler

Polymer pillars have been successfully fabricated on volume grating couplers and mirrors. With respect to the grating couplers, Figure 5.9 is a schematic of the fabricated structure shown in Figure 5.8. A 2 μm thick silicon dioxide layer was first deposited using a PlasmaTherm PECVD at a process temperature of 150°C on a photopolymer with the prefabricated volume grating coupler. The photopolymer with the prefabricated volume grating coupler is similar to the one reported in [5.4]. The use of a higher temperature process in the PECVD could damage the photopolymer, and thus, the temperature at which deposition was performed was limited to 150°C. Following PECVD, 100 μm tall and 55 μm wide polymer pillars were fabricated above the silicon dioxide film. The process conditions listed in Table 5.1 were used to fabricate the polymer pillars. One important difference, however, is that the soft bake time duration had to be increased dramatically (by a factor of 2-4) since the substrate was glass and not Si. Glass has poor thermal conductivity compared to Si, and thus, the increase in soft bake time duration compensates for this. For example, in Table 5.1, the 2nd soft bake step listed for the 100 μm thick polymer film was increased from 45 min to 100 min.

Following the fabrication of the polymer pillars and thermal cure (at peak temperature of 150°C for 1 hour), a Au hard mask was sputter deposited on the glass substrate. Next, photolithography was used to pattern the hard mask into long channels. Using a PlasmaTherm RIE, the silicon dioxide film and the photopolymer were etched. Following
RIE, the Au hard mask was etched using a KI based solution. Figure 5.8 illustrates the final structures.

5.2.2.2 Polymer Pillars on Mirrors

Polymer pillars have also been successfully fabricated on mirrors, as shown in Figure 5.7. The mirrors were fabricated through wet etch of a <100> orientation p-type Si wafer using KOH. The slant is 54.74°. The mirrors were fabricated as follows: a Si wafer was first coated with a 1 μm thick SiO₂ hard mask. Photolithography was used next to pattern the hard mask into 9 mm long and 100 μm wide rectangles. Dilute 45% KOH at 90°C solution was used next to etch the Si. Following the Si etch, the hard mask was etched using buffered oxide etchant (BOE). The slants should next be metallized to enhance optical reflectivity. The choice of metal depends on the wavelength of interest. However, the mirrors shown in the SEM micrograph were not metallized, for simplicity. The polymer pillars were next fabricated above the slanted regions using the process steps previously described (Table 5.1).

Mirrors have also been fabricated using a 'polymer spin around' method. In this method, a polymer slant is fabricated by first fabricating a structure with vertical sidewalls such as the polymer stubs shown in Figure 5.31. Next, a polymer film is spin coated on the substrate with the prefabricated polymer stubs to finally yield structures similar to those shown in Figure 5.32. The fabrication of mirrors using RIE of polymers has been demonstrated in the literature [5.10]. Such processes and structures can be process integrated with the polymer pillars.
Figure 5.31: SEM micrograph of polymer stubs.

Figure 5.32: SEM micrograph of slanted surfaces (mirrors) fabricated by spin coating a polymer film on a wafer with prefabricated polymer stubs, similar to those shown in Figure 5.31. The slants were next Au metalized to enhance reflectivity.
5.2.3 Polymer Pills with Spherical Microlenses on their Tips

Figure 5.33 is a schematic of one possible fabrication process that yields spherical lenses on the tips of the polymer pillars (Figure 5.11). The general fabrication sequence is as follows: two substrates are prepared in parallel. The first (Figure 5.11a) is a substrate coated with a polymer film (no soft bake is performed, and thus, the polymer is in liquid form). The second (Figure 5.11b) is a substrate with prefabricated polymer pillars. Next, the substrate with the pillars is flipped and pressed against the substrate with the liquid polymer film (Figure 5.11c). The aggregate structure is next placed on a hotplate for a brief soft bake. When the two substrates are separated after the brief soft bake, the polymer pillars attain polymer spheres on their tips due to surface tension (Figure 5.11d). This process of 'pillar dipping' is essentially an extension of the processes reported in [5.11, 5.12] in which the core of a fiber optic cable was dipped into photoresist to create a lens on the tip of the fiber.

Figure 5.34 is an SEM micrograph of a set of polymer pillars that was fabricated on a set of mirrors, similar to those shown in Figure 5.7, and have spherical microlenses on their tips. Figure 5.35 is a higher magnification SEM micrograph of one of the structures shown in Figure 5.34. The microlens on the tip of the polymer pillar can be used to enhance the optical input coupling efficiency into the polymer pillar. It may also be used to focus light away from the polymer pillar. In the SEM micrographs, the polymer pillars were 100 μm tall and 55 μm wide. The polymer spin coated on the first substrate was 20 μm thick. When the two substrates were joined, the aggregate sample was placed on a 100°C hotplate for 3 min. Next, the substrate with the polymer pillars
was pried off with a pair of tweezers. The substrate should not be sheared off. The polymers used to make the pillars and the lenses can be of different materials and thus, different indices of refraction. The lenses can be made using a different index of refraction material to control the optical properties of the lenses. The size of the lenses can be controlled by controlling the thickness of the spin coated material. In general, the height of the lenses will be equal to the thickness of the polymer film on the first substrate. If the lenses are fabricated using a photodefensible material, then the size and geometry of the lenses can be tailored by performing a photoimaging (patterning) process on the lenses. There are other methods of making the lenses, including heating the tips of the polymer pillars (temperature close to their glass transition temperature). Such an approach is mask-less.

Figure 5.33: The fabrication process used to fabricate spherical lenses on the tips of the polymer pillars. (a) Substrate after spin coating of a polymer, (b) substrate with prefabricated polymer pillars, (c) the substrate with the pillars is pressed against the substrate with the liquid-polymer, (d) the substrate with the pillars is removed.

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Figure 5.34: SEM micrograph of a set of polymer pillars with spherical lenses on their tips. The polymer pillars are fabricated on Si micromachined mirrors.

Figure 5.35: Higher magnification SEM micrograph of a polymer pillar with a spherical lens on its tip. The polymer pillar is fabricated above a Si micromachined mirror. The indices of refraction of the polymer pillar and spherical lens can be different.
5.2.4 Polymer Pillars with Micromirrors on their Tips

The tips of the polymer pillars can be patterned into any surface topology. In this section, methods of fabricating polymer pillars with slanted tips are described. However, the fabrication processes described can be used to fabricate polymer pillars with any other tip surface topology (surface relief gratings, diffractive lenses, concave and convex lenses and mirrors, etc.).

5.2.4.1 Method 1: Polymer Molding

In the first method, the fabrication process is based on polymer molding. The idea is to mold the top portion of a polymer film into the desired topology while it is in the uncured or plastically deformable state (mechanical measurements demonstrating this concept are described in Chapter 6). In principle, such a process should work. However, molding the polymer at room temperature is very difficult because the pressure required is relatively high. Thus, the approach adopted in this work is to mold the polymer at the end of the soft bake process step. Figure 5.36 is a schematic of the fabrication process. First, a mold is fabricated (Figure 5.36a). For simplicity, Si was used to fabricate trapezoidal hills, similar to those used as mirrors below the polymer pillars (Figure 5.7). Dilute 45% KOH at 90°C solution was used to etch the Si. A 1 μm thick SiO2 hard mask was used during the Si etch. Once fabricated, a 50 μm thick film of the polymer Avatrel 2000P was spin coated on another Si wafer, which had a silicon nitride passivation. Next, the wafer was placed on a hotplate for a soft bake (Figure 5.36a). After a 15 min soft bake, the mold was pressed against the polymer film and maintained there for the remainder of the soft bake (Figure 5.36b), which was 25 min long. Following the soft
bake, the mold was removed (pried off) from the polymer film (Figure 5.36c). This was a nontrivial task because the Si mold was 'adhered' to the polymer film. Ideally, the mold should be covered with a film that is phobic to the polymer being molded, or some type of lubricant should be used to prevent the two from adhering. Once molded, the substrate with the molded polymer film was placed in the mask aligner and was exposed through a mask containing the cross-sectional geometry of the polymer pillars. The wafer and the mask were aligned relative to each other such that the circular features on the mask were above the regions of the polymer film with the molded slants. Once exposed, the wafer was placed in a 100°C oven for 20 min (the typical hard bake process step). Finally, the molded polymer film was spray developed to yield polymer pillars with slanted tips (Figure 5.36d). Figure 5.37 illustrates a structure that was fabricated using this fabrication process. It is also possible to perform the molding process after the fabrication of the polymer pillars.

The process described above takes advantage of the ability to plastically deform the polymer at a temperature that is well below the \( T_g \) value of the polymer. The compression molding of non-photosensitive optical polymer waveguides at a temperature equal to their \( T_g \) has been reported in the literature [5.13, 5.14]. However, the \( T_g \) values were so low (60–180°C) that it is highly unlikely that such a polymer would be integrated into the PWWB or at the chip level. The hot embossing of polymer waveguides (with 45° mirrors at their ends for surface-normal coupling) that are more thermally stable at temperatures above 160°C has also been demonstrated [5.15]. However, the polymer was not photosensitive. The approach described in Figure 5.36 allows one to first pattern the
surface topology of a polymer film by plastically deforming the polymer and then photoimaging that polymer film into the desired structures.

Figure 5.36: Schematic of the fabrication process used to mold a polymer film to ultimately yield polymer pillars with slanted tips. The key is to mold the photosensitive polymer film while it is in the plastic (uncured) deforming state. (a) Mold is prepared. A polymer film is spin coated and partially soft baked. (b) The mold is pressed on the polymer film. (c) The mold is removed to leave behind the molded polymer film. (d) A standard photoimaging process follows next, and the polymer film is spray developed to yield polymer pillars with slanted tips.
Figure 5.37: SEM micrograph of a polymer stub with a partially slanted tip. This polymer structure was fabricated using the fabrication process outlined in Figure 5.36.

5.2.4.2 Method 2: Flip-Pillar Bonding

An alternative to the above described molding process is the reverse molding process outlined in Figure 5.38. The idea is to fabricate the polymer pillars on a template and then flipping the pillars onto another substrate such that the template pattern at the base of the pillars becomes the tip of the final reversed polymer pillars. The fabrication process begins by fabricating a template, or a mold, as shown in Figure 5.38a. Once again, Si was chosen as the template. Slanted channels were fabricated on a Si wafer using the same processes outlined previously. Next, a 100 μm thick polymer film of the polymer Avatrel 2000P was spin coated on the template (Figure 5.38b). Note that the polymer was directly spin coated on Si to reduce purposefully the adhesion between the polymer and the substrate. The importance of this will be noted in the following paragraph. The template was next placed on a hotplate for a soft bake. The soft bake conditions are identical to the ones used to fabricate the polymer pillars (Table 5.1). Next,
the substrate was transferred to the mask aligner. As described above, the circular features on the mask were aligned relative to the template such that they intersected with the slanted regions on the template. Following the exposure, the substrate was placed in an oven for a hard bake. The UV energy dosage and the hard bake process conditions are similar to those used to make the intinsic polymer pillars (Table 5.1). Next, the polymer film was spray developed (Table 5.1) to finally yield polymer pillars on the slanted Si surface, as shown in Figure 5.38c.

On another substrate, a very thin layer (~3 μm) of Avatrel 2000P was spin coated (Figure 5.38d). The polymer used for this purpose had a higher concentration of solvent than the one used to fabricate the polymer pillars to mitigate the spin coating of thin polymer layers. The substrate was chosen to be glass to later mitigate the optical testing of the structures. Next, the template was flipped and pressed against the glass substrate with the thin layer of Avatrel 2000P, as shown in Figure 5.38c. The aggregate structure was next placed on a hotplate for a soft bake, with the glass substrate being directly on the hotplate. Following a 15 min soft bake, the aggregate sample was removed and allowed to cool down. Figure 5.39 is a micrograph of the polymer pillars on the slanted Si surface looking from the backside of the glass substrate. Finally, the template was pried off the glass substrate to leave behind polymer pillars with slanted tips on the glass substrate, as shown in Figure 5.38f. This process was mitigated by the poor adhesion between the pillars and the Si surface. Remarkably, the yield from such a process was very high. Figure 5.40, Figure 5.41, and Figure 5.42 illustrate some SEM micrographs of the polymer pillars fabricated using this fabrication method.
Figure 5.38: Flip-pillar bonding: reverse molding process. (a) Template is prepared, (b) polymer film is spin coated on the template, (c) polymer pillars are fabricated, (d) a substrate is spin coated with a thin layer of a polymer (without a soft bake), (e) the template is flipped, and the polymer pillars are pressed against the polymer film. The aggregate structure is next placed on a hotplate for a soft bake, (f) following soft bake, the template is pried off leaving behind the tip-patterned polymer pillars.
Figure 5.39: Micrograph of the polymer pillars on the template as seen from the back side of the glass substrate with the thin layer of Avatrel 2000P (Figure 5.38e).

Figure 5.40: SEM micrograph of a set of polymer pillars with partially slanted tips fabricated using the process outlined in Figure 5.38.
Figure 5.41: Higher magnification SEM micrograph of one of the polymer pillars shown in Figure 5.40.

Figure 5.42: SEM micrograph highlighting the slanted region on the tip of a polymer pillar.
The slants may also be fabricated using directional RIE at oblique angles [5.10]. This method was successfully implemented to integrate 45° microres for surface-normal coupling into an H-tree polymeric waveguide optical clock distribution network with a 1-to-48 fan out [5.16].

5.2.5 Metallized Polymer Pillars and Out-of-Plane Micropipes

5.2.5.1 Polymer Pillar Metallization

There are many methods of metallizing the polymer pillars. In this research, a brute force method was adopted, although there are more elegant methods of metallizing the polymer pillars that do not require photoresist. Following the fabrication of the polymer pillars, a Ti/Au (300 Å/0.3 μm) seed layer was deposited using a Unifilm dc sputtering system. A thick layer of the negative tone photoresist NR3-8000 (Futurerex, Inc.) was next spin coated on the wafer. Using photolithography, the resist was patterned such that it was removed from the sidewalls of the polymer pillars. Next, the wafer was placed in an Au plating solution to plate the sidewalls of the polymer pillars. The end result of this process is polymer pillars with a thick layer of Au metallization on their sidewalls, as shown in Figure 5.6. Other metals can also be used.

5.2.5.2 Out-of-Plane Micropipe Fabrication

A potential fabrication process for the out-of-plane micropipes is an extension of the process used to fabricate the metallized polymer pillars. The only difference is that
the seed layer was first etched off the tips of the polymer pillars to expose the underlying polymer. Next, the sidewalls of the polymer pillars were plated to the desired thickness. Following electroplating, the wafer was placed in a nitrogen-purged furnace where the polymer pillars were thermally decomposed (see Section 5.2.5.3, below) The temperature profile used for the decomposition is the same as the one described for curing. The only difference is that the peak temperature was 420°C. Following thermal decomposition, transverse metallic micropipes are fabricated, as shown in Figure 5.16 and Figure 5.17. The sidewall thickness of these structures is approximately 8 µm. If the polymer pillars were thermally decomposed while they were fully encapsulated with a metal film, pressure buildup can cause the metal to break. This is shown in Figure 5.43. The yield from the fabrication process just described was relatively low; the polymer pillars do not melt/decompose uniformly across a wafer. This process requires more refinement.

5.2.5.3 Effects of Temperature on the Polymer Pillars

The maximum allowable temperature that the polymer pillars can be exposed to is very important. The temperature conditions that the polymer pillars are limited to are dictated by the polymer material used to fabricate the polymer pillars. All polymer pillars and polymer sockets were fabricated using the polymer Avatrel 2000P, as described earlier. This polymer has a Tg of approximately 250°C. This Tg value sets the upper temperature limit. The polymer pillars lose their geometrical shape at temperatures above the Tg value. For example, Figure 5.44 is an SEM micrograph of a 100 µm tall and 55 µm wide polymer pillar after being placed in a -350°C furnace for 30 min. The geometry/shape of the polymer pillar clearly changed. At this temperature, the results indicate that the polymer pillar partially melted and partially thermally decomposed.
Relative to the original polymer pillar, the polymer pillar shown in Figure 5.44 is approximately 30% smaller in width and height. Figure 5.45 is an SEM micrograph of a set of 100 µm tall and 55 µm wide polymer pillars after being placed in a 380°C furnace for 2 hrs. The polymer pillars clearly melted and almost completely thermally decomposed. Figure 5.46 illustrates an area on the substrate where it is clear that the pillars melted and lost most of their volume. Based on these results, it is important to maintain the polymer pillars in an environment below the polymer’s Tg to preserve the geometrical integrity of the structures. Short exposures to higher temperatures, however, can potentially be tolerated.

Figure 5.43: SEM micrograph of a pair of hollow metallic polymer pillar shells. The polymer pillars were thermally decomposed while they were fully encapsulated with a Au film. Pressure build-up during decomposition is potentially what caused the Au film to tear.
Figure 5.44: A 100 μm tall and 55 μm wide polymer pillar after being placed in a ~350°C nitrogen-purged furnace for 30 min.

Figure 5.45: The effects of high temperature on a set of 100 μm tall and 55 μm wide polymer pillars. The polymer pillars were exposed to 380°C for 2 hrs.
5.3 Conclusion

This chapter introduced the I/O interconnect configurations and fabrication details of the second generation of Sea of Leads (SoL), or Sea of Polymer Pillars (SoPP). The fundamental idea behind SoPP is to fabricate highly compliant, or mechanically flexible, polymer pillars (or polymer posts) on dice at the wafer level and to fabricate polymer sockets on the board to hold and align the polymer pillars to the board. Depending on what structures are fabricated above the polymer pillars and within their respective polymer sockets, the polymer pillars can be used for electrical, optical, and RF I/O interconnections. The electrical polymer pillars are created by metallizing the polymer...
pillars. The optical polymer pillars are created by fabricating a diffractive grating coupler on the tips of the polymer pillars. The diffractive grating coupler mitigates surface-normal optical coupling between the planar optical waveguide on the board and the polymer pillar waveguide. Polymeric spherical lenses may also be fabricated on the tips of the polymer pillar waveguides. One of the most significant attributes of SoPP is that all I/O interconnections (electrical and optical) are mechanically flexible. The compliant optical I/O interconnections maintain optical alignment between the chip and the board during thermal cycling to minimize optical losses due to offset. The use of a single polymer pillar for simultaneous electrical and optical interconnections was also described. Such a structure, or a dual-mode polymer pillar, provides a very high level of electrical and optical I/O interconnect process integration. The most promising dual-mode polymer pillar structure is a polymer pillar with metallized sidewalls and a metallized slanted tip. This chapter also described how SoPP can provide microfluidic I/O interconnections between two parallel planes (chip and board) through the fabrication of surface-normal microfluidic micropipes. Such structures can potentially be used for chip heat removal.

Various fabrication processes have been developed to fabricate the interconnect structures described above. The heart of all processes, however, is the photoimaging process of the polymer Avatrel 2000P. This polymer was used to fabricate all polymer interconnect structures.
Chapter 6

Sea of Polymer Pillars Mechanical Measurements

Sea of Polymer Pillars (SoPP) input/output (I/O) interconnect configurations and fabrication details were described in Chapter 5. In this chapter, three-dimensional mechanical measurements of the polymer pillars are presented. The measurements presented provide insight into the mechanical characteristics of the polymer pillars in the lateral and normal axes. The lateral, or in-plane, measurements demonstrate the high compliance of the polymer pillars. The normal, or out-of-plane, measurements demonstrate that the pillars undergo elastic compression at relatively large loads. This is important for many reasons. For example, it is critical that the polymer pillars are not damaged during assembly or processing due to the potential application of high loads. High transverse loads are also induced during the attachment process of heat sinks on the back side of chips. The reported polymer pillar out-of-plane and in-plane force-displacement measurements in this chapter are a function of the polymer pillar's aspect ratio, process conditions (cure time duration), and metallization. Moreover, simple fatigue measurements are made to demonstrate that the force-displacement characteristic curves of the polymer pillars essentially remain constant after multiple strain cycles.
6.1 Out-of-Plane Force - Displacement

Measurements

6.1.1 Indentation of Various Polymer Structures

The setup used to measure the out-of-plane force-displacement characteristic curves of the polymer pillars is shown in Figure 6.1. Using a Hysitron TriboIndenter equipped with a high-force head and an approximately 200 µm radius spherical tip, a set of polymer pillars was indented at room temperature. It is important to keep in mind that the measured force-displacement characteristic curves are a function of the probe tip. In general, the larger the tip surface area, the more force is required to indent a fixed depth. Since the primary interest in these experiments is to study the mechanical behavior of the polymer pillars and not the material that the polymer pillars are fabricated from, the correct tip size and geometry have to be selected. A relatively small and sharp tip will indent the polymer pillar's material while a relatively large and flat tip will indent the polymer pillar as a structure. At the time the measurements were performed, the availability of the tips was limited. There were no flat and wide tips available for purchase from Hysitron. The best available tip that met the above stated criteria was a spherical tip with a ~200 µm radius.
Table 6.1 illustrates three sets of indentation data. The first set of data is that of a blanket polymer film cured at 200°C for 4 hrs. The second set of data is that of polymer pillars also cured at 200°C for 4 hrs. Finally, the third set of data is that of polymer pillars with identical geometry to those measured in the second set except that the polymer pillars were uncured. In all three sets of data, the maximum force (mN) and the loading rate (μN/s) were programmed into the software controlling the indenter and are shown in the table. The exact (measured) applied force and the resulting displacement of each tested structure are also reported in the table.
Table 6.1: A summary of the out-of-plane force and displacement values for various indented polymer structures. The measurement setup is shown in Figure 6.1. There is a 5 s hold at the peak force.

<table>
<thead>
<tr>
<th>Sample #</th>
<th>Structure description</th>
<th>Max. force (mN)</th>
<th>Loading rate (μN/s)</th>
<th>Indent duration (s)</th>
<th>Measured force (μN)</th>
<th>Measured displacement (μm)</th>
<th>Disp. - Force ratio (μm/μN)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1</td>
<td>Poly film</td>
<td>25</td>
<td>100</td>
<td>505</td>
<td>25.07</td>
<td>1.5</td>
<td>0.060</td>
</tr>
<tr>
<td>A2</td>
<td>100 μm thick, 4 hrs cure at 200°C</td>
<td>25</td>
<td>1000</td>
<td>55</td>
<td>25.29</td>
<td>1.4</td>
<td>0.055</td>
</tr>
<tr>
<td>A3</td>
<td>100 μm thick, 4 hrs cure at 200°C</td>
<td>5</td>
<td>100</td>
<td>105</td>
<td>5.5</td>
<td>0.52</td>
<td>0.101</td>
</tr>
<tr>
<td>A4</td>
<td>110 μm thick, 4 hrs cure at 200°C</td>
<td>5</td>
<td>1000</td>
<td>55</td>
<td>5.21</td>
<td>0.55</td>
<td>0.106</td>
</tr>
<tr>
<td>A5</td>
<td>110 μm thick, 4 hrs cure at 200°C</td>
<td>1N</td>
<td>40,000</td>
<td>55</td>
<td>1.0012N</td>
<td>18.7</td>
<td>0.019</td>
</tr>
<tr>
<td>B1</td>
<td>110 μm x 55 μm, 4 hrs cure at 200°C</td>
<td>600</td>
<td>40,000</td>
<td>35</td>
<td>600.7</td>
<td>61.3</td>
<td>0.102</td>
</tr>
<tr>
<td>B2</td>
<td>110 μm x 55 μm, 4 hrs cure at 200°C</td>
<td>25</td>
<td>1000</td>
<td>55</td>
<td>25.30</td>
<td>2.5</td>
<td>0.14</td>
</tr>
<tr>
<td>B3</td>
<td>110 μm x 55 μm, 4 hrs cure at 200°C</td>
<td>5</td>
<td>100</td>
<td>105</td>
<td>5.18</td>
<td>0.79</td>
<td>0.15</td>
</tr>
<tr>
<td>B4</td>
<td>110 μm x 55 μm, 4 hrs cure at 200°C</td>
<td>5</td>
<td>1000</td>
<td>55</td>
<td>5.24</td>
<td>0.73</td>
<td>0.14</td>
</tr>
<tr>
<td>B5</td>
<td>110 μm x 55 μm, 4 hrs cure at 200°C</td>
<td>25</td>
<td>1000</td>
<td>55</td>
<td>25.30</td>
<td>1.2</td>
<td>0.047</td>
</tr>
<tr>
<td>B6</td>
<td>110 μm x 55 μm, 4 hrs cure at 200°C</td>
<td>25</td>
<td>1000</td>
<td>55</td>
<td>25.30</td>
<td>1.2</td>
<td>0.047</td>
</tr>
</tbody>
</table>

C1        | 110 μm x 55 μm, no cure | 25 | 1000 | 55 | 25.26 | 2.3  | 0.091 |
| C2        | 110 μm x 55 μm, no cure | 25 | 1000 | 55 | 25.26 | 2.3  | 0.091 |
| C3        | 110 μm x 55 μm, no cure | 25 | 1000 | 55 | 25.26 | 2.3  | 0.091 |
| C4        | 110 μm x 55 μm, no cure | 25 | 1000 | 55 | 25.26 | 2.3  | 0.091 |
| C5        | 110 μm x 55 μm, no cure | 25 | 1000 | 55 | 25.26 | 2.3  | 0.091 |
| C6        | 110 μm x 55 μm, no cure | 25 | 1000 | 55 | 25.26 | 2.3  | 0.091 |
In order to eliminate the dependence of the measurements on the tip size and shape, it is necessary to describe the z-axis displacement characteristics of the polymer pillars in terms of pressure (stress) per unit of displacement. Pressure is equal to force divided by the area the force is applied over. This conversion is fairly easy to make when the indentor tip surface area is much larger than the surface area of the structure under test. This is true for all tested circular shaped polymer pillars because while the radius of the indentor tip was ~200 μm, the radius of the polymer pillars was ~27.5 μm. Thus, the indentor tip is almost an order of magnitude larger in diameter than the tested polymer pillars. As a result, it can be assumed that the total measured force is applied over an area equal to the pillar’s tip area, which is π(27.5 μm)^2. For every 1 mN of force, the net applied pressure is 421.1 mN/mm^2, or 0.4211 N/mm^2. Considering the measurement of structure B2 in Table 6.1, the polymer pillar was compressed by approximately 3 μm at 25.3 mN, or 25.3*421.1 mN/mm^2 = 10.65 N/mm^2.

The force-displacement characteristic curves of structures A2 and B2 of Table 6.1 are shown in Figure 6.2. It is clear from the measurements that the two structures (the cured polymer film and the cured polymer pillar) undergo primarily elastic strain; the unloading curves terminate at the origine and are almost linear. Under the same cure conditions, the polymer pillar undergoes larger strain (compression) than the polymer film. For example, under 25.3 mN, or 10.65 N/mm^2, the polymer film was compressed by 1.4 μm while the polymer pillar was compressed by 3.5 μm. This result is expected for two reasons. First, since the polymer pillar is surrounded by air, the polymer pillar can easily stretch, or strain, in the lateral direction as it is being compressed. As the polymer film is compressed, however, the compressed region of the film is constrained in the
lateral direction by the surrounding polymer. As a result, the compressed region is limited from undergoing strain in the lateral direction. This causes the polymer film to exhibit higher mechanical resistance. Second, as the tip penetrates deeper into the polymer film, the tip-polymer contact area increases (since the tip is spherical in shape). This causes the effective applied pressure to gradually decrease during the measurement, which causes a decrease in the indent depth. This is probably not a significant factor in the measurement under consideration due to the small tip penetration (1.4 μm), however, this behavior is expected to be non-negligible in the measurement of structure A5 of Table 6.1, for example, due to the large compression.

![Graph](image)

Figure 6.2: Force-displacement characteristic curves of the cured polymer pillar (B2 in Table 6.1) and the cured polymer film (A2 in Table 6.1). The left curve is that of the polymer film.
As stated previously, the cured polymer pillars primarily strain elastically. This can be verified from the data shown in Table 6.1. At 5 mN, the cured polymer pillar (B4 in Table 6.1) was compressed by approximately 0.73 μm. When the applied force was increased by a factor of 5 (or 25 mN), the pillar's compression also increased by a factor of approximately 5, or 3.5 μm (B2 in Table 6.1). This value is very close to the theoretical value of 5*0.73 μm = 3.65 μm. This simple analysis cannot be extended to cases where the size of the indenter tip is comparable to the size of the structure that is indented.

Figure 6.3 illustrates the force-displacement characteristic curves of the cured polymer pillar (B2 in Table 6.1) and the cured low aspect ratio square polymer pillar (B6 in Table 6.1). It is clear that the low aspect ratio square polymer pillar exhibits a force-displacement characteristic curve similar to that of the blanket polymer film (A2 in Table 6.1). The fact that the 150 μm wide and 110 μm tall square polymer pillar (B6 in Table 6.1) has a force-displacement characteristic curve similar to that of the polymer film (A2 in Table 6.1) rather than that of the 55 μm wide and 110 μm tall circular polymer pillar (B2 in Table 6.1) indicates the following: as the polymer pillar aspect ratio decreases, the force-displacement characteristic curve of the pillars approaches that of a blanket polymer film. This is expected since as the aspect ratio of a polymer pillar approaches zero (the width of the polymer pillar becomes much larger than its height), the polymer pillar begins to resemble a blanket polymer film.

The force-displacement characteristic curves of pillars C1 and C2 of Table 6.1 are plotted in Figure 6.4. The effects of the loading rate (or measurement time duration) on the measurements are very visible for the uncured polymer pillars. The polymer is soft.
enough that the indenter tip sinks into the polymer while performing the indentation. In addition, the measurements clearly demonstrate plastic deformation: the unloading curve is essentially vertical and does not terminate at the origin. For comparison, Figure 6.5 illustrates the force-displacement characteristic curves of the cured (B2 in Table 6.1) and uncured (C2 in Table 6.1) polymer pillars. The difference in mechanical deformation (elastic vs. plastic) between the cured and uncured polymer film was the primary reason it was possible to mold the mirrors on the tips of the polymer pillars, as described in Chapter 5.

Figure 6.3: Plots of the force-displacement characteristic curves of the cured circular polymer pillar (right curve) and the square-shaped and cured low aspect ratio polymer pillar (B2 and B6, respectively, in Table 6.1).
Figure 6.6 plots the force-displacement characteristic curves of the three structures in Table 6.1 (A5, B5, and C5) that were indented with very large loads. The differences between the three curves provide vivid insight into how the mechanics of the three structures differ. The uncured polymer pillar underwent the most compression at the lowest load. The cured polymer film underwent the least compression at the highest load.

The reader should be cautioned against making direct numerical comparisons between the polymer pillars and the polymer film at such large indent depths. This is because the tip used to make these indents was spherical in shape, and thus, the tip-polymer contact area (applied pressure) on the polymer pillars and on the polymer film is different. In addition, the applied pressure gradually decreases during the indentation of the polymer film.

![Graph](image)

**Figure 6.4**: Measured force-displacement characteristic curves of the uncured polymer pillars under the two loading rates. The curve on the right is that of structure C1 in Table 6.1, and the curve on the left is that of structure C2 in Table 6.1.
Figure 6.5: Measured force-displacement characteristic curves of the cured polymer pillar (B2 in Table 6.1) and the uncured polymer pillar (C2 in Table 6.1). It is clear that the uncured polymer pillar (right curve) undergoes plastic deformation while the cured polymer pillar (left curve) undergoes mainly elastic deformation.
Figure 6.6: Measured force-displacement characteristic curves of the three structures indented with very large loads. The left most curve is that of the cured polymer film (A5 in Table 6.1), the middle curve is that of the cured polymer pillar (B5 in Table 6.1), and the right most curve is that of the uncured polymer pillar (C5 in Table 6.1).

Now that an understanding of the measurements has been attained, it is important to put the results in perspective and interpret their implication. A typical flip chip bonding process requires 5 N of force (assuming a 1 cm x 1 cm chip). If there are 1,000 I/Os distributed on that chip area, then the force per I/O is 5 mN. At this force magnitude, the above measurements indicate that the cured polymer pillars (circular) with the geometry and aspect ratios described above will be compressed elastically by 0.6 μm. This is a minimal displacement: the polymer pillars will not be crushed during bonding.
However, it is unknown at this time how temperature affects the mechanical behavior of the polymer pillars. The temperatures required for solder attachment will probably cause the polymer pillars to become soft.

6.1.2 Indentation of Metallized Polymer Pillars

Fully metallized polymer pillars were also indented. The same setup shown in Figure 6.1 was used for this set of measurements. The motivation for this set of measurements is to observe the effects of polymer pillar strain on the encapsulating metal. For this set of measurements, 110 μm tall and 55 μm wide polymer pillars cured for 2 hrs at 200°C were tested. The metallization used were Ti/Au (500 Å/1.2 μm) films. The metal layers were deposited using a Unifilm system. The Ti layer was used to enhance the adhesion between the polymer pillar and the Au film. The indenter was programmed to record the reaction force required to attain 1 μm, 3 μm, 5 μm, 7 μm, 10 μm, 15 μm, 20 μm, 30 μm, 50 μm, and 80 μm displacements. Summary of the numerical values are shown in Table 6.2. The table illustrates the value of force required to attain the peak compression for a set of polymer pillars under various load conditions. Each measurement was performed on a pair of pillars, as illustrated in the data summarized in Table 6.2. In Figure 6.7, the measured force-displacement characteristic curves of the polymer pillars that were indented by 5 μm, 10 μm, 15 μm, 20 μm, 30 μm, and 50 μm are plotted for comparison. It is clear that the polymer pillars exceeded their elastic range.

The Ti/Au films do not provide as much elastic strain as the polymer pillar. This was verified by inspecting the indented polymer pillars with an SEM. Wrinkles formed on the sidewall metallization of all polymer pillars that underwent greater than ~10% strain.
Figure 6.8 is an SEM micrograph of the pair of 10 μm indented polymer pillars. The Ti/Au wrinkles are visible at the base of the polymer pillar. At ~30% strain (~30 μm compression), the Ti/Au films on the polymer pillars become more wrinkled, as shown in Figure 6.9. At ~60% strain, the SEM micrograph shown in Figure 6.10 clearly shows the Ti/Au films rupturing and peeling off the polymer pillar. However, while the polymer pillar was compressed by ~60% of its total height, the SEM micrograph shows the polymer pillar bouncing back to a height that is comparable to its initial height following the measurement. This is evident in the micrograph since the final height of the indented polymer pillar is comparable to the height of the polymer pillar on the right, which was not indented. This result is in agreement with the elastic behavior of the polymer pillars described in the previous section. This experiment is reminiscent of placing a cardboard around a spring and trying to compress the aggregate structure. The spring will compress, but the cardboard will permanently deform. Figure 6.11 is an SEM micrograph contrasting the differences between the 7 μm and 66 μm indented polymer pillars. Again, it is clear that the metallic film undergoes plastic deformation under large loads.

The adhesion between the metal and the polymer can potentially be enhanced with an anneal. However, this will not solve the problem of metal wrinkling. The fundamental problem here is that a metallized polymer pillar is a microstructure that is composed of two materials with significantly different mechanical properties. The polymer pillar elastically deforms to absorb stress while the metal film undergoes plastic deformation under stress. This point is a recurring theme in this thesis: metal tends to degrade the mechanical characteristics of the compliant polymer structures. The effects of metal on the highly compliant polymer films with embedded air gaps were clearly
observed in the first generation of SoL. The second generation of SoL is no different: metal tends to degrade the mechanical performance of the polymer pillars.

Table 6.2: A summary of the values of interest extracted from the indentation measurements of polymer pillars with Ti/Au (500 Å/1.2 μm) metallization. The hold time at the peak force was 5 s and all measurements were 25 s in length. Moreover, all polymer pillars were ~110 μm tall and 55 μm wide and cured for 2 hrs at 200°C prior to metallization.

<table>
<thead>
<tr>
<th>Sample #</th>
<th>Rate (nm/s)</th>
<th>Measured Displ. (μm)</th>
<th>Measured Force (mN)</th>
<th>Pressure (N/m²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>100</td>
<td>1</td>
<td>12.4</td>
<td>5.22</td>
</tr>
<tr>
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<td>5</td>
<td>500</td>
<td>5.06</td>
<td>54.25</td>
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<td>500</td>
<td>5.08</td>
<td>54.12</td>
<td>22.78</td>
</tr>
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<td>7.1</td>
<td>57.16</td>
<td>24.06</td>
</tr>
<tr>
<td>8</td>
<td>700</td>
<td>7.1</td>
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<td>9</td>
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<td>26.90</td>
</tr>
<tr>
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<td>1000</td>
<td>10.11</td>
<td>66.05</td>
<td>27.81</td>
</tr>
<tr>
<td>11</td>
<td>1500</td>
<td>15.12</td>
<td>77.49</td>
<td>32.62</td>
</tr>
<tr>
<td>12</td>
<td>1500</td>
<td>15.18</td>
<td>76.21</td>
<td>32.08</td>
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<td>13</td>
<td>2000</td>
<td>20.24</td>
<td>92.5</td>
<td>38.95</td>
</tr>
<tr>
<td>14</td>
<td>2000</td>
<td>30.23</td>
<td>119.73</td>
<td>37.78</td>
</tr>
<tr>
<td>15</td>
<td>3000</td>
<td>30.36</td>
<td>114.6</td>
<td>48.25</td>
</tr>
<tr>
<td>16</td>
<td>3000</td>
<td>30.34</td>
<td>112.2</td>
<td>47.24</td>
</tr>
<tr>
<td>17</td>
<td>5000</td>
<td>50.45</td>
<td>245.81</td>
<td>101.50</td>
</tr>
<tr>
<td>18</td>
<td>5000</td>
<td>50.45</td>
<td>247.00</td>
<td>101.04</td>
</tr>
<tr>
<td>19</td>
<td>8000</td>
<td>66.25</td>
<td>570.87</td>
<td>240.34</td>
</tr>
<tr>
<td>20</td>
<td>8000</td>
<td>66.05</td>
<td>581.51</td>
<td>244.81</td>
</tr>
</tbody>
</table>
Figure 6.7: Force-displacement characteristic curves of the fully encapsulated polymer pillars that were compressed by 5 μm, 10 μm, 15 μm, 20 μm, 30 μm, and 50 μm. The pillars were coated with Ti/As (500 Å/1.2 μm).
Figure 6.8: SEM micrograph of the pair of polymer pillars (pillar number 9 and 10 in Table 6.2) that were indented by 10 μm and thus, underwent ~10% compression.

Figure 6.9: SEM micrograph of the pair of polymer pillars (pillar number 15 and 16 in Table 6.2) that were indented by 30 μm and thus, underwent ~30% compression.
Figure 6.10: The pillar on the left is pillar number 19 in Table 6.2. The pillar was compressed by 66 μm and thus, underwent ~60% compression. The pillar on the right was not indented.

Figure 6.11: SEM micrograph of a set of polymer pillars. In the lower row, the polymer pillars on the left and on the right were indented by 66 μm (pillar number 19 and 28, respectively, in Table 6.2). In the top row, the polymer pillars on the left and on the right were indented by 7 μm (pillar number 7 and 8, respectively, in Table 6.2).
6.2 Lateral Force-Displacement Measurements

6.2.1 Polymer Pillar Lateral Force-Displacement Measurements

The setup used to perform the polymer pillar lateral force-displacement measurements is shown in Figure 6.12. A diamond Berkovich tip (Figure 6.12a), which is connected to a low-force head equipped with a lateral transducer, was used to first stab the polymer pillar to mechanically secure the tip into the polymer pillar (Figure 6.12b). Once secured, the TribolIndenter was used to measure the reaction force required to displace the polymer pillar by a predefined value (Figure 6.12c).

Figure 6.12: Polymer pillar lateral force-displacement measurement setup. (a) A Berkovich diamond tip connected to lateral transducer on a Hysitron TribolIndenter. (b) The tip is secured into the polymer pillar. (c) The tip is laterally moved causing the pillar to move. The TribolIndenter measures the reaction force required to move the pillar.
The lateral force-displacement characteristic curves of several polymer structures were measured. The list of measured structures includes 110 μm tall and 55 μm diameter circular pillars, 110 μm tall and 55 μm diameter circular pillars with Ti/Au (500 Å/1.2 μm) sidewall metallization, 180 μm tall and 55 μm diameter circular pillars, 110 μm tall and 150 μm wide square pillars, and a 110 μm thick polymer film. The measurements of the polymer film were used as a benchmark with those of the polymer pillars. The measurements of the just listed polymer structures were tested as a function of various cure conditions. The three different cure conditions are no cure, 2 hrs at 200°C, and 4 hrs at 200°C. The no cure condition means that the polymer pillars were tested after they were spray developed.

Compared to the polymer pillar indentations discussed in the previous section, the measurement setup used to perform the lateral measurements is more complex. Consequently, this makes the interpretation of the measurements more difficult. The complexities in interpreting the measurements arise from several factors. First, the polymer pillar must be stabbed with the Berkovich tip to secure the tip into the polymer material (Figure 6.12b). As a result, this means that it is important to account for the applied normal force when comparing different measured data. The larger the normal force, the larger the tip penetration is into the polymer pillar. Ideally, it is desirable to push the pillars from the side so that they are not stabbed. However, this option is not available in the TribolIndenter. Second, by implanting the tip into the polymer pillar, the local interaction between the tip and the polymer material becomes important due to potential local plastic deformation. Once the tip is secured into the polymer pillar, the indenter is programmed to record the reaction force required to move the indenter tip.
(and thus the polymer pillar) in the lateral direction by the desired distance (Figure 6.12c). The next step in the measurement is for the TribolIndenter to measure the reaction force required to move the polymer pillar back to its original position. This will be referred to as the return-trip and will be important in understanding the mechanical behavior of the polymer pillars. Once the polymer pillar is back at its initial position, the tip retracts from the polymer pillar. While the primary interest is measuring the lateral force-displacement characteristic curve of the polymer pillars, the nature of the measurement setup requires a two-dimensional (2D) interpretation of the results (the normal and lateral components of displacement and force).

The four values of interest in each of the lateral force-displacement measurements are the normal force, normal displacement, lateral force, and lateral displacement. A schematic illustrating the typical curves of each of the four values of interest is shown in Figure 6.13. The load functions are programmed into the TribolIndenter by specifying the peak normal force to be applied by the tip on the polymer pillar during the measurement and by specifying the lateral displacement the tip is to travel by once it is secured into the polymer pillar. The TribolIndenter measures the resulting normal displacement and the lateral reaction force. In order to account for the effects of the applied normal force during the measurements, four different load functions were programmed and are summarized in Table 6.3.

The results from the measurements will be presented as follows: it is expedient to first provide a global overview of the measurements to understand the differences between the results under the four different load functions. Next, the measurements of the various structures under the fourth load function (Table 6.3) will be compared and
contrasted to understand the differences between the mechanical characteristics of the various structures.

Figure 6.13: Schematic illustrating the typical patterns of the four subplots of each of the lateral force-displacement measurements. The subplots are normal force (NF), normal displacement (ND), lateral force (LF), and lateral displacement (LD). The peak normal force and the peak lateral displacement curves are set prior to the measurement. Based on those values, the TriboIndenter measures the resulting normal displacement and the reaction force in the lateral direction.
Table 6.3: Summary of the four different load functions used to measure the lateral force-displacement characteristic curves of the polymer pillars.

<table>
<thead>
<tr>
<th>Function number</th>
<th>Normal force (mN)</th>
<th>Lateral displacement (μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>8</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>0.5</td>
<td>5</td>
</tr>
<tr>
<td>3</td>
<td>4</td>
<td>5</td>
</tr>
<tr>
<td>4</td>
<td>8</td>
<td>5</td>
</tr>
</tbody>
</table>

Table 6.4 presents a summary of the four values of interest for several different polymer structures when they were tested using the first load function of Table 6.3. Each measurement was repeated five times (i.e., five identical structures were each tested). Each of the values shown in the table is the average of the five measurements. Since the lateral displacement was set to 0 in this load function, this load function is essentially an indent. While in theory the measured lateral displacements and forces should be 0, due to potentially noise, these values are non-zero, as shown in the Table 6.4.

Table 6.5 presents a summary of the four values of interest for several different polymer structures when they were tested using the second load function of Table 6.3. The measured lateral reaction force is almost equivalent for all of the structures. This indicates that the indenter tip was not secured well enough into the polymer during the lateral displacement. In other words, the applied normal force was not large enough to secure the indenter tip into the polymer pillar during the measurement. Consequently, the measured lateral force is probably the value required for the indenter tip to slide on the polymer pillar's tip surface area. As a result, the success of the measurement setup shown
in Figure 6.12 depends on the ability to firmly secure the indenter tip into the polymer pillar. The two sets of measurements just described were used as a benchmark for all other measurements.

Table 6.6 and Table 6.7 present a summary of the four values of interest for several polymer structures when they were tested using the third and fourth load functions, respectively, of Table 6.3. Note that Table 6.7 also contains the measurements of 180 μm tall circular polymer pillars. The differences between the measured lateral reaction force of identical structures under the third and fourth load functions are noticeable. The larger indent depth caused by the high normal force (8 mN) causes an increase in the contact area between the indenter tip and the polymer pillar. As a result, there is a larger local interaction area that potentially leads to greater local deformation. The measured results in all tables include such effects. This potentially indicates that the true compliance value of the pillars is smaller than the value reported in the table.

When the normal displacement is large, the tip is better anchored (secured) into the polymer pillars. This implies that the recorded measurements under the fourth load function potentially more accurately reflect the compliance of the polymer pillars.

The lateral force-displacement characteristic curves of all tested polymer pillars were measured up to a peak lateral displacement value of 5 μm. However, the tested polymer pillars were shown to move laterally by approximately 10 μm (peak possible displacement from measurement setup).
Table 6.4: Summary of the lateral force-displacement measurements of various polymer structures when the first load function shown in Table 6.3 was used. The abbreviations used in the table are normal force (NF), normal displacement (ND), lateral force (LF), lateral displacement (LD), and polymer pillar (PP). The 'Initial,' 'Max,' 'Positive peak,' and 'Negative peak' values listed below correspond to those labeled in Figure 6.13. The metallized polymer pillars (labeled with 'Metal') were encapsulated with Ti/Au (500 Å/1.2 μm) films. The polymer films were 110 μm thick. The number below the polymer pillars is their height. All pillars were circular in shape and 55 μm wide, except for the 'Square PP,' which was square in shape and 150 μm wide.

<table>
<thead>
<tr>
<th>Sample</th>
<th>NF - Initial (μN)</th>
<th>NF - Max (μN)</th>
<th>ND - Initial (nm)</th>
<th>ND - Max (nm)</th>
<th>LF - Positive peak (μN)</th>
<th>LF - Negative peak (μN)</th>
<th>LD (μm)</th>
<th>LD/LF (μm/μN)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Poly Film 2 hrs Cure</td>
<td>7370</td>
<td>7370</td>
<td>3320</td>
<td>3320</td>
<td>58.4</td>
<td>201.5</td>
<td>0.043</td>
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<td>Poly Film 4 hrs Cure</td>
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<td>7380</td>
<td>2470</td>
<td>3260</td>
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<td>145.7</td>
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</tr>
<tr>
<td>PP 110 μm 2 hrs Cure</td>
<td>7250</td>
<td>7250</td>
<td>3500</td>
<td>3990</td>
<td>-171.2</td>
<td>-150</td>
<td>0.05</td>
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<tr>
<td>PP 110 μm 1 hrs Cure</td>
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<td>7296</td>
<td>3400</td>
<td>3750</td>
<td>-5.49</td>
<td>6.4</td>
<td>0.047</td>
<td>--</td>
</tr>
<tr>
<td>PP 110 μm 2 hrs Cure Metal</td>
<td>7450</td>
<td>7450</td>
<td>2500</td>
<td>2850</td>
<td>-191.2</td>
<td>-59.55</td>
<td>0.047</td>
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<tr>
<td>Square PP 110 μm 2 hrs Cure</td>
<td>7370</td>
<td>7370</td>
<td>3330</td>
<td>3330</td>
<td>87.5</td>
<td>138.2</td>
<td>0.05</td>
<td>--</td>
</tr>
</tbody>
</table>

197
Table 6.5: Summary of the lateral force-displacement measurements of various polymer structures when the second had function shown in Table 6.3 was used. The abbreviations used in the table are normal force (NF), normal displacement (ND), lateral force (LF), lateral displacement (LD), and polymer pillar (PP). The 'Initial,' 'Max,' 'Positive peak,' and 'Negative peak' values listed below correspond to those labeled in Figure 6.13. The metallized polymer pillars (labeled with 'Metal') were encapsulated with Ti/Au (500 Å/1.2 μm) films. The polymer films were 110 μm thick. The number below the polymer pillars is their height. All pillars were circular in shape and 55 μm wide, except for the 'Square PP,' which was square in shape and 150 μm wide.

<table>
<thead>
<tr>
<th>Sample</th>
<th>NF - Initial (μN)</th>
<th>NF - Max (μN)</th>
<th>ND - Initial (nm)</th>
<th>ND - Max (nm)</th>
<th>L2 - Positive peak (μN)</th>
<th>LF - Negative peak (μN)</th>
<th>LD (μm)</th>
<th>LD/LF (μm/μN)</th>
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<tr>
<td>Poly Film 2 hrs Cure</td>
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<td>359</td>
<td>600</td>
<td>710.8</td>
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<td>-213.8</td>
<td>5</td>
<td>--</td>
</tr>
<tr>
<td>Poly Film 4 hrs Cure</td>
<td>365</td>
<td>365</td>
<td>600</td>
<td>681.4</td>
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<td>-210.4</td>
<td>5</td>
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<tr>
<td>PP 110 μm 2 hrs Cure</td>
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<td>354</td>
<td>652</td>
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<tr>
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<td>635</td>
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<td>350</td>
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Table 6.6: Summary of the lateral force-displacement measurements of various polymer structures when the third load function shown in Table 6.3 was used. The abbreviations used in the table are normal force (NF), normal displacement (ND), lateral force (LF), lateral displacement (LD), and polymer pillar (PP). The 'Initial,' 'Max,' 'Positive peak,' and 'Negative peak' values listed below correspond to those labeled in Figure 6.13. The metallized polymer pillars (labeled with 'Metal') were encapsulated with Ti/Au (500 Å/1.2 µm) films. The polymer films were 110 µm thick. The number below the polymer pillars is their height. All pillars were circular in shape and 55 µm wide, except for the 'Square PP,' which was square in shape and 150 µm wide.

<table>
<thead>
<tr>
<th>Sample</th>
<th>NF = Initial (µN)</th>
<th>NF = Max (µN)</th>
<th>ND = Initial (nm)</th>
<th>ND = Max (nm)</th>
<th>LF = Positive peak (µN)</th>
<th>LF = Negative peak (µN)</th>
<th>LD (µm)</th>
<th>LD/LF (µm/µN)</th>
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<td>2000</td>
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<td>2.2</td>
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<tr>
<td>2 hrs Cure</td>
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<tr>
<td>Poly Film</td>
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<td>3500</td>
<td>2000</td>
<td>2378.8</td>
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<td>-2041.4</td>
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<td>3456</td>
<td>2250</td>
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<td>-4.9</td>
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<td>2250</td>
<td>2758.6</td>
<td>1778.4</td>
<td>-828</td>
<td>-4.9</td>
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<td></td>
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<td></td>
<td></td>
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</tr>
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Table 6.7: Summary of the lateral force-displacement measurements of various polymer structures when the fourth load function shown in Table 6.3 was used. The abbreviations used in the table are normal force (NF), normal displacement (ND), lateral force (LF), lateral displacement (LD), and polymer pillar (PP). The 'Initial,' 'Max,' 'Positive peak,' and 'Negative peak' values listed below correspond to those labeled in Figure 6.13. The metallized polymer pillars (labeled with 'Metal') were encapsulated with Ti/Au (500 Å/1.2 μm) films. The polymer films were 110 μm thick. The number below the polymer pillars is their height. All pillars were circular in shape and 55 μm wide, except for the 'Square PP,' which was square in shape and 150 μm wide.

<table>
<thead>
<tr>
<th>Sample</th>
<th>NF - Initial (µN)</th>
<th>NF - Max (µN)</th>
<th>ND - Initial (µm)</th>
<th>ND - Max (µm)</th>
<th>LF - Positive peak (µN)</th>
<th>LF - Negative peak (µN)</th>
<th>LD (µm)</th>
<th>LD/LF (µm/µN)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Poly Pillar 2 hrs Cure</td>
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<td>7300</td>
<td>3000</td>
<td>3373.5</td>
<td>4712.6</td>
<td>-4006</td>
<td>-4.98</td>
<td>1.06</td>
</tr>
<tr>
<td>Poly Pillar 4 hrs Cure</td>
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<td>7300</td>
<td>3000</td>
<td>3376</td>
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<td>-4.96</td>
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<tr>
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<td>7100</td>
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<td>1712.2</td>
<td>-444.2</td>
<td>-4.9</td>
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</tr>
<tr>
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<td>7285.6</td>
<td>3450</td>
<td>4057.2</td>
<td>2107</td>
<td>-599</td>
<td>-4.9</td>
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<tr>
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<td>7450.2</td>
<td>2500</td>
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<td>-2164</td>
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</tr>
<tr>
<td>PP 110 μm 2 hrs Cure Metal</td>
<td>7360.5</td>
<td>7360.5</td>
<td>3000</td>
<td>3515</td>
<td>4660</td>
<td>-3936.5</td>
<td>-4.95</td>
<td>1.06</td>
</tr>
<tr>
<td>PP 180 μm No Cure</td>
<td>5166</td>
<td>5166</td>
<td>4200</td>
<td>4769</td>
<td>749.8</td>
<td>~0</td>
<td>-4.9</td>
<td>6.53</td>
</tr>
<tr>
<td>PP 180 μm 2 hrs Cure</td>
<td>7198</td>
<td>7198</td>
<td>4000</td>
<td>4417</td>
<td>959.7</td>
<td>~0</td>
<td>-4.9</td>
<td>5.11</td>
</tr>
<tr>
<td>PP 180 μm 4 hrs Cure</td>
<td>7179</td>
<td>7179</td>
<td>4000</td>
<td>4559</td>
<td>1192</td>
<td>~0</td>
<td>-4.9</td>
<td>4.11</td>
</tr>
</tbody>
</table>
Now with a global understanding of what each of the four load functions measures, the next task is to understand the mechanical behavior differences between the various measured structures. For this analysis, the measurements under the fourth load function will be described since the indenter tip was secured the most with this load function. It is expedient at this point to examine the lateral force-displacement characteristic curves of the polymer films. Figure 6.14 is a plot showing the complete 2D measurement of the 110 \( \mu m \) thick film of Avatrel 2000P. The film was cured at 200°C for 2 hrs. Note the resemblances between the four subplots shown in this figure and those shown in the schematic of Figure 6.13. Figure 6.15 illustrates a similar measurement with the exception that the polymer was cured for 4 hrs at 200°C. The key value in all these measurements is the lateral force. The measured lateral reaction force in both sets of data shows non-linear (plastic) deformation. These measurements look very similar to those of the square pillar whose measurement is shown in Figure 6.16. This is expected since the aspect ratio of this structure is very small (110/150=0.73), and thus, the measured results reflect the force-displacement characteristics of the polymer material and not the structure. This fact is reinforced by examining the force-displacement characteristic curves of the 110 \( \mu m \) tall and 55 \( \mu m \) wide circular polymer pillars. Figure 6.17 plots the lateral force-displacement characteristic curves of an uncured circular polymer pillar while Figure 6.18 and Figure 6.19 are those of the 2 and 4 hrs cured polymer pillars at 200°C, respectively. It is clear that the lateral reaction force of the relatively high aspect ratio polymer pillars differs from those of the polymer films. Once the pillar reaches the peak displacement (~5 \( \mu m \)), the measured reaction force curve indicates that no lateral force was applied during the pillar's return trip (there is no negative peak force equal to
the magnitude of the positive peak force during the return trip). This is in sharp contrast to the measurements of the polymer film and the low aspect ratio square polymer pillar. As a result, one very important conclusion is that the polymer pillars elastically bounce back to their initial position. The measurement of the uncured polymer pillar indicates that the polymer is very soft. This is evident from the large normal displacement at low forces (Figure 6.17). The tip's penetration into the cured polymer pillars at the same normal force is substantially smaller.

The force-displacement characteristic curves of the 180 µm tall and 55 µm wide circular polymer pillars under the various process conditions are shown in Figure 6.20 (uncured), Figure 6.21 (cured for 2 hrs at 200°C), and Figure 6.22 (cured for 4 hrs at 200°C). The linear spring-like behavior of the polymer pillars is observed once again. It is clear that higher aspect ratio polymer pillars provide higher compliance. However, the measured lateral force curves suggest that perhaps the pillars were bending with the application of the normal force. The probability that the indenter tip was not secured at the center of the pillar is relatively high. This effect causes the pillar to bend with the application of the normal force. This potentially explains why the lateral force increases before the lateral movement of the tip. Thus, the lateral force required to displace the pillar is potentially lower than the measured peak force. For example, this force can be loosely calculated as 1161-300 = 861 µN in Figure 6.22.

Figure 6.25 illustrates the lateral force-displacement characteristic curves of a metallized polymer pillar when tested under the fourth load function of Table 6.3. The lateral force curve does not resemble that of the intrinsic polymer pillar (Figure 6.18). The encapsulating metal has caused the polymer pillar to lose some of its spring-like
behavior. The tip of one of the tested polymer pillars after the measurement is shown in Figure 6.24. The black triangular feature on the surface is the location where the indenter tip was secured. It is clear that the indenter tip penetration has caused the metal films to plastically deform. Note that in all four tables summarizing the measurements that the normal displacement of the metallized polymer pillars is smaller than those of the intrinsic polymer pillars under the same normal force. This is due to the fact that Au has a much higher modulus than the polymer.

Figure 6.14: Lateral force-displacement characteristic curves of a 110 μm thick polymer film (Avatrel 2000P) cured for 2 hrs at 200°C. The fourth load function of Table 6.3 was used in this measurement.
Figure 6.15: Lateral force-displacement characteristic curves of a 110 μm thick polymer film (Avatrel 2000P) cured for 4 hrs at 200°C. The fourth load function of Table 6.3 was used in this measurement.
Figure 6.16: Lateral force-displacement characteristic curves of a 110 μm tall and 150 μm wide polymer pillar with a square cross-section. The structure was cured for 2 hrs at 200°C, and the measurement was made using the fourth load function of Table 6.3.
Figure 6.17: Lateral force-displacement characteristic curves of a 110 µm tall and 55 µm wide polymer pillar with a circular cross-section. The structure was not cured, and the measurement was made using the fourth load function of Table 6.3.
Figure 6.18: Lateral force-displacement characteristic curves of a 110 μm tall and 55 μm wide polymer pillar with a circular cross-section. The structure was cured for 2 hrs at 200°C, and the measurement was made using the fourth load function of Table 6.3.
Figure 6.19: Lateral force-displacement characteristic curves of a 110 µm tall and 55 µm wide polymer pillar with a circular cross-section. The structure was cured for 4 hrs at 200°C, and the measurement was made using the fourth load function of Table 6.3.
Figure 6.20: Lateral force-displacement characteristic curves of a 180 μm tall and 55 μm wide polymer pillar with a circular cross-section. The structure was not cured, and the measurement was made using the fourth load function of Table 6.3.
Figure 6.21: Lateral force-displacement characteristic curves of a 186 μm tall and 55 μm wide polymer pillar with a circular cross-section. The structure was cured for 2 hrs at 200°C, and the measurement was made using the fourth load function of Table 6.3.
Figure 6.22: Lateral force-displacement characteristic curves of a 180 µm tall and 55 µm wide polymer pillar with a circular cross-section. The structure was cured for 4 hrs at 200°C, and the measurement was made using the fourth load function of Table 6.3.
Figure 6.23: Lateral force-displacement characteristic curves of a metallized (500 Å/1.2 μm Ti/Au) 110 μm tall and 55 μm wide circular polymer pillar. The structure was cured for 2 hrs at 200°C (prior to metal deposition), and the measurement was made using the fourth load function of Table 6.3.
6.2.2 Polymer Pillar Sideway Indention

In order to verify the trend in the measurements attained from the previous measurement setup, and in order to attain more insight into the physical behavior of the polymer pillars, a new measurement setup was created. A portion of a Si wafer containing the polymer pillars was mounted sideways in a Hysitron TribolIndenter, as illustrated in Figure 6.25. Next, using the high-force load head equipped with a 50 μm wide conical tip, the polymer pillars were indented at their tips. It should be noted that the high-force load head component of the indenter is independent of the low-force load head component. Thus, the measurements made in the previous section used a completely different component than the measurements reported in this section. When the polymer pillars were indented in the manner shown in Figure 6.25, the measured results reflect the force-displacement characteristic curves of the polymer pillars in the lateral direction.

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Figure 6.25: A schematic illustrating the measurement setup used to make polymer pillar sideway indentations to attain the lateral force-displacement characteristic curves of the polymer pillars.

Figure 6.26 is a micrograph of a polymer pillar that was mounted sideway (and as measured). The circular polymer pillar was ~113 μm tall and 55 μm wide and cured for 4 hrs in a 200°C furnace. The measured force-displacement characteristic curve when the polymer pillar was indented at approximately its tip is shown in Figure 6.27. The measured compliance of ~2.2 μm/mN agrees well with the measured value in the previous section (2.4 μm/mN when the fourth load function of Table 6.3 was used).

Figure 6.28 is a plot showing the force-displacement characteristic curves of the polymer pillar when indented at points 5 μm around the point used to make the measurement shown in Figure 6.27 (no indent location, however, was closer to the tip than the initial point). This provides an insight into the sensitivity of this measurement setup with respect to indent location.
Figure 6.26: Micrograph of a polymer pillar on a Si wafer that is mounted sideways. The polymer pillar is 113 μm tall and 55 μm wide. The polymer pillar was cured for 4 hrs in a 200°C furnace.

Figure 6.27: Force-displacement characteristic curve of the side mounted polymer pillar (Figure 6.26) at its tip. The average compliance from several measurements is ~2.2 μm/N.
Figure 6.28: Force-displacement characteristic curves of the sideway mounted polymer pillar shown in Figure 6.26 when indented at points around its tip.

Figure 6.29 is micrograph of a circular polymer pillar that is ~180 μm tall and 55 μm wide and cured for 4 hrs in a 200°C furnace. It is clear from visual inspection that the polymer pillar slightly tapers in width. The width is maximum (~ 55 μm) near the tip of the pillar and is minimum near the base. The difference between the two width values is less than 7%. Using the same measurement setup, the force-displacement characteristic curve of the pillar at its tip is shown in Figure 6.30. On average, the measured peak force required at the tip for a 5 μm displacement was approximately 0.9 mN. The compliance of 5.5 μm/mN is larger than the compliance measured using the previous setup (4.1 μm/mN). This is potentially due to the fact that the lateral-force values used to calculate
the lateral compliance included the pillar bending effect described earlier: the actual force required to move the pillar is lower than the peak force shown in the lateral-force curves. Figure 6.31 is the family of curves when the polymer pillar is indented at locations 5 µm around a point that ~10 µm away from the tip.

![Image](image.png)

**Figure 6.29:** Micrograph of a ~180 µm tall and 55 µm wide circular polymer pillar.
Figure 6.30: Force-displacement characteristic curve of the ~180 μm tall and 55 μm wide polymer pillar shown in Figure 6.29 at its tip.
Figure 6.31: Force-displacement characteristic curves of the sidewall mounted polymer pillar shown in Figure 6.26 when indented at points approximately around its tip.

Figure 6.32 plots the forces required to indent the polymer pillar geometry under consideration by 5 μm as a function of location across its length (height). Except for the three points nearest to the base of the pillar, the plot seems to fit a cubic curve that is a function of the length. The force-displacement characteristic curves measured to attain the peak forces plotted in Figure 6.32 are shown in Figure 6.33.

Figure 6.34 is a micrograph of a circular polymer pillar that is ~113 μm tall and 55 μm wide and is fully metallized (Ti/Au, 500 Å/1.2 μm). The pillar was cured for 2 hrs in a 200°C furnace prior to metallization. Figure 6.35 is a plot of its force-displacement
characteristic curve at its tip. The force-displacement characteristic curve of the ~113 \( \mu m \) tall and 55 \( \mu m \) wide polymer pillar (Figure 6.27) is also plotted for comparison. As was noted in the previous section, the sidewall metallization has caused the polymer pillar to undergo partial plastic deformation.

**Figure 6.32:** Plot of the measured forces required for the indenter to displace the polymer pillar (Figure 6.29) by approximately 5 \( \mu m \) at various locations across the polymer pillar's length.
Figure 6.33: Family of curves required to displace the polymer pillar by approximately 5 μm at various locations across the polymer pillar's length. The peak force values shown in Figure 6.32 were obtained from the above curves.

Figure 6.34: Micrograph of ~113 μm tall and 55 μm wide polymer pillar that is fully encapsulated with Ti/Au.
Figure 6.35: Force-displacement characteristic curve of the sideways mounted and fully metallized polymer pillar shown in Figure 6.34 (top curve). For comparison, the force-displacement characteristic curve of the same height polymer pillar cured for 4 hrs at 200°C shown in Figure 6.27 is also plotted (center curve). It is clear that the metallized polymer pillar undergoes partial plastic deformation. The displacement-force ratio of the metallized pillar is \(-1.1 \ \mu\text{m/mN}\).

Finally, great care was taken to mount the samples exactly perpendicular to the surface of the sample holder in the TribolIndenter. Since the samples were manually adhered to the stage, however, visual inspection indicated that they were tilted by at most \(\pm 7^\circ\). This could be a source of variation in the measurements from one sample to the
other. Another source of variation is the location where the polymer pillars were exactly indented. The height variation of the pillars across a wafer is also potentially important to account for. The taller the pillars are, the greater the variation across a sample. Measurements suggest that the variation is less than 5%. Finally, the indenter tip used to make the above described measurements is potentially wide enough such that the force load is not being applied over a point, but rather over a finite space. This could cause the pillar to observe a distributed load over a finite space and not a point load.

6.2.3 Polymer Pillar Simple Fatigue Analysis

It is important to demonstrate that the spring-like behavior of the polymer pillars does not diminish as the pillars undergo multiple strain cycles. This was experimentally confirmed using the same experimental setup shown in Figure 6.12. Figure 6.36 plots the force-displacement characteristic curves of a 110 μm tall and 55 μm wide circular polymer pillar (cured for 2 hrs at 200°C) that was displaced by 5 μm in two opposite directions for a total of 4 cycles (in each direction). Thus, the polymer pillar moved a total distance equivalent to 20 μm on either direction or a total of 40 μm. The results demonstrate that the lateral force-displacement characteristics of the polymer pillars do not degrade with time. The gradual increase in the positive peak lateral force is potentially due to the local tip-polymer plastic deformation. Similarly, the polymer pillars with metal covering their sidewalls were also tested in the same manner, and the result of one such measurement is shown in Figure 6.37. Evidence of plastic deformation is clear in the figure. The gradual increase in the positive peak force is partially due to the plastic deformation of the metal film around the indenter tip.

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Similarly, when the ~180 μm tall polymer pillar described in the previous section was indented multiple times at approximately 2s tip using the setup shown in Figure 6.25, the measured force-displacement characteristic curves were essentially identical.

Figure 6.36: Lateral force-displacement characteristic curves of a 110 μm tall and 55 μm wide polymer pillar with a circular cross-section under multiple lateral displacements. The polymer pillar was cured for 2 hrs at 200°C.
Figure 6.37: Lateral force-displacement characteristic curves of a Ti/Au metallized (500 Å/1.2 μm Ti/Au) 110 μm tall and 55 μm wide polymer pillar with a circular cross-section under multiple lateral displacements. The polymer pillar was cured for 2 hrs at 200°C prior to metallization.

6.3 Conclusion

This chapter presented out-of-plane and in-plane force-displacement measurements of the polymer pillars at room temperature. The out-of-plane compliance of the polymer pillars was shown to be dependent on the polymer pillar's aspect ratio and
the cure process conditions. When the polymer pillars were uncured, the polymer pillars plastically deformed. However, when the polymer pillars were thermally cured in a furnace, the polymer pillars elastically deformed with a typical displacement-force ratio of 0.15 µm/mN. A set of 500 Å/1.2 µm Ti/Au metallized (cured) polymer pillars was also indented. Visual inspection through SEM revealed that the metal around the polymer pillars primarily underwent plastic deformation while the polymer pillars underwent elastic deformation. This mismatch in mechanical behavior could impose some limitations on the out-of-plane compliance attainable from metallized polymer pillars.

Similarly, it was shown that the lateral displacement-force ratio of the polymer pillars was a function of their aspect ratio and cure process conditions. The lateral force-displacement characteristic curves of the tested polymer pillars were measured up to a peak displacement value of 5 µm. Two completely different measurement setups were used to measure the lateral displacement properties of the polymer pillars. The elastic bending of the intrinsic polymer pillars and the partial plastic bending of the metallized polymer pillars were observed from both measurement setups. The compliance of the polymer pillars increased as their aspect ratio increased. Measurements reveal that the compliance of the tested polymer pillars range between 2-6 µm/mN. Their compliance in the lateral direction decreased as the time duration at the peak cure temperature increased from 2 hrs to 4 hrs. Their compliance also decreased when the polymer pillars were metallized.
Chapter 7

SoPP Optical Measurements and Integration

with Group IV MSM Photodetectors

The various polymer pillar I/O interconnect configurations were described in Chapter 5 while the mechanical characteristics of the polymer pillars were described in Chapter 6. The focus of this chapter is two fold. First, relatively simple optical measurements that demonstrate some of the optical interconnection configurations described in Chapter 5 are reported. The measurements include those relating to dual-mode polymer pillars and polymer pillars integrated with volume grating couplers. Second, the performance of an optical subsystem that uses polymer pillars is described. In this set of experiments, some of the key performance metrics of symmetric metal-semiconductor-metal (MSM) Si photodetectors with and without polymer pillars are described.
7.1 Polymer Pillar Optical Measurements and Demonstrations

Several optical measurements have been made to experimentally demonstrate the optical interconnection configurations introduced in Chapter 5. This section describes the various measurement setups and their results.

7.1.1 Polymer Pillar Optical Measurements

7.1.1.1 Optical Transmission of a Set of Vias through Ti/Au Films

The optical transmission of a set of vias fabricated in a metallic film on a glass substrate was measured first. This measurement was made as a benchmark for all future measurements. The fabrication of the vias is as follows: first, Ti/Au metal films (300 Å/0.5 µm) were deposited using a Uniﬁlm dc sputtering system on a glass substrate. Using photolithography, the metal films were etched such that 55 µm wide circular vias on a 325 µm area-array pitch were fabricated. KI based solution and buffered oxide etchant (BOE) were used to etch the Au and Ti layers, respectively.

Figure 7.1 illustrates the measurement setup used to measure the transmitted optical power through the vias on the glass substrate. The incident light was a HeNe laser (632.8 nm wavelength) with a beam diameter of ~800 µm. The transmitted power was measured as a function of the angular rotation of the substrate. The rotation of the substrate is defined relative to the incident light. At 0°, the incident light and the glass substrate are perpendicular. The transmitted power was measured at a range of angles...
equal to $\pm 5^\circ$, as shown in Figure 7.1. The average value of the transmitted power is 0.072 mW. The peak at normal incidence in the measurement is due to back reflections. Back reflections are caused by the light reflecting off the backside of the glass substrate. The reflected light becomes incident on the laser source, which causes another reflection. This new reflection becomes incident on the substrate and thus, increases the effective incident power.

7.1.1.2 Optical Transmission of a Set of Polymer Pillars on Vias through Ti/Au Films

The next step was to fabricate polymer pillars directly above the previously tested glass substrate, which contained the vias through the metal films (Figure 7.1). The pillars were fabricated on this glass substrate as follows: a thin (0.2 µm) layer of silicon nitride was deposited using a PlasmaTherm PECVD on the patterned metal films prior to the fabrication of the polymer pillars. Silicon nitride enhances the adhesion between the polymer and the substrate. The nitride film was thin enough to be negligible in the optical measurements. Following the nitride deposition, the polymer pillars were fabricated using the process described in Chapter 5. The polymer pillars were ~100 µm tall and 55 µm wide. Note that since the polymer pillars were fabricated on a glass substrate, the soft bake time duration was increased compared to when they are fabricated on Si. The soft bake time duration was 100 min (on a 100°C hotplate). All other process steps are identical to those reported in Chapter 5. Finally, following the fabrication of the polymer pillars, the substrate was placed in a nitrogen-purged furnace for a cure (2 hrs at 200°C). The glass substrate at this stage in the process is schematically illustrated in Figure 7.2.
The transmitted power through the glass substrate with the polymer pillars is shown in Figure 7.2. The average transmitted power (Figure 7.2) is approximately 0.047 mW. This value is ~30% smaller than the value measured in the previous measurement (Figure 7.1). The decrease is due to the change of geometry of the structure under test, and it is highly unlikely that the cause of this decrease is due to the polymer material alone.

7.1.1.3 Optical Transmission of a Set of Sidewall Metallized Polymer Pillars on Vias through Ti/Au Films

Next, a set of polymer pillars was fabricated such that they had Ti/Au films covering only their sidewalls (tips were not metallized). Figure 7.3 is an SEM micrograph illustrating such polymer pillars. The process used to fabricate such polymer pillars is shown in Figure 7.4. First, polymer pillars were fabricated in the same manner as described in Section 7.1.1.2. Next, Ti/Au (300 Å/0.7 µm) films were sputter deposited on the substrate. Finally, a thick layer of photoresist (NR9-8000) was spin coated and patterned such that the metal films on the tips of the polymer pillars were exposed. KI based solution and BOE were used to etch the Au and Ti layers, respectively. The photoresist was next removed using acetone.

The transmitted power from such structures is shown in Figure 7.5. The average transmitted power is approximately 0.050 mW. The difference between the measured transmitted power from this measurement and from the previous one (pillars without sidewall metallization, as shown in Figure 7.2) is so small that it is difficult to distinguish between the two. This potentially suggests that the sidewall metallization of the polymer
pillars does not impede the pillar's ability to transmit light. Although, the output characteristic curve appears to be slightly non-symmetric with respect to 0°. This is potentially due to slightly tilted pillars. The measured transmitted power is also ~30% less than the average power measured from the setup shown in Figure 7.1 (vias through the Ti/Au films).

![Graph showing power vs rotation](image)

**Figure 7.1:** Schematic of the setup used to measure light transmission through a set of vias fabricated in Ti/Au (300 Å/0.5 μm) metal films. The vias were fabricated on a 325 μm pitch. The circular vias were 55 μm in diameter.
Figure 7.2: Schematic of the setup used to test light transmission through a set of polymer pillars fabricated above the vias shown in Figure 7.1. The polymer pillars were 100 μm tall and 55 μm wide.
Figure 7.3: SEM micrograph of a set of polymer pillars with Ti/Au sidewall metallization. The only optically transparent regions on the substrate are the tips of the polymer pillars.
Figure 7.4: Schematic illustrating the fabrication sequence used to fabricate polymer pillars with sidewall metallization (Figure 7.3). (a) Polymer pillars are fabricated on a glass substrate, (b) Ti/Au films are sputter deposited on the substrate, (c) using a stack layer of photoresist, the resist is patterned to reveal the tips of the polymer pillars. Next, the Ti/Au metal films are etched. The resist is finally etched off.
Figure 7.5: Schematic of the setup used to test light transmission through a set of sidewall metalized polymer pillars. The polymer pillars were 100 μm tall and 55 μm wide, and the Ti/Au metal films were 300 Å/0.7 μm thick.
7.1.2 Optical Measurements of Polymer Pillars with Volume Grating Couplers

In order to demonstrate the feasibility of SoPP with respect to optical interconnection, several experiments were performed. Figure 7.6 illustrates one of the experiments conducted. First, a volume grating coupler of 70% input coupling efficiency was fabricated on a glass substrate. This nonfocusing grating coupler was fabricated with methods and materials like those reported in [7.1]. A set of 100 μm tall and 55 μm wide polymer pillars was fabricated on a second glass substrate. Next, 300 Å/7000 Å thick Ti/Au metal films were sputter deposited and patterned such that the metal films covered everything except the tips of the polymer pillars. Such polymer pillars were shown in Figure 7.3. When the two glass substrates were brought into contact (no 'glue' was used to interconnect the two substrates), as shown in Figure 7.6, a 632.8 nm HeNe laser illuminated the back side of the glass substrate containing the polymer pillars. The input coupling efficiency as a function of angular rotation of the aggregate sample was measured to be approximately 50% at near normal incidence. The reduction in the input coupling efficiency is potentially due to the input coupling efficiency variation of the grating coupler across the laminated photopolymer. This experiment is significant for three reasons. First, it demonstrates the ability to couple light from a set of polymer pillars into an optical device, such as a volume grating coupler. Second, it demonstrates that depositing metal on the sidewalls of the polymer pillars does not induce detrimental consequences on the optical interconnection capability of the polymer pillars. This result is in agreement with results reported in the previous section (Figure 7.5). Third, this
Figure 7.6: Schematic of the measurement setup used to demonstrate optical coupling from a set of polymer pillars into a volume grating coupler. The polymer pillars were 55 \( \mu \text{m} \) wide and 100 \( \mu \text{m} \) tall. Coupled light into the photopolymer was \(~50\%\) at normal incidence.
A similar experiment to the one illustrated in Figure 7.6 was performed with the
difference being that a Au (0.2 μm thick) mesh was fabricated on the first glass substrate
rather than a grating coupler, as shown in Figure 7.7. When the two glass substrates were
brought into contact, light transmission was detected through the back side of the glass
substrate with the Au mesh, and simultaneous electrical interconnection was measured
using the multimeter. This represents an elementary demonstration of dual-mode polymer
pillar I/O interconnection.

7.1.3 Optical Coupling using Polymer Pillars with Slanted Tips

The ability to couple light out of a polymer pillar using a mirror on its tip has
been demonstrated. The measurement setup used for this demonstration is shown in
Figure 7.8. Using the flip-pillar bonding fabrication technique described in Chapter 5, a
set of polymer pillars with slanted tips was fabricated on a glass substrate. After flip-
pillar attachment, the polymer pillars were cured in the furnace at 200°C for 2 hrs. Next,
using a Unifilm dc sputtering system, a 0.2 μm thick Au film was deposited on the
substrate. In order to ensure that no metal was in the path of the light to be reflected off
by the mirrors, polymer pillars with 'polymer umbrellas' at their tips were used, as shown
in Figure 7.8. Such polymer pillars were fabricated by making the slanted surface on the
template highly reflective. The polymer pillars were 100 μm tall and 55 μm wide.
Figure 7.7: Measurement setup used to demonstrate electrical and optical interconnection through a set of polymer pillars.

Figure 7.8: Schematic of the structure tested to demonstrate the ability to couple light out of a polymer pillar using a mirror fabricated on its tip.
The measurement of a single polymer pillar is shown in Figure 7.9. When the laser is turned off, no light is observed from any location around the polymer pillar. However, when the laser is turned on, light is seen from the side of the polymer pillar that is opposite to the mirror's slant. While this is a simple measurement, it is an important measurement because it demonstrates that a polymer pillar with a slanted tip can be used to couple light.

![Image of the pillar when the laser is off.](image1)

![Image of the pillar when the laser is on.](image2)

**Figure 7.9:** Micrograph of a polymer pillar resembling that shown in the schematic of Figure 7.8 with and without laser illumination from the backside of the substrate.
7.2 SoPP Process Integration with Group IV MSM

Photodetectors: An Optoelectronic Subsystem

Demonstration

In this section, some of the key performance metrics of Si MSM photodetectors with and without polymer pillars are reported. The primary metrics in this analysis are the dark current ($I_{dark}$) and the normalized phot-to-dark current ratio (NPDR) [7.3]. When the dark current is low, the detector has a higher sensitivity to light and a lower power consumption. All MSM photodetectors used in these experiments were fabricated and tested at Stanford University [7.2].

An SEM micrograph of a typical MSM photodetector is shown in Figure 7.10 [7.2]. The area between the interdigitated metal fingers and the area covered by the metal fingers is the active area of the photodetector. The large pads on either side of the active area are used to facilitate electrical measurements.
Figure 7.10: SEM micrograph of a typical MSM photodetector. The micrograph is of a Ni-Si-Ti asymmetric MSM photodetector. The metals are coated with Au to prevent oxide formation.

7.2.1 Fabrication

Before describing the key performance metrics of Ti-Si-Ti symmetric MSM photodetectors before and after polymer pillar fabrication, details of the process integration are discussed. The polymer pillars were fabricated on the photodetectors using the same fabrication process described in Chapter 5. A schematic of the complete fabrication process is shown in Figure 7.11. Starting with the wafer containing the prefabricated MSM photodetectors (Figure 7.11a), less than a 1 μm thick layer of SiO\textsubscript{2} was deposited, as shown in Figure 7.11b. The SiO\textsubscript{2} film was deposited using a PlasmaTherm PECVD at a temperature of 150°C. While higher quality SiO\textsubscript{2} film can be
attained by using a higher temperature during the deposition process, it was important to maintain the MSM photodetectors at a relatively low temperature [7.3]. Next, a 50 μm thick film of the polymer Avatrel 2000P was spin coated on the wafer. After a 30 min soft bake on a 100°C hotplate, the wafer was transferred to a mask aligner. The cross-sectional geometries of the polymer pillars on the mask were aligned with respect to the wafer such that the active area of the detectors was centered within the cross-sectional geometry of the polymer pillars. Following UV irradiation, hard bake, and spray developing (details are shown in Table 5.1 of Chapter 5), the polymer pillars were in place (Figure 7.11c). Next, the wafer was placed in a nitrogen-purged furnace (1 hrs at 200°C) for a cure. Finally, it was important to etch the SiO₂ off the MSM photodetectors’ contact pads to facilitate electrical testing. Using the polymer pillars as an etch mask, the substrate was immersed in BOE to etch the SiO₂ film (Figure 7.11d). Finally, the wafer was rinsed with DI water and was shipped back to Stanford University [7.2].
Figure 7.11: A schematic of the process used to fabricate polymer pillars on MSM photodetectors. (a) Wafer with prefabricated MSM photodetectors. (b) SiO₂ is deposited on the wafer to enhance adhesion between the polymer film (subsequent step) and the substrate. (c) Polymer pillars are fabricated above the active area of the MSM photodetectors using the process described in Chapter 5. (d) Using the polymer pillars as an etch mask, the SiO₂ film was etched using BOE. This process step exposed the contact pads of the detectors to facilitate electrical testing.
7.2.2 Layout Design Details and Images of MSM

Photodetectors with Polymer Pillars

In order to investigate the effects of polymer pillar geometry and size (cross-section) on the characteristics of the MSM photodetectors, the layout was designed in the following manner: for each MSM photodetector size, circular and square shaped polymer pillar with sizes larger than (Figure 7.12(a)), equal to (Figure 7.12(b)), and smaller than (Figure 7.12(c)) the size of the active area of the photodetector were designed. Moreover, polymer pillars were not fabricated on some detectors to benchmark the measurements. This is schematically illustrated in Figure 7.12(d). Finally, few polymer pillars were designed in the layout such that they covered more than one photodetector, as shown in Figure 7.12(e).

Figure 7.13 and Figure 7.14 illustrate a set of high aspect ratio (2) and circular polymer pillars fabricated above MSM photodetectors. Figure 7.15 is an SEM micrograph illustrating two circular polymer pillars with different sizes (diameter) and aspect ratios fabricated on two similar MSM photodetectors. Figure 7.16 illustrates a square-shaped polymer pillar above a MSM photodetector with a large active area.

An optical micrograph of a set of square-shaped polymer pillars that are larger than the active area of the MSM photodetectors is shown in Figure 7.17. Figure 7.18 illustrates a pair of similar MSM photodetectors with and without a circular polymer pillar. In this case, the size of the circular polymer pillar is equal to the size of the active area of the MSM photodetector. Finally, Figure 7.19 is a micrograph illustrating MSM photodetectors with small active areas and the fabrication of equally small cross-section circular polymer pillars above them.

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Figure 7.12: Schematic illustrating how various size and shape polymer pillars (PP) were fabricated on identical MSM photodetectors (PD). Through measurements, such a layout design will ultimately provide insight into how the polymer pillars affect the characteristics of the MSM photodetectors.
Figure 7.13: SEM micrograph of a set of polymer pillars fabricated on Ti-Si-Ti MSM photodetectors.

Figure 7.14: A higher magnification SEM micrograph of Figure 7.13 illustrating a polymer pillar on a MSM photodetector.
Figure 7.15: SEM micrograph illustrating two polymer pillars with different aspect ratios fabricated on two similar MSM photodetectors.

Figure 7.16: SEM micrograph of a very low aspect ratio square-shaped polymer pillar on a large MSM photodetector.
Figure 7.17: Optical micrographs of a set of square-shaped polymer pillars fabricated above the active area of MSM photodetectors. The size of the pillars is much larger than the size of the photodetectors.
Figure 7.18: Optical micrograph of a MSM photodetector with and without a polymer pillar. The cross-sectional area of the pillar is equal to the size of the active area.

Figure 7.19: Optical micrograph illustrating small diameter and high aspect ratio circular polymer pillars fabricated above relatively small MSM photodetectors.
7.2.3 Performance Metrics of the MSM Photodetectors with and without Polymer Pillars

At the time of writing this thesis, the MSM photodetectors with the polymer pillars were partially characterized. While the measurements described below are very promising and insightful, more testing is required to fully understand the effects of the polymer pillars on the photodetectors.

As stated previously, the two performance metrics of interest are the dark current and the NPDR. The measured dark current as a function of bias and finger width and spacing for a set of symmetric Si MSM photodetectors with an active area of 1156 µm² is shown in Figure 7.20. The four samples plotted in the figure are detectors prior to fabrication of the polymer pillars (labeled "No Process"), detectors that went through the polymer pillar processing but did not have polymer pillars (labeled "None"), detectors with circular polymer pillars that are smaller than the size of the active area (labeled "Small Circle"), and detectors with circular polymer pillars that are equal to the size of the active area (labeled "Circle"). The data suggests that the MSM photodetectors with polymer pillars consistently demonstrated 1-2 orders of magnitude reduction in the dark current. The processing required for the fabrication of the polymer pillars seems to enhance the surface quality of the detectors, which, in general, causes a decrease in the dark current. Another clearly visible trend in the plots is that as the spacing between the interdigitated fingers increases, the dark current decreases.

Figure 7.21 illustrates the dark current measurements when performed on a set of symmetric Si MSM photodetectors with an active area of 10,000 µm². The measurements are plotted for the following samples: detectors prior to the fabrication of the polymer pillar...
pillars (labeled "No Process"), detectors that went through the polymer pillar processing but did not have polymer pillars (labeled "None"), detectors with square-shaped polymer pillars that are smaller than the size of the active area, (labeled "Small Square"), detectors with square-shaped polymer pillars that are equal to the size of the active area (labeled "Square"), detectors with circular polymer pillars that are equal in size to the active area (labeled "Circle"), and detectors with wide rectangular polymer pillars that cover multiple detectors (labeled "Cont Rect"). The trend in the results is similar to that of the 1156 μm² large MSM photodetectors. However, the dark current is almost an order of magnitude smaller for the MSM photodetectors with the larger active area. In addition, the continuous coverage of the wide rectangular polymer pillars yielded the lowest dark current.

Figure 7.22 plots the NPDR as a function of bias for the same samples listed in Figure 7.20. Similarly, Figure 7.23 plots the NPDR as a function of bias for the same samples listed in Figure 7.21. As expected, the NPDR is higher for the detectors with the larger active area because of their lower dark current. Moreover, detectors with larger finger spacing attained higher NPDR because of the lower dark current. The NPDR curves tend to merge for the various samples with increasing bias due to the higher responsivity of the non-processed detectors.

Many other measurements were performed. It was shown that the dark current increased when the MSM photodetectors were exposed to high temperatures for an extended period. This signifies the importance of developing low temperature processes for the fabrication of the I/O interconnections. Finally, all MSM photodetector measurements reported in this chapter were the average value of several measurements.
Figure 7.20: Measured dark current as a function of bias for a set of Ti-Si-Ti MSM photodetectors with and without polymer pillars. The plots are for detectors with a 1 μm x 1 μm and 1 μm x 4 μm finger width and spacing. The active area of the detectors is 1156 μm².
Figure 7.22: Measured dark current as a function of bias for a set of Ti-Si-Ti MSM photodetectors with and without polymer pillars. The plots are for detectors with a 5 µm x 5 µm and 10 µm x 10 µm finger width and spacing. The active area of the detectors is 10,000 µm².
Figure 7.22: Normalized photo-to-dark current ratio (NPRD) as a function of bias for a set of Ti-Si-Ti MSM photodetectors (Figure 7.20) with and without polymer pillars. The plots are for detectors with a 1 μm x 1 μm and 1 μm x 4 μm finger width and spacing. The active area of the detectors is 1156 μm². The measurements were made with a 790 nm and 1-1.5 mW laser.
Figure 7.23: Normalized photo-to-dark current ratio (NPRD) as a function of bias for a set of Ti-Si-Ti MSM photodetectors (Figure 7.21) with and without polymer pillars. The plots are for detectors with a 5 μm x 5 μm and 10 μm x 10 μm finger width and spacing. The active area of the detectors is 10,000 μm². The measurements were made with a 790 nm and 1-1.5 mW laser.
7.3 Conclusion

This chapter described some optical measurements that demonstrated the optical functionality of the polymer pillars and their ability to ultimately provide chip-to-module optical interconnection. In the first part of the chapter, optical measurements were made to demonstrate the ability of the polymer pillars to couple light into a volume grating coupler. In addition, polymer pillars with slanted tips were shown to reflect light through a relatively simple demonstration. The second part of this chapter described the process integration of the polymer pillars with Si MSM photodetectors. Initial measurements suggest that the polymer pillars do not degrade the characteristics of the MSM photodetectors. In fact, photodetectors with polymer pillars consistently demonstrated an increase in NPDR compared to detectors prior to the fabrication of the pillars. This is potentially due to the indirect consequence of enhancing the quality of the Si surface through the various process steps used to fabricate the polymer pillars. In addition, detectors with larger active area and larger finger spacing demonstrated higher NPDR.
Chapter 8

Opportunities for a Third Generation of
Sea of Leads

This chapter is essentially an extensive discussion of future Sea of Leads (SoL) prospects and research opportunities for a third generation of SoL. Unlike other chapters, neither fabrication nor measured results are presented.

To summarize, the first generation of SoL consisted of in-plane electrical and optical I/O interconnections while the second generation of SoL consisted of surface-normal electrical and optical I/O interconnections. Thus, SoL technology progressed from being exactly in-plane to being exactly out-of-plane. A potential opportunity for a third generation of SoL is in-between the two spatial extremes: curved off-surface and diagonal interconnections. Such interconnects are essentially three-dimensional diagonal leads, as schematically illustrated in Figure 8.1. The design space for each of the three SoL technology generations is illustrated in Figure 8.2. For clarity, an SEM micrograph of metallic off-surface curved leads is shown in Figure 8.3 [8.1-8.3]. The motivations for pursuing such interconnect structures will be apparent later. In short, however, the motivation for developing such structures is that they can mitigate optical interconnection between the chip and the board without the need for optical coupling devices (mirrors,
grazing coupler, etc.). In addition, the interconnections are potentially easily fabricated because their required fabrication processes take place while they are planar (all processing takes place prior to the release of the interconnections and prior to making into three-dimensional interconnections).

This chapter first describes some of the electrical and optical interconnect configurations. The reader should note, however, that the design, fabrication, and testing of curved off-surface electrical interconnections have been demonstrated in the literature [8.1-8.3]. The two primary novel features of the third generation of SoL are the optical interconnect configurations and the integration of the optical interconnections with the electrical interconnections. While there are numerous possible configurations, the main idea is to fabricate a polymer waveguide above an off-surface curved metallic lead to yield a three-dimensional optical interconnect with a radius of curvature that meets the optical and mechanical requirements. While none of the proposed structures have been fabricated, suggested methods of fabrication and implementation are presented.

![Curved and diagonal off-surface interconnect](image)

**Figure 8.1:** Schematic of a curved and diagonal off-surface interconnect.
Figure 8.2: Design space for each of the three generations of SoI.

Figure 8.3: SEM micrograph of stress-engineered metal interconnects [8.1-8.3].
8.1 Electrical Interconnections

8.1.1 Configurations

As stated above, curved off-chip electrical interconnections have been demonstrated in the literature [8.1-8.3]. SEM micrographs of some of the electrical interconnects are shown in Figure 8.3. Moreover, such structures have been assembled onto a printed wiring board (PWB) with solder, as shown in Figure 8.4.

![SEM micrograph of a bonded stress-engineered metal interconnect.](image)

**Figure 8.4:** SEM micrograph of a bonded stress-engineered metal interconnect.
8.1.2 Fabrication

The fabrication of the off-surface curved electrical interconnects has been demonstrated in the literature using a variety of methods [8.1-8.3]. One of the possible methods is illustrated in Figure 8.5. Following the fabrication of vias in the chip’s passivation layer to expose the die pads (Figure 8.5a), a release layer is first deposited and patterned into the shape of the desired metal leads. This is shown in Figure 8.5b. The release layer can potentially be metallic (Ti, for example), organic (thermally decomposable polymers, similar to those used to make the embedded air gaps), and inorganic (silicon nitride/oxide, for example). Next, a thin-film metal with a stress gradient is deposited through either sputtering or plating. Sputtering of Mo/Cr while precisely controlling the Ar pressure to yield the highly stressed metal films has been successfully demonstrated [8.1-8.3]. The metal with the built-in stress gradient is patterned before release such that a portion of the film extends over the release layer, as shown in Figure 8.5c. Finally, once the release layer is etched (or thermally decomposed, for the case of sacrificial polymers), the stress-engineered metal springs off the surface as shown in Figure 8.5d. A release window is used when needed. This concludes the fabrication of the electrical compliant interconnections.
Figure 8.5: Schematic illustrating the fabrication process of a stress-engineered metal interconnect. (a) Die pads are exposed on a wafer. (b) Release layer is deposited. (c) Stress-engineered thin-film metal is deposited. (d) Release layer is etched to release the stress-engineered metal and cause the film to spring off the surface. A release window may be used.

8.2 Optical Interconnections

8.2.1 Configurations

Optical waveguides can potentially be process integrated with the curved off-surface electrical interconnections. In fact, polymer waveguides may be directly fabricated above the curved off-surface metallic leads to yield an aggregate structure that resembles what is illustrated in Figure 8.6. Since the stress-engineered metal curves off the surface, so does the polymer waveguide. This configuration enables the routing of an
optical signal between two parallel surfaces without the use of any optical coupling devices, such as mirrors and grating couples. Instead, the underlying metal film curls upward to mitigate chip access to the cross-section of the polymer waveguide for direct butt-coupling.

![Figure 8.6: Schematic of a polymer waveguide fabricated above a curved off-surface metallic lead.](image)

The benefits of such an interconnect structure are fully harnessed when it is fabricated on the printed wiring/waveguide board (PWWB). The curved polymer waveguide can be directly bonded to an on-chip optical source or detector, as illustrated in Figure 8.7. An adhesive is used to make the mechanical interconnection. Such an interconnection enables the use of a single polymer waveguide for board-to-chip optical communication. As a result, a single polymer waveguide on the PWWB is potentially all that is needed to enable chip-to-chip optical communication. On the chip side, only optical sources and detectors are fabricated/hybrid integrated. As a result, this potentially minimizes the processing required on the board and on the chip because no mirrors and
grating couplers are needed. In addition, the overall cost of the system is perhaps minimized because the chip and the PWWB are co-designed and co-optimized.

The structure shown in Figure 8.6 requires at least two additional masking steps at the board level. The additional masking steps needed are those for the stress-engineered metal film. The planar optical waveguides are readily available since any type of guided wave chip-to-chip optical communication network requires them. The structure under consideration can be directly incorporated into a board-level optical clock distribution network. Following the fan-out distribution, it is possible to fabricate the endpoints of the clock distribution network with the above described curved off-surface leads. Also, the three-dimensional curved waveguides can have an air-cladding which decreases the tolerated radius of curvature. The optical losses associated with the curved optical waveguide are potentially less than the optical losses associated with optical coupling elements, such as mirrors and gratings, which are needed for right-angle bends. Such a comparison requires rigorous modeling and more research, however.

![Diagram of a polymer waveguide interconnection from the board to the chip.](image)

**Figure 8.7:** Schematic of an all polymer waveguide interconnection from the board to the chip.

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One of the limitations of the structure shown in Figure 8.7 is that it behaves as a unidirectional optical interconnect. The cross-sectional dimensions of a single mode planar waveguide are very small. In fact, depending on the index of refraction difference ($\Delta n$) between the core and the cladding, the thickness of the core, $t_{core}$, can be as small as 0.5-2 $\mu$m. Such small dimensions do not facilitate easy and low-loss butt-coupling. As a result, it is highly unlikely that light can be butt-coupled at high efficiency into the waveguide from a chip level optical source. Not only is the waveguide core cross-section small, but the alignment accuracy required is potentially too high to be feasible.

This problem of unidirectional interconnection is potentially mitigated with the structure shown in Figure 8.8, which resembles a microphotonic funnel. The principle idea is to fabricate the core of the waveguide such that it tapers in both thickness and width. The thickness (and width) of the waveguide core tapers from the tip, $t_{w-g \text{ tip}}$, where it is maximum, to the thickness (and width) of the board-level planar waveguide, $t_{bp}$, where it is minimum. This is necessary to reconcile the dimensional differences between the chip-level optical device and the board-level single mode planar waveguide. As a result, the large waveguide core cross-section at the chip end mitigates the spatial requirements for low-loss optical butt-coupling. It may be desirable to make the cross-section of the waveguide core at the tip to be slightly larger than the size of the detectors/sources (or mirrors/gratings) to account for the alignment tolerances. Some of the design issues involved with such an optical interconnect structure are the radius of curvature of the lead from mechanical (compliance) and optical (waveguide) perspectives, core tapering, the indices of refraction of the core and cladding, and the thickness of the cladding. Once again, the interconnect structure under consideration can
also potentially be used at the terminating ends of a board-level optical clock distribution network. The fabrication of in-plane three-dimensional tapered polymer waveguides has been demonstrated in the literature [8.4]. In addition, curved in-plane polymer waveguides have been fabricated and analyzed [8.5, 8.6].

There are numerous potential variations to the structures just described. Figure 8.9 illustrates an optical interconnect where the end portion of a planar waveguide, which is terminated with a mirror (or a grating couple), is directly bonded beneath an optical source/detector. The polymer waveguide is not fabricated on a metallic lead in this case (although, it potentially can be). The electrical leads are fabricated independent of the optical interconnections. The chip and board assembly takes place prior to the release of the stress-engineered metallic leads. Thus, the assembly takes place while the two surfaces are flat. Once the electrical and optical interconnections are bonded to their respective locations, the release layer is removed to cause the metallic leads, and thus the chip, to spring off the surface of the board.

Note that in the previous discussion, the words input/output (I/O) were not used when describing the third generation of SoL. The reason for this is that the projected vision for the third generation of SoL is one that merges the functionality of the I/Os with the board-level interconnections. As a result, the I/O interconnection level is essentially eliminated, or at least, becomes difficult to distinguish from the rest of the interconnections.
Figure 8.8: Schematic illustrating a bidirectional optical interconnection between the chip and the board. This structure resembles a three-dimensional microphotonic funnel.

Figure 8.9: One of the possible variations to the structures described previously. The cladding may or may not be elevated with the core: the core may have an all air cladding once released from the surface.
8.2.2 Fabrication

The fabrication process of the curved off-surface optical waveguides is based on the fabrication process of the stress-engineered metallic leads. The following is one potential fabrication method: first, a release layer and a stress-engineered thin film metal are deposited and patterned as described previously. These steps are shown in Figure 8.10b. Next, the optical waveguide cladding layer is deposited, as shown in Figure 8.10c. This layer can be either organic or inorganic. When necessary, it can also be used as a planarization layer. Next, the polymer waveguide core is deposited and patterned into the desired shape. This is illustrated in Figure 8.10d. While the waveguide core is shown as a flat layer, the core can be fabricated such that it tapers in height and width. This can be accomplished through polymer molding or the use of a grey scale photodefinae polymers and grey scale masks. Once the release layer is etched or thermally decomposed (Figure 8.10e), the polymer/metal lead curves off the surface.
Figure 8.10: Fabrication of a polymer waveguide on a stress-engineered metallic interconnect. (a) Wafer/substrate on which the interconnections will be fabricated upon. (b) The release layer and the stress-engineered thin film metal are deposited and patterned. (c) Waveguide cladding is deposited. (d) Waveguide core is deposited. The core and the cladding are patterned. (e) The release layer is etched causing the metallic lead and the optical waveguide to spring off the surface.
8.3 Conclusion

This chapter introduced new I/O interconnect configurations that when experimentally demonstrated and rigorously modeled can form the basis of a third generation of Sea of Leads (SoL). Unlike the other chapters in this thesis, no measured results were reported. As a result, this chapter represents an extensive discussion of future work and future prospects of SoL. The principal idea presented in this chapter is to fabricate an off-surface curved microphotonic interconnect to enable chip-to-chip optical communication using a single waveguide. The use of a microphotonic funnel can provide spatial matching between the dimensions of an on-chip optical source/detector and the dimensions of a board-level single mode plasor waveguide. Promising methods of fabricating and assembling such interconnect structures were also described in this chapter.
Chapter 9

Conclusion and Future Work

This chapter begins by first listing the key results and contributions in each of the three generations of Sea of Leads (SoL) I/O interconnection technology. Future work and possible extensions of the research presented in this thesis are described in the second part of this chapter.

9.1 Conclusion

The following sections summarize the key results in each of the three SoL technology generations in bullet format.

9.1.1 First Generation Sea of Leads

- A SoL chip with 12,000 compliant leads distributed across a 1 cm x 1 cm area was fabricated. The leads were oriented approximately perpendicular to the contours of chip expansion to increase their compliance. In order to increase the I/O density, longer leads were fabricated at the edges of the chip, and shorter leads were fabricated at the inner region of the chip.
- Methods of fabricating vias using photodefinition and reactive ion etching (RIE) using the polymer Avatrel 2000P were described. Plasma etched vias attain the most desirable attributes: positively sloped sidewall angles, rough sidewalls, and a fabrication method that is not dependent on via aspect ratio.

- Methods of fabricating partially adhered, or slippery, leads were introduced. Such leads provide higher compliance when compared to adhered leads.

- Metallic leads with polymer backbone were introduced and fabricated. Such leads potentially provide higher compliance and provide a convenient non-wettable surface for solder.

- Compliant leads on tall (>30 μm) embedded air gaps were fabricated.

- Optical polymer waveguides were fabricated within a SoL chip.

- The compliance of polymer films with and without embedded air gaps were compared. It was shown that the embedded air gaps dramatically increase compliance. It was also shown that metal on the surface of the overcoat polymer degrades the mechanical performance of the embedded air gaps.

- High frequency electrical measurements were made to gain some insight into the high-frequency behavior of the compliant leads. The leads exhibit flat frequency response from 5 GHz to 40 GHz.

- An analysis describing some of the concerns with the distribution of high dc current through the leads was presented. The primary concern was how much chip surface area can be devoted to the power and ground pads. This will determine the current density per lead. Solder bumps were identified as one of the primary
bottlenecks for high current density distribution per lead because of their poor electromigration properties.

- The fabrication of SoL chip I/O interconnections on an Intel chip at the wafer-level was described. Some of the problems encountered during the process integration were also described.

9.1.2 Second Generation Sea of Leads

- Sea of Polymer Pillars (SoPP) was introduced.

- Methods of using the polymer pillars for electrical, optical, and RF I/O interconnections were described. The use of microfluidic, or thermal, I/O interconnections integrated with the polymer pillars was also introduced.

- The use of a single polymer pillar for simultaneous electrical and optical interconnections was introduced. Such a structure is called a dual-mode polymer pillar.

- The polymer pillars yield compliant optical I/O interconnections that maintain optical alignment between the chip and the board during thermal cycling.

- The fabrication process of high aspect ratio polymer pillars that exhibit vertical and smooth sidewalls was developed: the polymer pillars are photodefined using the polymer Avatrel 2000P.

- The fabrication of polymer sockets to ultimately hold and align the polymer pillars to the module/board was demonstrated.

- The fabrication of polymer pillars on mirrors and volume grating couplers was demonstrated.
• Polymer pillars with lenses and mirrors on their tips were fabricated.

• Methods of fabricating polymer pillars with any tip surface topology were demonstrated. The polymer film can be molded/stamped with the desired surface topology prior/following photodefinition. In addition, the polymer pillars can be directly fabricated on a template with the inverse pattern of the desired surface topology followed by the flip-pillar attachment of their tips to another substrate. This finally yields polymer pillars with tips resembling the inverse pattern of the mold.

• Polymer pillar microindentations were reported. The out-of-plane force – displacement characteristic curves were analyzed. The mechanical characteristics of the pillars were shown to be a function of the cure conditions. The approximate compliance of the cured polymer pillars was 0.15 μm/mN. Indentation of polymer pillars with sidewall metallization was shown to cause the metal to plastically deform and delaminate as the polymer pillars underwent large compression.

• The lateral force-displacement characteristic curves of the polymer pillars as a function of aspect ratio, cure conditions, and sidewall metallization were reported. The compliance of the tested polymer pillars was in the range of 2-6 μm/mN.

• Simple optical measurements that demonstrated the optical interconnection capability of the polymer pillars were reported. The ability to couple light out of a polymer pillar using a mirror on its tip was demonstrated.

• The allowable temperature conditions that the polymer pillars can be exposed to were described. The polymer pillars melt and thermally decompose at
temperature substantially higher than the glass transition temperature ($T_g$) of the polymer.

- The fabrication of polymer pillars on the active area of symmetric Si (Group IV) MSM photodetectors was demonstrated.
- The optical-electrical characteristics of the MSM photodetectors with and without polymer pillars were reported.

9.1.3 Third Generation Sea of Leads

- Opportunities of fabricating a stress-engineered metal/non-organic film below a polymer waveguide was described. Such a structure resembles a curved off-surface optical I/O interconnection.
- The fabrication of curved off-surface optical waveguides enables the uninterrupted optical signal propagation from the board to the chip and ultimately chip-to-chip. This represents a true single waveguide chip-to-chip optical interconnect communication network. While mirrors and grating couplers can be process integrated, they are potentially not needed.
- The use of a three-dimensional microphotonic funnel to mitigate the spatial transformation between the chip-level optical sources and detectors and the board-level single-mode planar waveguides was described.
9.2 Future Work

9.2.1 Assembly and Reliability Testing

The reliability of all interconnect structures must be investigated. This requires the design and fabrication of a printed wiring board (PWB) that will facilitate the routing of the I/O interconnections to the periphery of the board for testing. Some PWB layouts are shown in Figure 9.1. The left side of the layout consists of several bonding areas for SoL chips with an I/O density of 12,000 electrical lead/cm² while the right side of the layout consists of several bonding areas for SoL chips with an I/O density of -1,000 electrical lead/cm². With respect to the first generation of SoL, the reliability analysis should demonstrate the effects of lead thickness, shape, metal, and solder geometry and properties. The potential benefits of the leads with a polymeric backbone and the slippery leads should also be investigated. The reliability of SoL chips with embedded air gaps should also be examined. Not only is the in-plane reliability (the ability of the leads to undergo in-plane elastic strain) important, but the reliability of the embedded air gaps (out-of-plane reliability) is also critical: at what load conditions do the embedded air gaps begin to show fatigue. Finally, the moisture absorption of SoL interconnect structures is of prime importance.

Preliminary assembly results of electrical polymer pillars are shown in Figure 9.2. The figure illustrates an SEM micrograph of a chip with Ti/Cu (300 Å/0.2 µm) fully coated polymer pillars bonded to a glass substrate with a blanket film of Cu and solder. For clarity, Figure 9.3 is a schematic of the chip and the substrate. A higher magnification SEM micrograph of the bonded polymer pillars is shown in Figure 9.4.
Reliability testing should not be limited to the electrical interconnections. The reliability of the optical interconnections must also be investigated. While the polymer pillars are compliant polymer waveguides, it is important to understand and quantify the possible optical losses caused as the polymer pillars undergo strain. In short, it is critical to understand how an optical interconnection network that uses polymer pillars performs during thermal cycling.

9.2.2 Using Cu-to-Cu Bonding for Chip-to-Module Interconnections

A potential alternative to solder is direct Cu-to-Cu bonding. Figure 9.5 is a schematic of a Cu-to-Cu bonding process applied to a chip with polymer pillars. This process was demonstrated using low aspect ratio polymer pillars. Figure 9.6 is an SEM micrograph of polymer pillars bonded to a substrate using Cu-to-Cu bonding. The bonding process was performed at MIT [9.1]. After extensive experimentation, reliable bonding was attained when the pillars were pressed against the substrate for 16 hrs at 150°C and at a pressure of greater than 4000 mbar. Much more work is needed to make this process more practical.
Figure 9.1: PWB layouts to accommodate SoL electrical chips with densities of \( \sim 12,000 \) I/O per cm\(^2\) and \( \sim 1,000 \) I/O per cm\(^2\).
Figure 9.2: SEM micrograph of a Si chip with 110 μm tall and 55 μm wide circular polymer pillars bonded to glass substrate with a blanket film of Cu and solder.

Figure 9.3: Schematic of the assembled components shown in Figure 9.2
Figure 9.4: Higher magnification SEM micrograph of the bonded polymer pillars shown in Figure 9.2.

Figure 9.5: Schematic of a Cu-to-Cu bonding process when used with the polymer pillars [9.1].
9.2.3 Mechanical Modeling

All SoL interconnect structures should be mechanically modeled to gain more insight into their behavior. While it is known that all leads are compliant, it is still unclear exactly what the geometry of all interconnect structures should be. Moreover, it is unclear what metals should be used for the electrical interconnections. For example, while Au has a smaller Young's modulus than Cu, Au has lower yield stress. Thus, Au undergoes plastic deformation quicker, even though it is more compliant. This is potentially unacceptable for some applications.
9.2.4 Optical Modeling

It is important to model the optical transmission of the polymer pillars as a function of aspect ratio and shape. The polymer pillar's intensity patterns as a function of distance from their tip can provide valuable information about the quality of the polymer pillars as optical waveguides. Figure 9.7 is a schematic of a simple optical measurement setup used to make such measurements. Figure 9.8 illustrates the results of one such measurement using the polymer pillars fabricated in Chapter 5. The figure also illustrates the expected intensity patterns from rigorous modeling. The close agreement between the modeled and measured intensity patterns suggests that the polymer pillars are precision many-moded optical waveguides.

![Figure 9.7: Measurement setup used to measure the intensity patterns of the polymer pillars as a function of distance from the polymer pillar's tip.](image)

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9.2.5 Integrated Electrical-Mechanical-Optical Modeling

Once the I/O interconnect structures have been modeled from electrical, mechanical, and optical perspectives, it is important to combine these results to develop an integrated model. Such a model will provide a design space for the interconnections.

9.2.6 Polymer Pillar to Planar Waveguide Interconnection Modeling

The details of making an optical interconnection between a polymer pillar and a planar waveguide must be studied. There is potentially a waveguide geometrical mismatch problem between the polymer pillars and the planar waveguides. As a result, it
is important to understand how to couple light in and out of a polymer pillar using a planar waveguide. Some of the I/O interconnect configurations may work best as a unidirectional interconnect: coupling efficiency may be higher from the board-to-the-chip than in the opposite direction, for example. Optimizing the unidirectional and bidirectional interconnections by modeling the coupling elements is necessary.

9.2.7 Polymer Pillar and MSM Photodetector Testing

Much more research can be done with the integration of the polymer pillars and the MSM photodetectors. For example, demonstrating optical coupling to the detectors through sidewall metallized polymer pillars is important. In addition, successful flip-chip attachment of a chip with MSM photodetectors and electrical and optical polymer pillars onto a board with planar waveguides and electrical interconnections would represent a major result. Finally, testing the assembled electrical/optical system is necessary for a convincing demonstration of an integrated electrical-optical interconnection technology.

9.2.8 Wafer-Level Testing of all Structures

All SoL I/O interconnect structures are designed and fabricated to be compatible with wafer-level testing and burn-in. As a result, it is important to demonstrate the ability to perform wafer-level optical and electrical testing on SoL interconnections. An optical-electrical probe card has to be designed and fabricated to be compatible with SoL structures.
9.2.9 Fabrication of Surface Relief Structures on the Polymer Pills

While two fabrication methods of making surface relief structures on the polymer pillars were demonstrated, all fabricated structures in this thesis were limited to mirrors. The fabrication of slanted surface relief gratings for preferential order coupling should be pursued. Diffractive lenses, concave and convex lenses and mirrors are also of interest. Moreover, it is important to quantify the quality of the transferred surface relief pattern and thus, the molding process.

9.2.10 Polymer Sockets: Modeling and Fabrication

The polymer sockets are an important component of the overall interconnection technology in SoPP. As a result, the effects of the sockets on the optical, electrical, and mechanical interconnections should be analyzed. In addition, the fabrication of sockets with positively sloped sidewalls should be pursued. This could be accomplished by fabricating the sockets using a polymer material that undergoes shrinkage following thermal cure.

9.2.11 Polymer Pillar Metallization

Polymer pillar metallization is a non-trivial task. It is very difficult to spin coat photoresist on/around the polymer pillars. The complexity in processing skyrockets as the pitch between the pillars decreases. As a result, methods of metallizing and patterning
metal on the sidewalls of the polymer pillars with and without the use of photoresist should be investigated.

9.2.12 Out-of-Plane Microfluidic Micropipes

Preliminary structures resembling out-of-plane micropipes were fabricated. These devices can ultimately be used for microfluidic applications. The fabrication process must be refined and the structures have to be thoroughly tested. In addition, methods of bonding/attaching the micropipes to planar channels must be investigated: leakage could potentially be a concern.

9.2.13 Design, Fabrication, and Testing of the Third Generation of SoL

Some new I/O interconnect configurations that represent opportunities for a third generation of SoL were introduced. However, the structures were not modeled, fabricated, or tested. Thus, there is much work to be done in this area.

9.3 Conclusion of the Thesis

The focus of this thesis has been on the development of wafer-level batch fabrication technologies for integrated electrical and optical I/O interconnections. The global terminology used to refer to the I/O interconnection techniques is Sea of Leads
(Sol). Two generations of SoL were demonstrated and future opportunities for a third generation of SoL were described in this thesis.

In the first generation, s-like partially adhered leads with a polymer backbone laying on a polymer film with embedded air gaps were developed. Mechanical and electrical measurements demonstrating the performance of the leads were reported. Finally, SoL was process integrated with an Intel chip at the wafer level.

In the second generation, polymer pillars that simultaneously provide electrical and optical interconnections were developed. Mechanical and optical measurements were made to demonstrate the behavior of the polymer pillars. Finally, the polymer pillars were process integrated with MSM photodetectors to demonstrate an optoelectronic subsystem.

Opportunities for a third generation of SoL were also described. In addition, opportunities for integrating microfluidic surface-normal micropipes for heat removal and RF I/O interconnections with the electrical and optical I/Os were also described.
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Vita

Muhammad Bakir was born in Richmond, Virginia on May of 1978. In June of 1999, he received the degree of Bachelor of Electrical Engineering from Auburn University (Summa Cum Laude). Awards he received while at Auburn University include IEEE's most outstanding graduating senior from Auburn's ECE, Spring 1999; International Engineering Consortium's William L. Everitt Student Award of Excellence, 1999; The White Family Engineering Scholarship Endowment, 1998-1999; Engineering Dean's Honor List for ten quarters; Fred H. Pumphrey Outstanding Pre-Engineering Student Award, 1997; Phi Kappa Phi Award for most Outstanding Freshman, 1997.

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