A Wireless Neural Recording SoC and Implantable Microsystem Integration

Lian Duan, Tao Wang, Siwei Wang, Amir Yazdanbakhsh

***Abstract* — An integrated 4-channel wireless neural recording system architecture is proposed. The system was designed to detect extracellular activity potential in the brain. Highly power-efficient front-end signal processing, spike detector, analog-to-digital converter, on-chip power management system, and FSK transmitter are designed and implemented on 0.5 µm CMOS process.**

***Index Terms*—neural recording, wireless microsystem, SoC, low power, spike detector, analog to digital converter, FSK transmitter**

I. Introduction

Monitoring neural-electrical activity in human brain is seen as one vitally important technique to diagnose neuron activity-related disease, like epilepsy, schizophrenia, and Alzheimer's, as well as to provide instructions for neural prosthetics [1]. Neural recording from microelectrodes, such as Utah microelectrode arrays, allows for acquisition of wider-bandwidth neuron activity signals, knows as neural spikes ranging until 7 kHz [2]. The amplitude of targeted extracellular activity potential (EAP) signal usually has amplitude of 50 ~ 500 µV and frequency range of 100 Hz ~ 10 kHz. Local field potential (LFP) signal frequency range is around 0.01Hz to 200Hz. [3-8]

Two mostly important technical challenges of integrated neural recording microsystem are high miniaturization and low-power consumption. On one hand, the size of the integrated microsystem should be as close as the microelectrode array for brain implanting capability. On the other hand, extremely tight power density budget is demanded to minimize excessive heat dissipation to the surrounding tissue and neurons. One solution is to divide all the system blocks into implantable and outside of the body. All the blocks inside the brain should be as compatible and power-efficient as possible, while all the outside blocks should provide the highest performance, including low-noise receiver and digital signal processing (DSP).

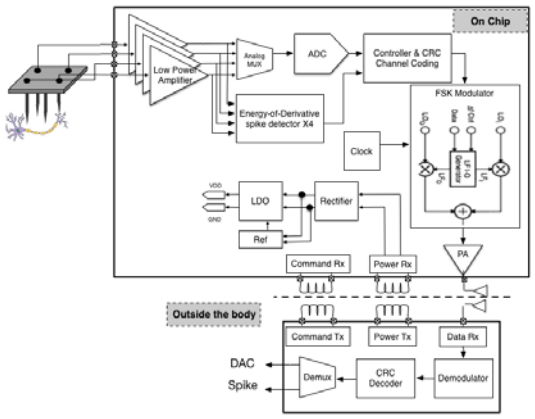

Figure 1 System Architecture

II. System Architecture

Figure 1 shows the system-level architecture of the wireless neural recording system-on-chip (SoC). All the implantable circuits were designed for low-power consumption. 2-stage low-noise amplifiers in the array of 2x2 were placed after the Utah electrode array (UEA) sensor to acquire, filter, and amplify the neural potential signals. Meanwhile, ultra-low power dissipation energy-of-derivative spike detecting circuit was designed to efficiently sample the spike signals. All the output signals after each channel were connected to an analog multiplexer which is controlled by a digital circuit. The output is fed into an analog to digital converter (ADC), followed by a wireless transmitter and sent to the off-chip antenna. The other functional circuits in the implantable SoC include inductive power receiver, command receiver, rectifier and low dropout voltage regulator to provide stable power supply and command signals.

The circuits outside the body include data Rx, clock recovery and digital processing.

A. Sensor

The Utah electrode array (UEA, *Figure 2*) is chosen as our sensor. The array is comprised of up to 96 electrodes (commercial version, manufactured by Blackrock), electrode length of 0.5mm to 1.5mm, and electrode pitch of 400µm, all in less than 5.9mm in length and width. Table 2 shows the specifications of the sensor. The sensor obtains cumulative electrical activity of its surrounding neurons.

B. Low Power Amplification

The potential that neurons generate is about 150mV. If it is detected at a distance with UEA, the voltage that can be detected is around 50 - 500µV. In order to make it suitable for spike detection and transmission, it has to be amplified to about 3V, which corresponds to about 5000 times (~74dB). We implement a two-stage low noise, low power amplifier first introduced in [4].

The specification requirements for first stage amplifier (telescopic transconductance operational amplifier) is detailed

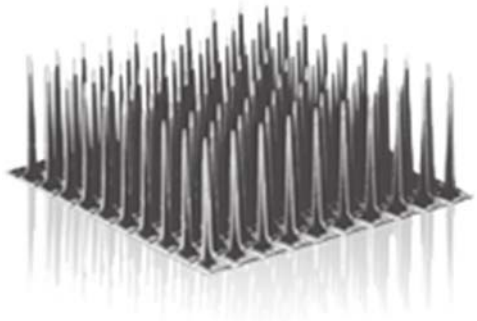

Figure 2 Utah electrode array

TABLE 1
DESIRED SPECIFICATIONS FOR LOW-POWER NEURAL AMPLIFIER

Requirement	Value
Noise (5kHz)	15μV
Bandwidth	100Hz-10kHz
Power	6μW
NEF	6dB
Area	0.04mm^2
Gain	~72dB

TABLE 2
SPECIFICATIONS FOR UTAH ELECTRODE ARRAY [4]

Requirement	Value
Channel count	> 4
Sensor size	1500μm × 750μm
Impedence	25kΩ
Electrode material	Platinum
Insulation	Parylene-C
Standard electrode lengths	0.5 - 1.5mm
Standard electrode pitch	400μm

TABLE 3
SPECIFICATIONS FOR SPIKE DETECTION ALGORITHMS

Parameters	NEO	fNEO	ED
STD	0.0965	0.0592	0.0669
PCR	0.963	1.134	1.128
Power Consumption (nW)	250	260	129

in a later section. The second stage is comprised of a voltage amplifier with larger output swing. Since the input signal voltage for the second stage is higher than the first stage, it is less sensitive to noise. The desired specification for the entire two-stage neural amplifier is detailed in Table 1. Chip size, power consumption, bandwidth and noise factor need to be balanced in the design.

Compared with other transconductance amplifiers, the telescopic transconductance amplifier based neural amplifier has benefit of significantly lower chip area and lower power at the expense of slightly increased noise efficiency factor (NEF).

C. Spike Detection

Spike detection is critical to neural sensor in the sense that for modern neural system processors, simultaneous acquisition of channels of up to 256 has been reported, but it is not possible to transmit all these channels in full resolution at the same time. Spike detections allows neural scientists to find channel of interest and get full resolution ADC output.

Several spike detection topologies have been proposed, such as the conventional nonlinear energy operator (NEO), frequency-enhanced nonlinear energy operator (fNEO), and energy of derivative (ED). The parameters of these three topologies are compared in Table 3. In light of the comparison, energy of derivative spike detection suits our need best, providing adequate spike detection efficiency while reducing power consumption by more than a half.

D. Analog-to-Digital Converter

An analog to digital converter is incorporated on-chip to convert amplified signal to digital domain and then sent off-chip using RF transmission. The design goal is an 8-bit ADC at 100 kHz sampling rate. ADC works in parallel with spike detector to capture the characteristic of neural signal. The user is allow to choose a channel using external control which is enabled by an analog multiplexer. Using successive approximation register (SAR) architecture ADC with embedded charge redistribution DAC, a fully functional ADC is implemented and simulated using SPICE.

E. Power Management

As shown in the *Figure 1*, the overall power was supplied by an inductive power receiver, receiving energy from the outside. Off-chip inductive and capacitive elements were needed to provide the chip with energy, the power carrier frequency of which is 12.32MHz. This frequency was chosen for two reasons, one of which was within the 1 MHz~20 MHz acceptable range for implantable microelectronic devices (IMD)[10]. While the other one was slightly larger than 10MHz, above which tissue absorption will not be acceptable.

After the power receiver block, there follows a full-bridge voltage rectifier, changing the AC voltage to DC. A low dropout voltage regulator (LDO) provided a regulated 3.3V supply to the chip. Besides, there should also be a precise voltage reference, which is fed by the output of the rectifier, to provide reference voltage to LDO. The regulator is evaluated by two main parameters, load regulation and line regulation. The former one indicates that how much the output voltage will change when the load current is changing, while the latter shows that how much the output voltage will change when the supply voltage changes.

F. RF Transmission

One technical challenge of data transmitter design is how to implement low-power circuits meeting up required data transmission rate. The project targets to solve the wireless data transmission rate of 800 kbps, in which quadrature FSK up-conversion is utilized. The FSK transmission module includes a voltage controlled local oscillator generating quadrature oscillating signals in the frequency of 433 MHz, a digital quadrature baseband modulator, two up-conversion mixers, and a power amplifier targeted to deliver a wireless signal having the intensity of 0 dBm. The modulating frequency was selected to be 433 MHz, which is the closest to the Industrial, Scientific, and Medical (ISM) band to the FCC-approved Medical Implant Communications System (MICS) band at 402~405MHz.

Meanwhile, a high-frequency transmission makes small antenna design possible.

III. Circuit Design

A. *Low-Power Amplifier*

Many amplifier topologies have been proposed as the first stage of neural amplifier because of its stringent power and noise requirements. Differential amplifier with current mirror load is widely used, but it poses a tradeoff between low power and low noise which is sometimes very difficult to decide. Using telescopic amplifier for the first amplification stage has been proposed in [3]. It exploits the fact that differential amplifier with current mirror has a large output voltage swing and input common mode range that is not required for the first amplification stage. By using telescopic amplifier, input and output voltage range is traded for high voltage gain. The circuit used is show in *Figure 3*.

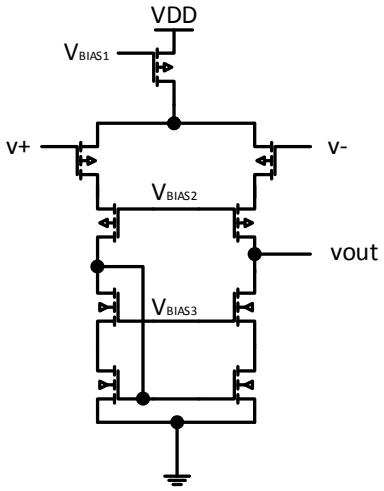

Figure 3 Telescopic amplifier schematic

The amplifier was put to test in a closed-loop testing circuit with the gain set to be about 40dB. A low pass filter is also incorporated into the feedback such that the cutoff frequency is about 30 kHz. Since the input is a differential signal, a capacitor feedback circuit with switch-based biasing is implemented. The testing circuit is shown in *Figure 4*, and the Bode plot is shown in *Figure 5*.

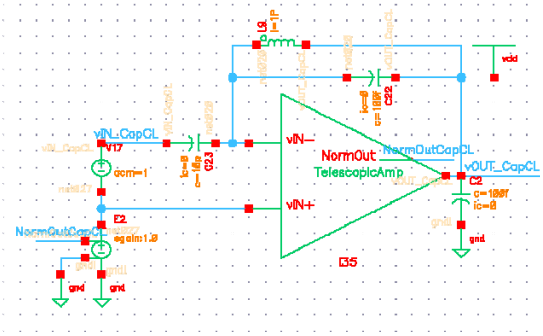

Figure 4 Testing circuit for telescopic amplifier.

TABLE 4
SPECIFICATIONS FOR LOW-POWER NEURAL AMPLIFIER

Requirement	Value	[4]
DC Gain	90dB	88dB
Unity Gain Frequency	5MHz	106.4kHz
Total Bias Current	1.3uA	1.4uA
Input-Referred Noise	140nV/ √ Hz	52.7nV/ √ Hz
Supply Voltage	3.3V	3V

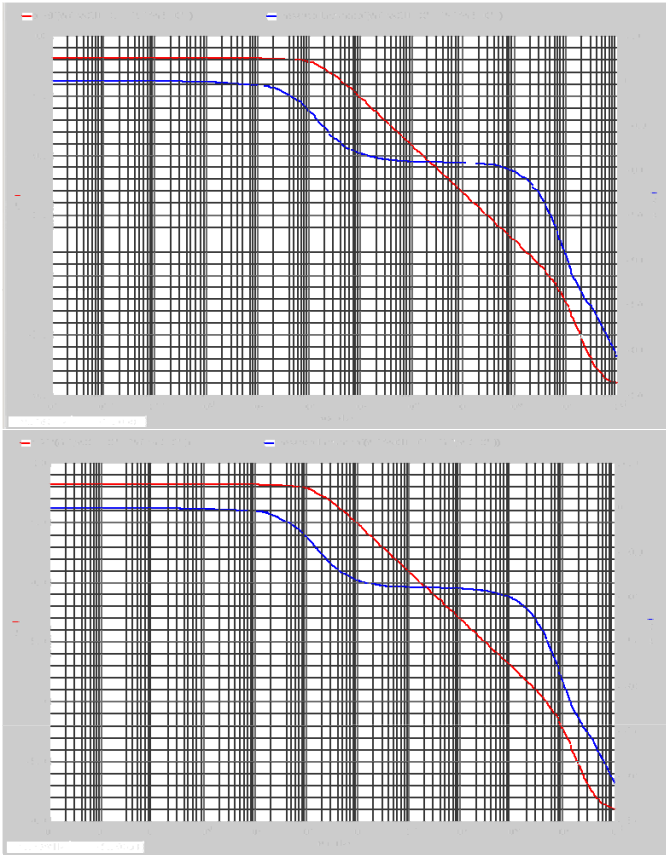

Figure 5 Bode plot of open and close loop telescopic amplifier.

The parameters of the telescopic amplifier (open loop) are shown in Table 4. When compared to state-of-the-art implementations, there are still room for improvement. Careful tuning of transistor W/L ratio is still necessary to better fit the ON-Semi 0.5um process.

The second stage of the neural amplifier is comprised of a standard differential amplifier loaded with current mirror and a common source amplifier. The close loop Bode plot is shown in *Figure 6*.

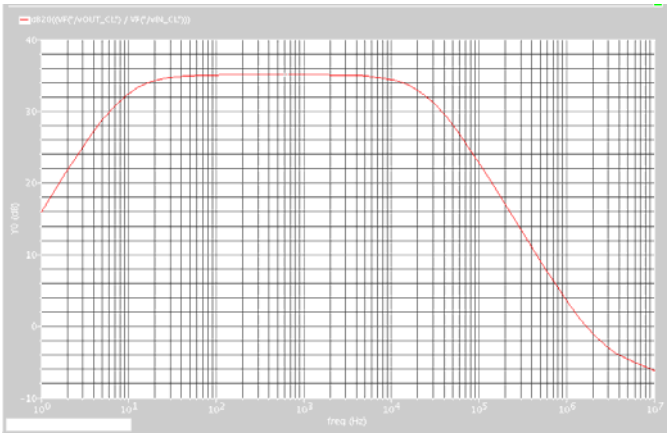

Figure 6 Close loop bode plot of differential amplifier

Combining the stage 1 telescopic amplifier and stage 2 differential amplifier, we can obtain a neural amplifier with 75dB gain (~5623V/V), amplifying input from 50uV ~ 500uV to approximately 281mV ~ 2.81V, which is close to our full ADC range, with some headroom left in case input signal goes beyond expected values.

B. Analog to Digital Converter

There are several ADC architectures that can be chosen from, including flash ADC, integrating ADC and successive approximation ADC. Flash ADC is relatively fast, but it consumes more power. Integrating ADC is more power efficient and accurate, but it has limited speed. If we want to achieve sampling rate of 100kS/s, the clock speed needs to be higher than 25MHz. To achieve an optimal tradeoff between power and speed, the successive approximation architecture ADC was chosen here, in which an embedded charge redistribution DAC is required. The output of DAC is buffered with a rail-to-rail input operational amplifier with a cut-off frequency of approximately 1 MHz at unity gain.

The clock scheme of the ADC is described as follows. Two signals are required to drive the ADC: enable and clock. When enable is high, the ADC is in quiescent state. When enable signal is driven low, the ADC is powered on. After 9 clock cycles, the output of the ADC are latched into the output. 9 clock cycles are required for each conversion (including the first conversion after enable), and no additional clock cycles is required between subsequent conversions.

The schematic of the ADC is shown in *Figure 7*.

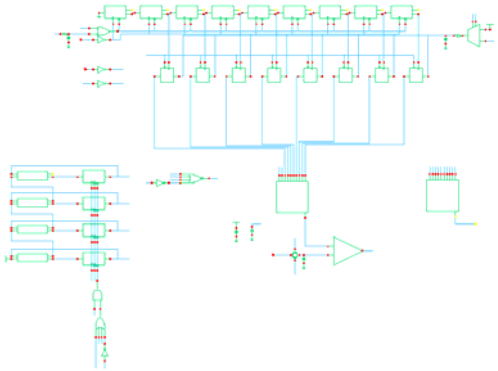

Figure 7 ADC Schematic

Simulation output in *Figure 8* showing a sinusoidal input being sampled using this ADC and regenerated using another DAC.

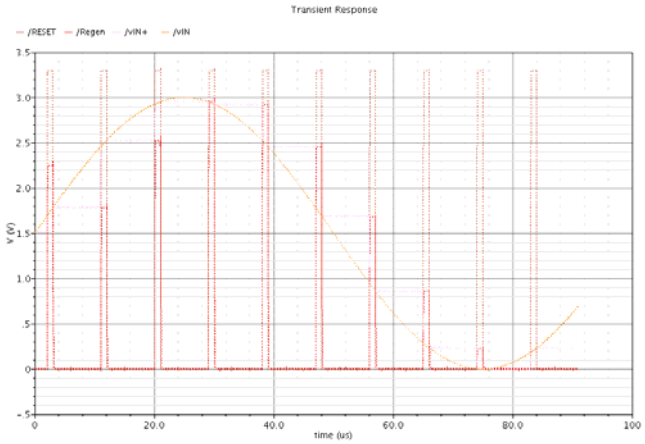

Figure 8 ADC sinusoid regeneration

The SPICE simulation results of the ADC are listed in Table 5.

TABLE 5
PERFORMANCE OF ADC

Metric	Value
Bits	8
Reference Voltage	3V
Input range	0V – 3V
Maximum Sampling Rate	100kSamples/s
Current consumption	500uA
Supply Voltage	3.3V

C. Power Management

Transmitting power via a wireless power transfer (WPT) system was first raised by Nikola Tesla 100 years ago [11]. But not until 2007, when MIT yielded significant improvements in transmission efficiency by employing the electromagnetic coupled resonance system (ECR) [12], was this topic further developed. Compared with the conventional induction system, the ECR system features extremely high transmission efficiency and extends the transmission distance more than 10 times by using resonance between the transmitting and receiving coils, in which the coupled mode theory (CMT) is applied [13].

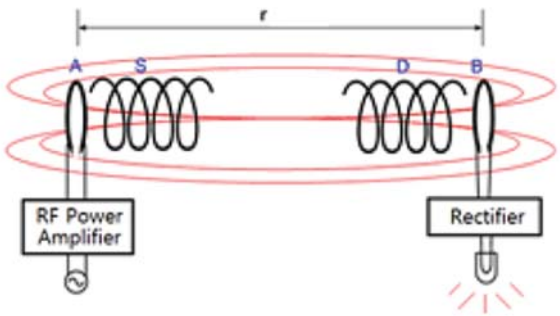

Figure 9 WPT system using ECR method

Figure 9 shows a simple structure of the ECR wireless power

transfer system. The RF power amplifier [14] amplifies the high frequency of 12.32 MHz and sends it to the power transmitting antenna (A). The power signal generated from the transmitting antenna (A) is delivered to the power receiving antenna (B) while the transmitting coil (S) and the receiving coil (D) are mutually resonated. The power received to the antenna (B) is converted into DC by the rectifier and works as the operating power supply for the low-dropout voltage regulator. *Figure 10* illustrate the whole power management system block in this design.

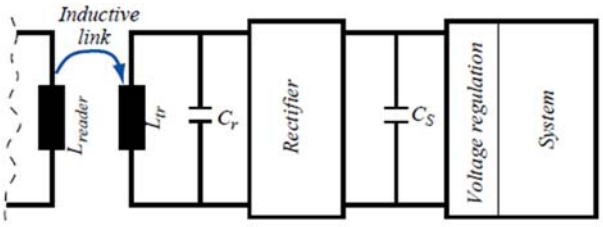

Figure 10 Schematic of a telemetric powered transponder

Lr and Cr, which are off-chip, make up the resonant circuit that receives power from the RF power amplifier. After that, the rectifier and the storage capacitor Cs offer an unregulated DC voltage. At last, a low dropout voltage regulator with 3.3V DC power supply was generated.

1) Rectifier

The rectifier proposed in this paper uses a simple negative voltage converter (NVC) that converts the negative half of the input wave into positive, as shown in *Figure 11*. This output wave can be regarded as a DC voltage and the value of Vdc can be derived from the following equation.

$$V_{dc} = \frac{2 \times V_{max}}{\pi} = 0.637 \times V_{max}$$

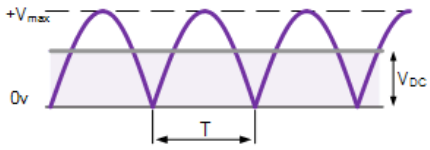

Figure 11 Equivalent DC output

To further smooth the DC output voltage, the rectifier was followed by a storage capacitor Cs. Since the Cs was typically at the level of μF, it is implemented off-chip. The output waveform is illustrated in *Figure 12*.

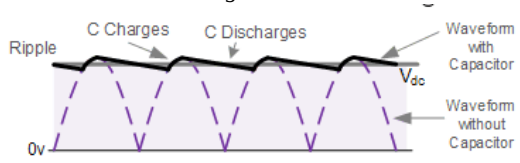

Figure 12 Capacitor followed by NVC

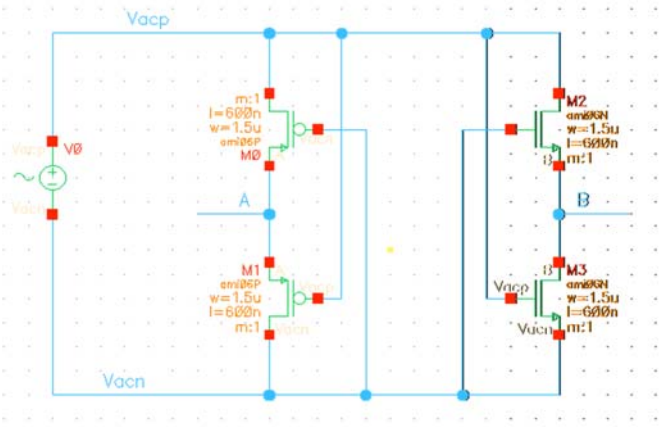

Figure 13 Circuit diagram of the negative voltage converter.

Figure 13 is a diagram of the NVC. It is the simplest circuit, in which the PMOS in the left part always deliver the higher potential to port A while the NMOS counterparts deliver the lower the potential to port B.

In this application the minimum length and width of the MOSFET was chosen to be L = 0.6 μm and W = 1.5μm. Considering the voltage regulator in the next stage gives an output of 3.3V, the output of the rectifier should be higher than 3.5V. Hence, 12.32 MHz AC voltage with 5.4V magnitude was used in simulation. The V_{DC} output in *Figure 14* shows that V_{DC} is about 3.75V.

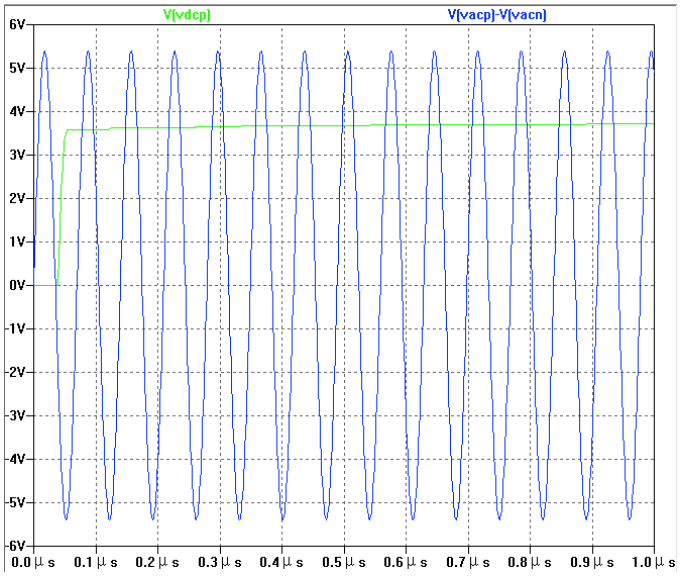

Figure 14 Transient response of rectifier

2) Low Dropout Voltage Regulator (LDO)

The input power supply is a slightly varying unregulated voltage at about 3.75V that comes from the rectifier. With a band-gap voltage reference, which will be discussed later, the output voltage is regulated to 3.3V.

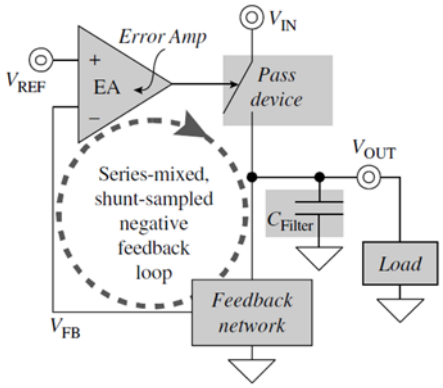

Figure 15 LDO block diagram

The typical LDO block diagram is shown in *Figure 15*, and *Figure 16* shows the realization of it. The pass device is usually a PMOS, which can lower the dropout voltage.

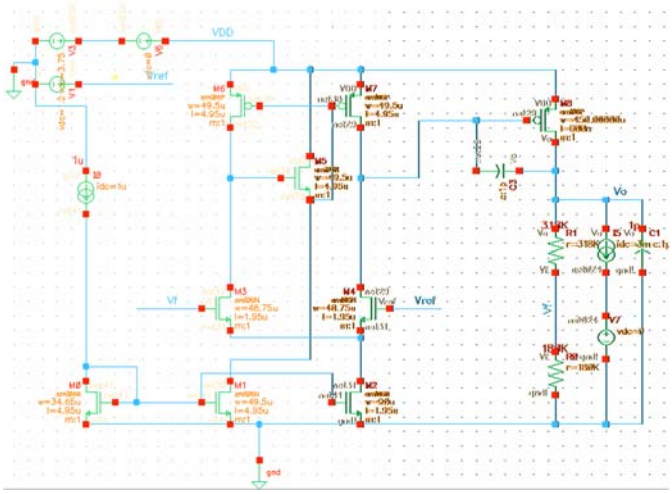

Figure 16 Circuit diagram of a LDO

Using LTSpice to simulate the load regulation and line regulation of the designed LDO. The result is shown in *Figure 17* and *Figure 18*.

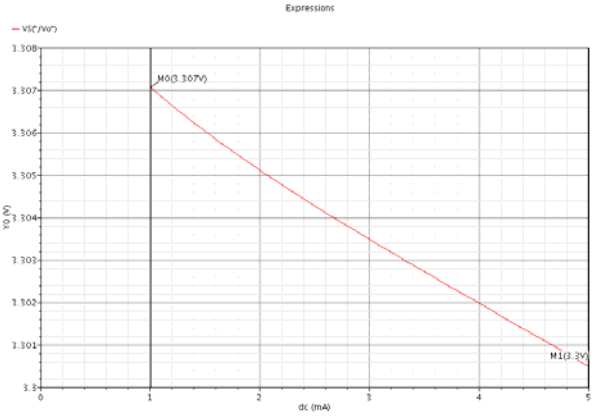

Figure 17 Load regulation of the LDO

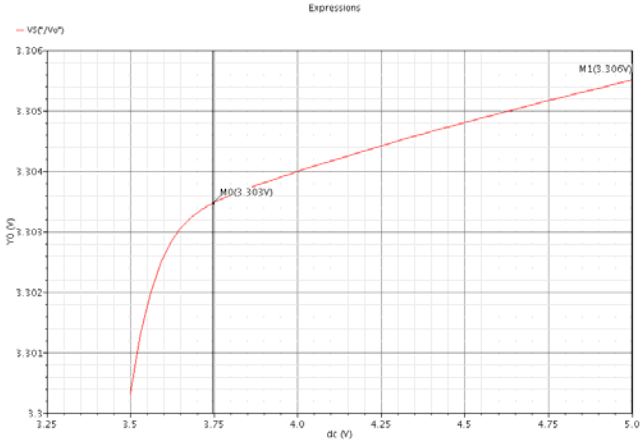

Figure 18 Line regulation of the LDO

Since the targeting whole power consumption of this design was less than 5mW, the maximum load current of the LDO would not excess 2mA. *Figure 17* shows when the load current varies from 1 to 5 mA, the load current changes from 3.307V to 3.3005V.

Similarly, the input voltage changes from 3.75-5 V, *Figure 18* illustrates the line regulation in this condition. The output voltage increase from 3.303 V to 3.3006V.

The parameters of the LDO are list in Table 6. Compare with the state-of-art, it is suitable for this design.

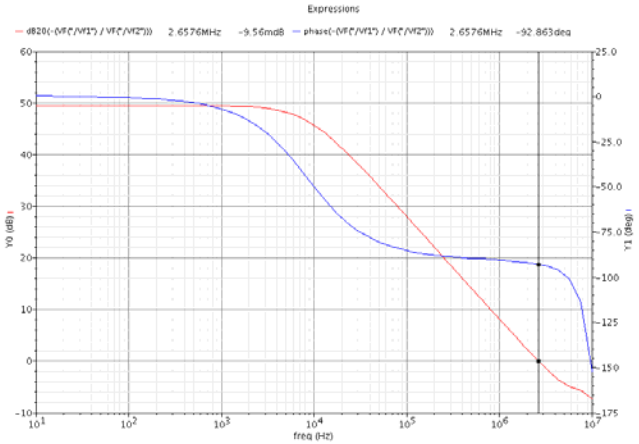

Figure 19 Open loop response

TABLE 6
SPECIFICATIONS FOR LDO

Parameters	[9]	[5]	This Work
load (mA)	NA	2-10	1-5
Vin for LDO (V)	3-4	3.5-8	3.4-5
line regulation	NA	0.3%	0.2%
load regulation	NA	0.15%	0.2%

Figure 19 shows the open loop gain of the LDO. When at the 0dB frequency, the phase shift was -92.8 degree which means that the phase margin of this circuit was almost 90 degree and it was extremely stable. *Figure 20* shows the transient response of the system. The settling time was 0.628us.

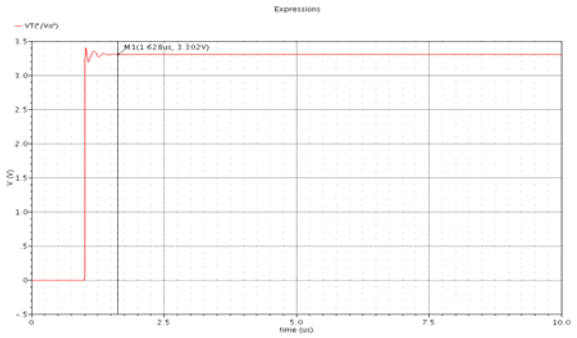

Figure 20 Transient response

3) *Voltage Reference.*

To make LDO work properly, a stable voltage reference should be carefully designed. It must be extremely stable no matter how the input voltage or the temperature changes.

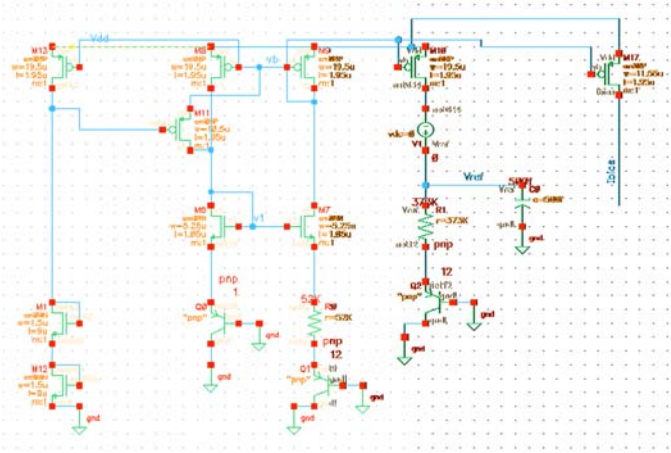

Figure 21 Circuit diagram of a BGR

Figure 21 is a circuit diagram of band-gap voltage reference (BGR) formed by using CTAT and PTAT reference. When designed properly, the temperature coefficient (TC) of the BGR can be very small. However, temperature is not a critical criterion here because the temperature inside the human body is always 37.5 ℃. The main concern is that the BGR is required to work at a quite low voltage, before all other blocks.

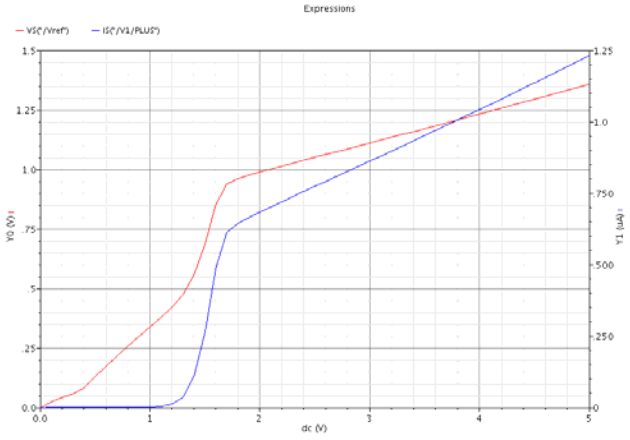

Figure 22 Reference voltage and bias current output

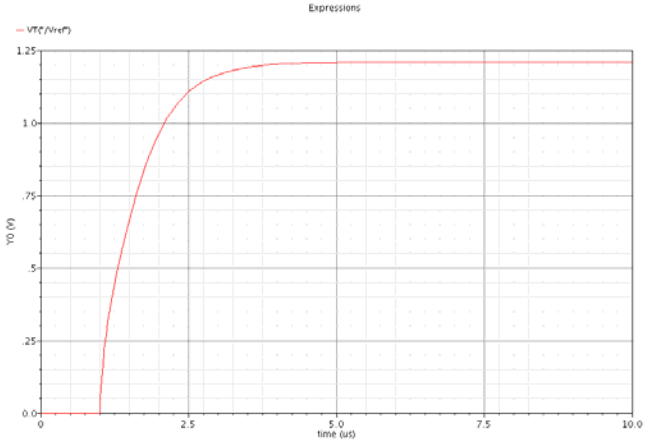

Figure 23 Transient response of BGR

From the transient response above, it can be seen that the settling time (95%) was approximately 2.5µs with steady state output of 1.2025V. A 1µA bias current was also produced using this circuit.

D. *RF Transmitter*

Figure 24 shows the block schematic of the FSK transmitter architecture used in this wireless neural recording system. The frequency synthesizer signals LO_I and LO_Q are generated by an on-chip quadrature voltage oscillator which is not shown in the graph. LF I-Q generator acts as the digital baseband modulator with inputs of shift controlling frequency Δf and data from the CRC channel coding output, and outputs of LF_I and LF_Q which are frequency shift keying modulated quadrature low-frequency data signals. Two mixers on top and bottom of the block schematic provide up-conversion of both LF signals to be transmitted into the input of power amplifier. To make sure low-power consumption and high amplitude gain, the power amplifier utilizes three-stage amplification. Below describes each module separately in detail.

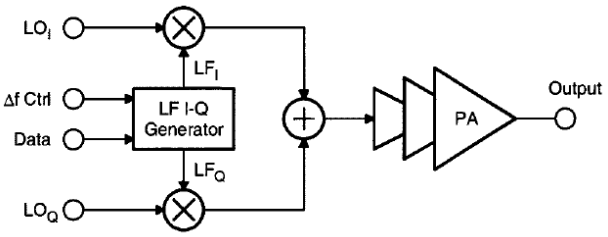

Figure 24 Block schematic of the transmitter section [16]

1) *Local Oscillator*

The quadrature oscillator was used to generate quadrature I/Q oscillating signals at 433 MHz. Two identical oscillators were coupled such that they operated in quadrature. The coupling factor between the two identical oscillators was -1, or can be named as anti-phase coupling. From the feedback model of two coupled oscillators, the output signals from the two oscillators had 180º phase difference.

The circuit of one voltage-controlled ring oscillator generating 433MHz oscillating signals is shown in *Figure 25*. Parasitic capacitors enabled by voltage-controlled varactors were inserted between each stage of inverter to control the time

delay for each round. The oscillating frequency tuning plot with the controlled voltage is shown in *Figure 26*. At the control voltage of 0.76V, an oscillating frequency of 433.0 MHz can be achieved. And the oscillating voltage signals are shown in *Figure 27*.

To address the concern that less than ideal consistency of oscillation between chips, a phase locked loop with tuning bandwidth larger than the possible frequency span across chips can be implemented to demodulate the RF signal. The cut-off frequency of loop filter in the phase locked loop should be larger than the bit rate of transmission, which is relatively easy considering the low data rate transmitted from this chip.

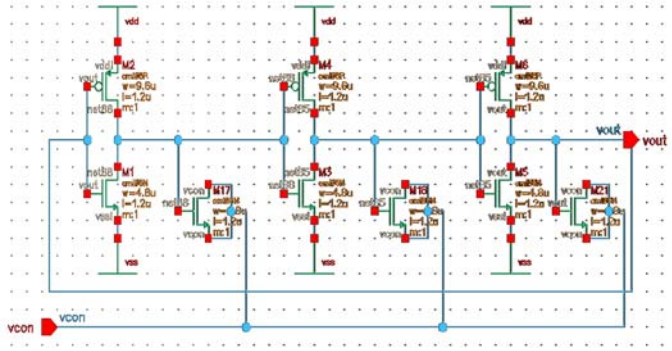

Figure 25 Circuit diagram of voltage-controlled local oscillator

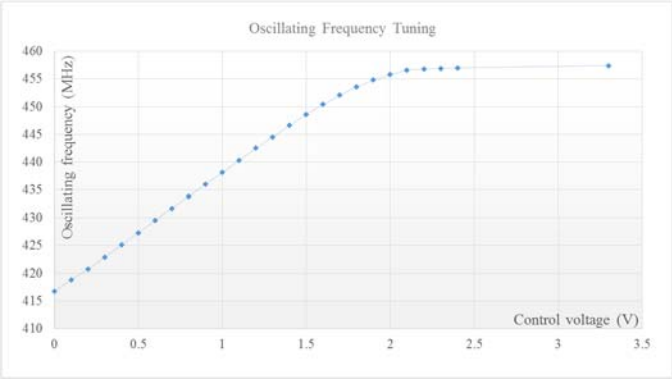

Figure 26 Oscillating frequency tuning plot with control voltage

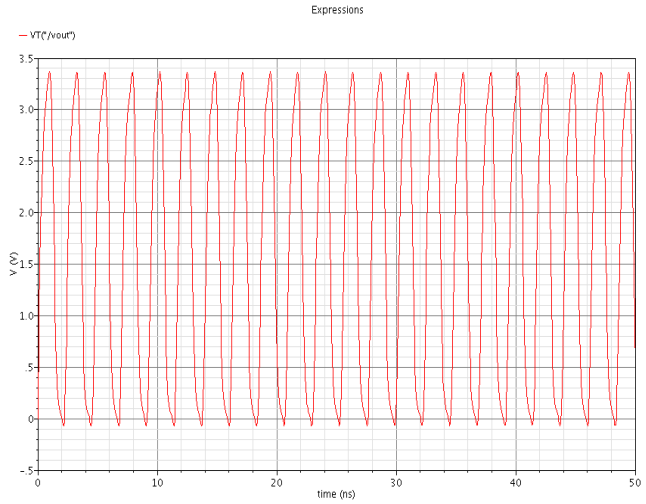

Figure 27 Oscillating voltage signals at a frequency of 433 MHz

2) *Upconversion Mixer*

Figure 28 shows the circuit diagram of the differential up-conversion mixer. The up-conversion mixer utilizes modulated bias current signal $I_{LF,I}$ and $I_{LF,Q}$ which are the output transconductance of the I/Q baseband modulator. LO signals are directly connected to the gates of transistors to up-convert the LF-range modulated current signals into RF-range FSK modulating signal. Differential topology is used to cancel the even-order harmonics. The transistors should operate between moderate and strong inversion mode to make sure a proper operation at 433 MHz, in which about 100 mV gate overdrive voltage is required (refer to Baker's book, table 9-1). The transistor's active area should be large enough to make sure the gain difference between I transistor and Q transistor is small enough, like within 3%. Simulation will be done to calculate the required transistor size (W/0.5um) and total current consumption.

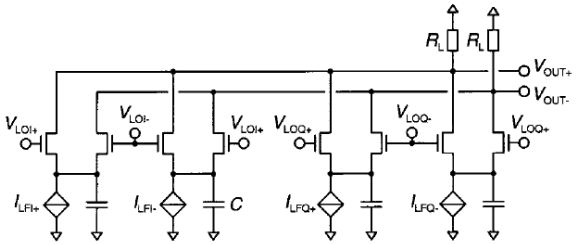

Figure 28 Circuit diagram of the up-conversion mixer [16]

3) *Power Amplifier*

The power amplifier should provide a high input impedance to exceed the maximum load of the up-conversion mixers, and also deliver an output power of 0 dBm at 433 MHz. Differential topology is also utilized in the power amplifier to cancel the even-order harmonics. In addition, only the final stage requires large inductor which can be placed externally. The preamplifier is designed to be fully integrated on chip.

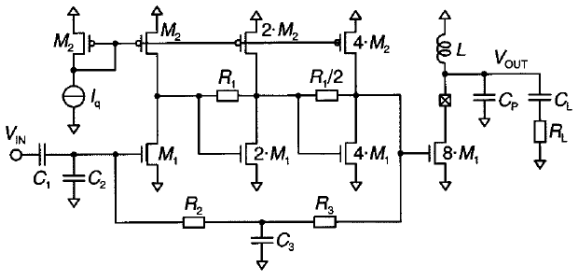

Figure 29 Circuit diagram of the power amplifier [16]

Here, a pseudo-differential circuit was chosen, composing a three-stage class-A preamplifier and an output class-B stage. The input signal from the output of up-converting mixer is ac coupled to first-stage transistor gate of the preamplifier through capacitor C_1 which also includes a parasitic capacitor C_2 at the bottom plate. The cutting-off frequencies of all the three stages were designed to be higher than 433 MHz, like 600 MHz with a moderate gain of 10 dB.

The output class-B stage has a theoretical power efficiency of 78.5%. Maintaining the supply voltage equals to 1.2 V, simulate the efficiency of the output stage with the value of load resistor R_L to find out the optimum point of highest power efficiency.

Simulate the operating of both the preamplifier and the output amplifier to figure out the transistor sizes (W/0.5um, 2W/0.5um, 4W/0.5um, and 8W/0.5um), and also the total

current consumption. *Figure 30* shows the simulating results of the voltage gain. The output power

Pout = 78.5% * 3.3 V * 554 uA = 1.44 mW = +1.58 dBm

And the power efficiency:

η = 78.5% * 554uA/1.25mA = 34.8%

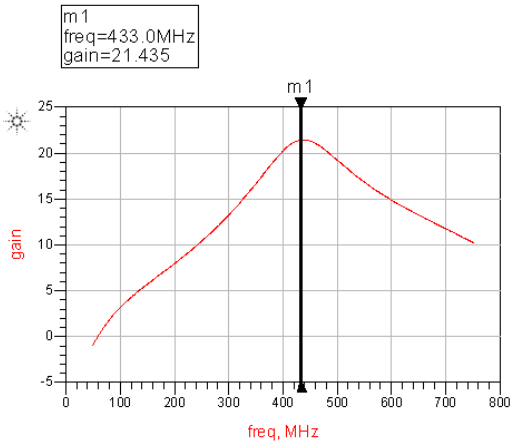

Figure 30 Voltage gain of the power amplifier

E. Spike detector

Energy derivative algorithm was used for the spike detector. The simulated output of the spike detector can be shown in *Figure 31*.

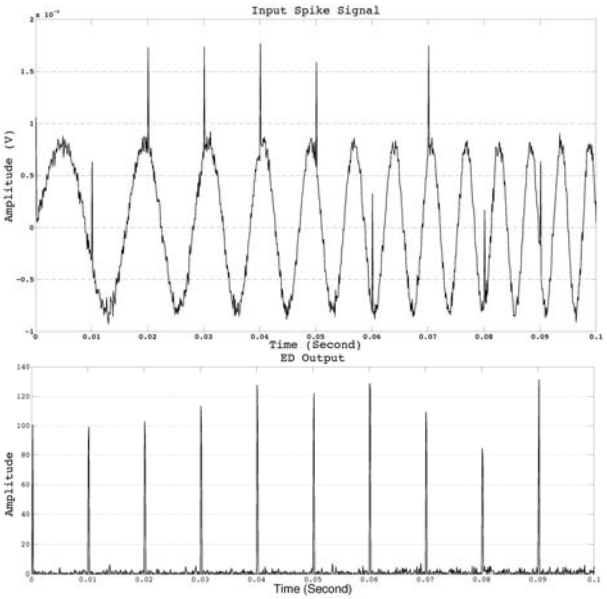

Figure 31 Spike detector simulation

F. Layout

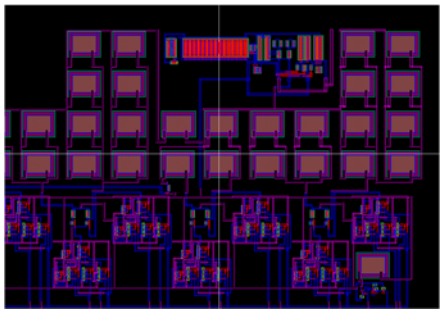

Figure 32 Layout of DAC

Layout for the DAC used in the SAR architecture of ADC and the ring oscillator are shown in Figure 32 and Figure 33 respectively. Simple matching techniques have been used.

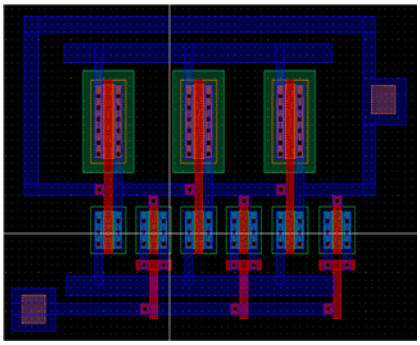

Figure 33 Layout of ring oscillator

IV. Task Division

All the team members had multiple discussions and enough collaboration all through the project. Ideas were exchanged thoroughly. Given the system requirements or all the blocks shown in the system architecture in *Figure 1*, each individual member has been assigned a portion based on his interest.

- Siwei Wang: front-end amplifier and analog to digital converter.
- Tao Wang: local oscillator, power amplifier, and physical design and realization of the entire implantable microsystem.
- Lian Duan: inductive power receiver, rectifier, bandgap reference, bias current source, and voltage regulator.
- Amir Yazdanbakhsh (auditing): ED spike detector and comparator.

V. Benchmark with State-of-The-Art

TABLE 7
COMPARISON WITH STATE-OF-THE-ART

Parameters	Harrison 2007 [5]	Genov 2009 [4]	This Work
Power	13.5mW	3.8mW	<8mW
Supply Voltage	3.3V	3V	3.3V
Year of Publication	2007	2009	2014
Channels Recorded	100	256	4
Dimmension	4.7×5.9 mm^2	3.5×4.5 mm^2	1.5×0.75 mm^2
Telecomm. Method	FSK	None FSK in 2013	FM/FSK

VI. Future Work

In order to improve the design of this chip, lower input referred noise of neural amplifier is desired. Resonance based wireless power transmission can be implemented for higher efficiency. Lower power consumption can be achieved using class C power amplifier in the FSK transmitter because currently it is the main bottleneck in terms of power consumption.

VII. Acknowledgement

We would like to thank the guidance and suggestions from Professor Maysam Ghovanloo all through the project. In

addition, all the other people who contributed to this project are appreciated.

REFERENCES

[1] Karim Abdelhalim, "915-MHz FSK/OOK Wireless Neural Recording SoC With 64 Mixed-Signal FIR Filters", JSSC, October 2013.

[2] M. Mollazadeh, K. Murari, G. Cauwenberghs, and N. Thakor, "Micropower CMOS integrated low-noise amplification, filtering, and digitization of multimodal neuropotentials," IEEE Trans. Biomed. Circuits Syst., vol. 3, no. 1, pp. 1–10, Feb. 2009.

[3] B. Gosselin "Recent advances in neural recording microsystems", Sensors, vol. 11, no. 5, pp.4572 -4597 2011

[4] Aziz, J.N.Y.; Abdelhalim, Karim; Shulyzki, R.; Genov, R.; Bardakjian, B.L.; Derchansky, M.; Serletis, D.; Carlen, P.L., "256-Channel Neural Recording and Delta Compression Microsystem With 3D Electrodes," *Solid-State Circuits, IEEE Journal of* , vol.44, no.3, pp.995,1005, March 2009

[5] Harrison, R.R.; Watkins, P.T.; Kier, R.J.; Lovejoy, R.O.; Black, D.J.; Greger, B.; Solzbacher, F., "A Low-Power Integrated Circuit for a Wireless 100-Electrode Neural Recording System," *Solid-State Circuits, IEEE Journal of* , vol.42, no.1, pp.123,133, Jan. 2007

[6] Yang-Guo Li; Qingyun Ma; Haider, M.R.; Massoud, Y., "Ultra-low-power high sensitivity spike detectors based on modified nonlinear energy operator," *Circuits and Systems (ISCAS), 2013 IEEE International Symposium on* , vol., no., pp.137,140, 19-23 May 2013

[7] Abdelhalim, K.; Jafari, H.M.; Kokarovtseva, L.; Perez Velazquez, J.L.; Genov, R., "64-Channel UWB Wireless Neural Vector Analyzer SOC With a Closed-Loop Phase Synchrony-Triggered Neurostimulator," *Solid-State Circuits, IEEE Journal of* , vol.48, no.10, pp.2494,2510, Oct. 2013

[8] Abdelhalim, K.; Kokarovtseva, L.; Perez Velazquez, J.L.; Genov, R., "915-MHz FSK/OOK Wireless Neural Recording SoC With 64 Mixed-Signal FIR Filters," *Solid-State Circuits, IEEE Journal of* , vol.48, no.10, pp.2478,2493, Oct. 2013

[9] Harrison, R.R.; Kier, R.J.; Chestek, C.A.; Gilja, V.; Nuyujukian, P.; Ryu, S.; Greger, B.; Solzbacher, F.; Shenoy, K.V., "Wireless Neural Recording With Single Low-Power Integrated Circuit," *Neural Systems and Rehabilitation Engineering, IEEE Transactions on* , vol.17, no.4, pp.322,329, Aug. 2009

[10] Seung Bae Lee; Hyung-Min Lee; Kiani, M.; Uei-Ming Jow; Ghovanloo, M., "An Inductively Powered Scalable 32-Channel Wireless Neural Recording System-on-a-Chip for Neuroscience Applications," *Biomedical Circuits and Systems, IEEE Transactions on* , vol.4, no.6, pp.360,371, Dec. 2010

[11] Tesla, N., "Apparatus for transmitting electrical energy." U.S. patent number 1,119,732, issued in December 1914

[12] Andre Kurs, Arsteidis Karalis, Robert Moffatt, John joannpoulos, Peter Fisher, Marin Soljacic, "Wireless Power Transfer via Strongly Coupled Magnetic Resonances," *Science Magazine*, Vol.317, No.5834, 2007, pp.83-86

[13] Hermann A. Haus and Weiping Huang, "Coupled-Mode Theory," *Proceedings of The IEEE*, Vol. 19, No 10, 1991, pp. 1505-1518

[14] GiBum Lee, Carlton Thompson, Taesong Hwang, Raul Andres Chinga, Jenshan Lin, "A 63W 14MHz Class-E Amplifier for Wireless Power Transmission," *Proceedings of APMC*, 2012, pp. 469-471.

[15] Razavi, Behzad, RF microelectronics, 2nd edition, New Jersey: Prentice Hall, 2012.

[16] Thierry Melly, Alain-Serge Porret, Christian C. Enz, and Eric A. Vittoz, "An ultralow-power UHF transceiver integrated in a standard digital CMOS process: transmitter", *IEEE Journal of Solid-State Circuits*, Vol.36, No.3, March 2001.