A field-effect transistor includes a gate, a source and a drain; a semiconductor layer between the source and the drain; and a gate insulator between the gate and the semiconductor layer. The gate insulator comprises a first layer adjoining the semiconductor layer; and a second layer. The first layer is formed from an amorphous fluoropolymer having a first dielectric constant and a first thickness. The second dielectric constant is higher than 5, and the second thickness is smaller than 500 nm.
References Cited

U.S. PATENT DOCUMENTS


OTHER PUBLICATIONS


* cited by examiner
Dipole polarization and/or gate charge injection

Interfacial deep traps

FIGURE 3

FIGURE 4A
FIGURE 4B

FIGURE 4C

FIGURE 4D

FIGURE 4E
FIGURE 5

$\frac{I_{DS}(t)}{I_{DS}(0)}$ vs. Time (s)

- CYTOP (25 nm)/Al$_2$O$_3$ (50 nm)
- CYTOP (40 nm)/Al$_2$O$_3$ (50 nm)
- CYTOP (530 nm)/Al$_2$O$_3$ (50 nm)

FIGURE 6A

$V_{\text{local}} / V_G$ vs. $d_{\text{CYTOP}}$ (nm)

FIGURE 6B

$V_{\text{CYTOP}}$ vs. $k_{\text{Al}_2\text{O}_3}$

$V_G = 8$ V

$V_G = 8$ V
### FIGURE 9A

<table>
<thead>
<tr>
<th>Condition</th>
<th>Before air exposure</th>
<th>After air exposure</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dielectric</td>
<td>Pristine</td>
<td>1,000 scanns 1 h stress</td>
</tr>
<tr>
<td>Dev. 1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CYTOP /Al₂O₃</td>
<td>Dev. 2</td>
<td></td>
</tr>
<tr>
<td>Dev. 3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dev. 4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dev. 5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dev. 6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dev. 7-8</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### FIGURE 9B

**After O₂ plasma**

- ▲ Al₂O₃
- △ CYTOP
- ⋄ CYTOP /Al₂O₃

<table>
<thead>
<tr>
<th>Time (Days)</th>
<th>0</th>
<th>20</th>
<th>100</th>
<th>120</th>
<th>140</th>
<th>160</th>
<th>180</th>
<th>200</th>
</tr>
</thead>
<tbody>
<tr>
<td>µ (cm²/Vs)</td>
<td>10⁻³</td>
<td>10⁻²</td>
<td>10⁻¹</td>
<td>10⁰</td>
<td>10¹</td>
<td>10²</td>
<td>10³</td>
<td>10⁴</td>
</tr>
</tbody>
</table>

### FIGURE 9C

**After O₂ plasma**

- ▲ Al₂O₃
- △ CYTOP
- ⋄ CYTOP /Al₂O₃

<table>
<thead>
<tr>
<th>Time (Days)</th>
<th>0</th>
<th>20</th>
<th>100</th>
<th>120</th>
<th>140</th>
<th>160</th>
<th>180</th>
<th>200</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_th (V)</td>
<td>-26</td>
<td>-24</td>
<td>-22</td>
<td>-20</td>
<td>-18</td>
<td>-16</td>
<td>-14</td>
<td>-12</td>
</tr>
</tbody>
</table>
FIGURE 10A

$W/L = 2550 \mu m/180 \mu m$

$V_{DS} = -8 \, V$

Plot every 2000th interval

$V_{GS}$ (V)

FIGURE 10B

$W/L = 2550 \mu m/180 \mu m$

$V_{DS} = -8 \, V$

Plot every 100th interval

$V_{GS}$ (V)
FIGURE 11A
Before air exposure

FIGURE 11B
After air exposure for 31 days

FIGURE 11C
After air exposure for 31 days and O₂ plasma for 5 min

FIGURE 11D

$V_{GS} = V_{DS} = -8 \text{ V}$

**FIGURE 11E**

- **Dev.1**: pristine
- **Dev.2**: air exposure for 31 days
- **Dev.3**: O$_2$ plasma
- **Dev.4**: air exposure for 90 days
- **Dev.5**: air exposure for 150 days
- **Dev.6**: air exposure for 210 days
- **Dev.7**: air exposure for 365 days

**Axes:**
- $y$-axis: $I_{DS(t)} / I_{DS(0)}$
- $x$-axis: Time (h)

**Legend:**
- ▲ Dev.1: pristine
- △ Dev.2: air exposure for 31 days
- ■ Dev.3: O$_2$ plasma
- □ Dev.4: air exposure for 90 days
- ● Dev.5: air exposure for 150 days
- ○ Dev.6: air exposure for 210 days
- ● Dev.7: air exposure for 365 days
FIGURE 12A

W/L = 200 μm/20 μm
V_{GS} = 7 V

Initial
--- after 1000 times scan
--- after 18 hour bias stress

FIGURE 12B

W/L = 200 μm/20 μm
V_{GS} = 7 V

Initial
--- after 1000 times scan
--- after 18 hour bias stress
**FIGURE 13A**

- **W/L =** 2550 µm/180 µm
- **V_{DS} =** -8 V
- **V_{TH} =** -0.9 V
- **μ =** 0.34 cm²/V·s

**FIGURE 13B**

- **W/L =** 2550 µm/180 µm
- **V_{GS} =** 0 to -8 V
- **V_{DS} (V) =** 0 to -8 V
- Step = 2 V
**FIGURE 16A**  
O₂ effects

**FIGURE 16B**  
H₂O effects

**FIGURE 16C**  
Bias stress

- **Pristine**
- **After O₂ exposure**
- **After H₂O exposure**

\[ \frac{I_{DS}(t)}{I_{DS}(0)} \text{ vs. Time} \]
FIGURE 17

Pristine
(without any exposure)

Exposure to dry O₂ ambient
at 50 °C for 1 day

Vacuum (1 torr)
at 100 °C for overnight (16 h)

Exposure to humid air
(RH 80%) at 50 °C for 1 day

Vacuum (1 torr)
at 100 °C for overnight (16 h)

Soaking in water (H₂O)
for overnight (16 h)

Vacuum (1 torr)
at 100 °C for overnight (16 h)
FIGURE 18A

FIGURE 18B

FIGURE 18C

Pristine

Vacuum

Humid

Vacuum

H₂O

Vacuum

air

Exposure sequence
FIGURE 19A

FIGURE 19B

$C_{\text{in}}$ (nF/cm$^2$)

frequency (Hz)

- ▲ Pristine
- ■ $O_2$
- ◼ Vacuum
- ● Humid air
- ○ $H_2O$
- ◆ Vacuum

$C_{\text{in}}$ (nF/cm$^2$)

frequency (Hz)

- ▲ Pristine
- ■ $O_2$
- ◼ Vacuum
- ● Humid air
- ○ $H_2O$
- ◆ Vacuum
FIGURE 20A

\[ V_{DS} = -8 \text{ V} \]

- ▲ Pristine
- ■ \( \text{O}_2 \)
- ○ - Vacuum
- ◼ - Humid air
- • - Vacuum
- ○ - \( \text{H}_2\text{O} \)
- ◼ - Vacuum

\[ I_{DS}^{1/2} (\mu\text{A}) \]

\[ V_{GS} (\text{V}) \]

FIGURE 20B

\[ \frac{I_{DS}(t)}{I_{DS}(0)} \]

\[ \text{Time (s)} \]

- ▲ Pristine
- ■ \( \text{O}_2 \)
- ○ - Vacuum
- ◼ - Humid air
- • - Vacuum
- ○ - \( \text{H}_2\text{O} \)
- ◼ - Vacuum
FIGURE 22A

$V_{DS} = -8 \text{ V}$

$\frac{I_{DS}}{\sqrt{2} (\mu A)}$ vs $V_{GS} (V)$

FIGURE 22B

$\frac{I_{DS}(t)}{I_{DS}(0)}$ vs Time (s)

- Pristine
- $O_2$
- Humid air
- Vacuum
- $H_2O$
- Vacuum
**FIGURE 23A**

- **C**<sub>in</sub> (nF/cm<sup>2</sup>)

<table>
<thead>
<tr>
<th>Voltage (V)</th>
<th>20</th>
<th>30</th>
<th>40</th>
<th>50</th>
</tr>
</thead>
<tbody>
<tr>
<td>-8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>-6</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>-4</td>
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</tr>
<tr>
<td>-2</td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>0</td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>4</td>
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<td></td>
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</tr>
<tr>
<td>6</td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**FIGURE 23B**

- **J** (A/cm<sup>2</sup>)

<table>
<thead>
<tr>
<th>E-field (MV/cm)</th>
<th>10&lt;sup&gt;-10&lt;/sup&gt;</th>
<th>10&lt;sup&gt;-9&lt;/sup&gt;</th>
<th>10&lt;sup&gt;-8&lt;/sup&gt;</th>
<th>10&lt;sup&gt;-7&lt;/sup&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>-3</td>
<td>10&lt;sup&gt;-10&lt;/sup&gt;</td>
<td>10&lt;sup&gt;-9&lt;/sup&gt;</td>
<td>10&lt;sup&gt;-8&lt;/sup&gt;</td>
<td>10&lt;sup&gt;-7&lt;/sup&gt;</td>
</tr>
<tr>
<td>-2</td>
<td>10&lt;sup&gt;-10&lt;/sup&gt;</td>
<td>10&lt;sup&gt;-9&lt;/sup&gt;</td>
<td>10&lt;sup&gt;-8&lt;/sup&gt;</td>
<td>10&lt;sup&gt;-7&lt;/sup&gt;</td>
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<tr>
<td>-1</td>
<td>10&lt;sup&gt;-10&lt;/sup&gt;</td>
<td>10&lt;sup&gt;-9&lt;/sup&gt;</td>
<td>10&lt;sup&gt;-8&lt;/sup&gt;</td>
<td>10&lt;sup&gt;-7&lt;/sup&gt;</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- ▲ CYTOP (40 nm)/Al<sub>2</sub>O<sub>3</sub> (50 nm)
- ▲ CYTOP (20 nm)/Al<sub>2</sub>O<sub>3</sub> (50 nm)/CYTOP (20 nm)
- ▼ Hyflon (40 nm)/Al<sub>2</sub>O<sub>3</sub> (50 nm)
- ▼ Teflon (40 nm)/Al<sub>2</sub>O<sub>3</sub> (50 nm)
FIGURE 23C

Voltage (V) vs. $C_{in}$ (nF/cm$^2$)

- ▲ CYTOP (40 nm)/SiN$_x$ (50 nm)
- ■ CYTOP (20 nm)/SiN$_x$ (50 nm)/CYTOP (20 nm)
- ▬ Hyflon (40 nm)/SiN$_x$ (50 nm)
- ● Teflon (40 nm)/SiN$_x$ (50 nm)

FIGURE 23D

E-field (MV/cm) vs. J (A/cm$^2$)

- ▲ CYTOP (40 nm)/SiN$_x$ (50 nm)
- ■ CYTOP (20 nm)/SiN$_x$ (50 nm)/CYTOP (20 nm)
- ▬ Hyflon (40 nm)/SiN$_x$ (50 nm)
- ● Teflon (40 nm)/SiN$_x$ (50 nm)
**FIGURE 24A**

W/L = 2550 µm/180 µm

$V_{DS} = -8$ V

$V_{TH} = -3.6$ V,

$\mu = 1.11$ cm²/Vs

**FIGURE 24B**

W/L = 2550 µm/180 µm

$V_{DS} = 0$ to -8 V

Step = 2 V
**FIGURE 24C**

- W/L = 2550 µm/180 µm
- \( V_{DS} = -8 \) V
- \( V_{TH} = -3.3 \) V
- \( \mu = 0.76 \text{ cm}^2/\text{Vs} \)

**FIGURE 24D**

- W/L = 2550 µm/180 µm
- \( V_{GS} = 0 \) to -8 V
- Step = 2 V
FIGURE 24G

$W/L = 2550 \mu m/180 \mu m$

$V_{DS} = -8 \, V$

$V_{TH} = -3.1 \, V$

$\mu = 1.00 \, \text{cm}^2/\text{V} \cdot \text{s}$

FIGURE 24H

$W/L = 2550 \mu m/180 \mu m$

$V_{GS} = 0 \, \text{to} \, -8 \, V$

Step = 2 \, V
**Figure 24I**

- **W/L = 2550 µm/180 µm**
- **V_D = -15 V**
- **V_{TH} = -7.9 V**
- **\( \mu = 0.069 \text{ cm}^2/\text{Vs} \)**

**Figure 24J**

- **W/L = 2550 µm/180 µm**
- **V_{GS} = 0 to -15 V**
- **Step = 3 V**
FIGURE 24K

$W/L = 2550 \mu m/180 \mu m$

$V_{DS} = -15 V$

$V_{th} = -7.8 V$

$\mu = 0.016 \text{ cm}^2/\text{Vs}$

FIGURE 24L

$W/L = 2550 \mu m/180 \mu m$

$V_{GS} = 0 \text{ to } -15 V$

Step = 3 V
FIGURE 24M

- W/L = 2550 µm/180 µm
- V_DS = -15 V
- V_TH = -7.0 V,
- \( \mu = 0.006 \text{ cm}^2/\text{Vs} \)

FIGURE 24N

- W/L = 2550 µm/180 µm
- V_GS = 0 to -15 V
- Step = 3 V
W/L = 2550 µm/180 µm

V_{DS} = -15 V

V_{TH} = -7.9 V,

\mu = 0.02 \text{ cm}^2/\text{Vs}

FIGURE 24O

FIGURE 24P

W/L = 2550 µm/180 µm

V_{GS} = 0 \text{ to } -15 V

Step = 3 V
**FIGURE 25A**

$V_{DS} = -8$ V

**FIGURE 25B**

$V_{DS} = 8$ V

$-I_{DS}$ (A) vs. $V_{GS}$ (V)

- $I_{DS}$ for $V_{DS} = -8$ V
- $I_{DS}$ for $V_{DS} = 8$ V
FIGURE 26A

$V_{DS} = -8$ (V)

- $\triangle$ initial
- $\square$ after 500 scans
- $\bullet$ after 1 h DC bias stress

$-I_{DS} (A)$ vs $V_{GS} (V)$

$-I_{DS}^{1/2} (\mu A^{1/2})$

FIGURE 26B

$V_{GS} = 0$ V to $-8$ V

$Step = 1.0$ V

$I_{DS} (\mu A)$ vs $V_{DS} (V)$
**FIGURE 27A**

- $V_{DS} = 8V$
- Initial
- After 500 scans
- After 1h DC bias

**FIGURE 27B**

- $V_{DS} = 8V, V_{DS} = 1V$
- Initial
- After 500 scans
- After 1h DC bias
FIGURE 28A

- Before bias stress
- After 500 scans of only p-channel FET
- After 500 scans of both p- and n-channel FETs
- After 1h DC stress of only p-channel FET
- After 1h DC stress of both p- and n-channel FETs

$V_{OUT} (V)$

$V_{IN} (V)$
\[ W/L = 2000 \mu m/180 \mu m \]

\[ V_{DS} = 10 \text{ V} \]

\[ V_{TH} = 0.18 \text{ V}, \quad \mu = 0.08 \text{ cm}^2/\text{Vs} \]

\[ V_{GS} = 0 \text{ to } 10 \text{ V} \]

\[ \text{Step} = 2 \text{ V} \]
**FIGURE 32A**

**n-mode**

\[ W/L = 6050 \mu m/180 \mu m \]

\[ V_{DS} = 25 \text{ V} \]

\[ V_{TH} = 13.4 \text{ V} \]

\[ \mu = 1.5 \text{ cm}^2/\text{Vs} \]

\[ I_{DS} (A) \]

\[ I_{DS}^{1/2} (\mu A)^{1/2} \]

\[ V_{GS} (V) \]

**FIGURE 32B**

**n-mode**

\[ W/L = 6050 \mu m/180 \mu m \]

\[ V_{GS} = 0 \text{ to } 25 \text{ V} \]

\[ \text{Step } = 2.5 \text{ V} \]

\[ I_{DS} (\mu A) \]

\[ V_{DS} (V) \]
FIGURE 33A

p-mode
$V_{DS} = -25 \text{ V}$

$W/L = 6050 \ \mu \text{m} / 180 \ \mu \text{m}$

$V_{TH} = -14.4 \ \text{V}$,

$\mu = 9.8 \times 10^{-3} \ \text{cm}^2/\text{Vs}$

FIGURE 33B

p-mode
$W/L = 6050 \ \mu \text{m} / 180 \ \mu \text{m}$

$V_{GS} = 0 \ \text{V}$

to $-25 \ \text{V}$

Step = 2.5 \text{ V}
FIGURE 35A

n-mode
W/L = 6050 \mu m/180 \mu m
V_{DS} = 20 V
V_{TH} = 13.0 V
\mu = 0.75 \text{ cm}^2/\text{Vs}

FIGURE 35B

n-mode
W/L = 6050 \mu m/180 \mu m
V_{GS} = 0 \text{ to } 20 V
Step = 2.5 V
FIGURE 36A

p-mode

\[ V_{DS} = -20 \text{ V} \]

\[ W/L = 6050 \mu\text{m} / 180 \mu\text{m} \]

\[ V_{TH} = -12.3 \text{ V}, \]

\[ \mu = 7.7 \times 10^{-3} \text{ cm}^2/\text{V}s \]

FIGURE 36B

p-mode

\[ V_{GS} = 0 \text{ V} \]

to -25 V

Step = 2.5 V

\[ W/L = 6050 \mu\text{m} / 180 \mu\text{m} \]

\[ V_{DS} (\text{V}) \]

\[ I_{DS} (\mu\text{A}) ]^{1/2} \]
FIGURE 37A

Stability in Ambient

$V_{DS} = 25$ V

0 Days 5 Days 17 Days Annealed

$V_{GS}$ (V) vs $I_{DS}$

$10^{-4}$ $10^{-5}$ $10^{-6}$ $10^{-7}$ $10^{-8}$ $0$ $5$ $10$ $15$ $20$ $25$
This is an image of a patent document page showing a graph. The graph is labeled as FIGURE 37B and includes a title that reads "(Λ)^(HT)Λ". The x-axis is labeled "(ς/ς)(cm^2/s)" and the y-axis is labeled "Exposure (Days)". The graph appears to show two curves crossing each other at a point. The exact nature of the graph and its relevance to the patent is not clear from the image alone.
Stability in Ambient

$V_{DS} = 25 \text{ V}$

0 Days
5 Days
17 Days
Annealed
MULTI-LAYER GATE DIELECTRIC FIELD-EFFECT TRANSISTOR AND MANUFACTURING PROCESS THEREOF

STATEMENT OF GOVERNMENT LICENSE RIGHTS

The inventors received partial funding support through the STC Program of the National Science Foundation under Agreement Number DMR-0120967 and the Office of Naval Research through Contract Award Number N00014-04-1-0120. The Federal Government has certain license rights in this invention.

BACKGROUND

1. Field of the Invention

The present invention relates to a field-effect transistor, a manufacturing process thereof and a circuit comprising a plurality of such transistors.

2. Description of the Related Art

Over the last several years, organic and mixed transition metal oxide semiconductor channel based field-effect transistors (FETs) have been extensively studied because they can be produced at a very low cost on large areas, and on flexible or free-form substrates.

Two critical aspects for the realization of these technologies relate to: 1) the environmental and electrical stability of FETs; and 2) to its low voltage operation. The most common sign of device degradation manifests itself as a threshold voltage shift upon prolonged gate bias stress. Other changes that could arise under bias stress are an increase in the subthreshold slope, reductions of the field-effect mobility, an increase in the OFF current and/or hysteresis between subsequent measurements.

Emerging FET technologies such as those based on organic or transition metal oxide semiconductors suffer from electrical instabilities but offer some advantages over Si-based technologies in that they can be processed at lower temperatures and electrically at a lower cost. In the literature, several routes have been taken to improve the stability of FETs and can be summarized as follows: 1) passivation of gate dielectric/semiconductor interface 2) variation of gate dielectric materials; 3) annealing at high temperatures; 4) variation of source and drain metal electrodes. Among the wide variety of materials used as gate dielectric, fluoropolymers, such as CYTOP, have shown potential to produce interfaces with organic semiconductors with very low trap densities. WO03/052841 in the name of Apecia Ltd (hereby incorporated by reference in its entirety) discloses a process of manufacturing such organic field-effect transistors, where CYTOP has been used in combination with one or more further insulator layers. However, polymers have typically a very low dielectric constant. The latter in conjunction with a large thickness required to avoid large leakage currents, results in a low capacitance density. On the other hand, gate dielectrics with high capacitance can be achieved through the use of inorganic high-k dielectric materials. However, in general the performance of the known devices with a multi-layer dielectric in bias stress tests is unsatisfactory for many applications.


SUMMARY OF THE INVENTION

The object of the invention is to provide a FET having high electrical stability that at the same time can operate at low voltages. More in particular the object of the invention is to provide a FET with an improved performance under continuous bias stress.

According to an embodiment of the invention there is provided a field-effect transistor comprising a gate, a source and a drain. A semiconductor layer extends between said source and said drain, and there is provided a gate insulator between the gate and the semiconductor layer. The gate insulator comprises a first layer and a second layer. The first layer has a first dielectric constant and a first thickness and touches the semiconductor layer along an interface. The interface comprises a plurality of traps causing a first effect on a current between the drain and the source over time under continuous bias stress. The second layer has a second dielectric constant and a second thickness and the second dielectric constant is higher than the first dielectric constant. The second layer is arranged such that said second dielectric constant increases over time under continuous bias stress causing a second effect on the current between the drain and the source over time under continuous bias stress. The first and second thickness and the first and second dielectric constant are such that said first effect compensates at least partly said second effect.

Applying a continuous bias stress means that a drain voltage and gate voltage corresponding to the normal operation of a FET are applied for a long period of time (e.g. one hour). For example for a typical DC bias stress test, the drain and gate voltage could be equal and a couple of volts higher than the threshold voltage of the FET.

According to an embodiment of the invention said first effect on the current between the drain and the source over time under continuous bias stress consists in an increase of the current over time while said second effect on the current between the drain and the source over time under continuous bias stress consists in a decrease of this current. The first and second thickness and the first and second dielectric constant are such that the increase over time compensates at least partly the decrease over time. In that way the variation of the current between the drain and the source over time under continuous bias stress remains within a limited range.

According to an embodiment of the invention the variation of the current between the drain and the source under continuous bias stress (wherein the drain and gate voltage with respect to the source voltage are at least 0.5V above the threshold voltage, i.e. $|V_{DS}|, |V_{GS}|>|V_{TH}|+0.5V$) for 1 hour is less than 5 percent, preferably less than 3 percent. More preferably this variation is less than 5 percent, preferably less than 3 percent, for 2 hours.

According to an embodiment of the invention the variation of the current between the drain and the source under continuous bias stress (wherein the drain and gate voltage with respect to the source voltage are at least 0.5V above the threshold voltage, i.e. $|V_{DS}|, |V_{GS}|>|V_{TH}|+0.5V$) is less than 0.03 per hour, preferably less than 0.015 per hour.

According to a preferred embodiment of the invention the second layer comprises dipoles causing an increase of the second dielectric constant over time under continuous bias stress. In that way, by introducing dipoles in the second layer, the second effect can be influenced in order to obtain an optimal compensation of the first and second effect. In a further embodiment the dipoles produce a change of polar-
This typically leads to negligible hysteresis effects. In a top gate geometry such a bi-layer typically also acts as a barrier coating that can significantly reduce the diffusion of oxygen and moisture into the semiconductor layers, therefore improving the overall FET stability. The combined properties offered by this multilayer gate insulator can therefore be applied to a variety of semiconductor materials. Furthermore, this multilayer gate structure serves as an efficient protection layer when the FETs are subjected to extreme conditions such as oxygen plasma, and immersion in water or common organic solvents, such as acetone. This will allow the use of a photolithography process to pattern the metal gate.

According to another embodiment the first layer is formed of a copolymer of fluorinated 1,3-dioxole and tetrafluoroethylene (TFE), having the formula:

\[
\begin{align*}
\text{X: H, F;} & \\
\text{Y, Z: F, CF}_{3}, & \\
\text{C}_{2}F_{5} \\
\end{align*}
\]

An example thereof is a copolymer of 4,5-difluoro-2,2-bis (trifluoromethyl)-1,3-dioxole (PDD) and tetrafluoroethylene (TFE) such as TEFLON AF with X: F; Y, Z: CF\textsubscript{3} and for example TEFLON AF 1600 (65\% mol PDD, Tg 160° C., permittivity 1.93) or AF 2400 (87\% mol PDD, Tg 240° C., permittivity 1.90). Another example is a copolymer of 2,2,4-trifluoro-5-trifluoromethoxy-1,3-dioxole (TDD) and tetrafluoroethylene (TFE), such as HYFLON AD with X: OCF\textsubscript{3}; Y, Z: F, and for example HYFLON AD40 (40\% mol in TDD, Tg 95° C.) or AD60 (60\% mol in TDD, Tg 125° C.).

According to another embodiment the first layer is formed of an alternating copolymer of perfluorofuran (PFF) and tetrafluoroethylene (TFE); or a homo- or copolymer of perfluoro(4-vinylxoyl)-1-alkenes, as shown in the formula below:
or a PFF derivative having the structure below:

```
F \(\equiv\) X
\(\equiv\) Y
\(\equiv\) Z
```

X: H, F, \(\text{OCF}_3\)
Y: Z, \(\text{CF}_3\), \(\text{CF}_2\text{CF}_3\)

Suitable commercially available materials of this type can be found in the CYTOP class. An example is CYTOP grade CTL-809M supplied by Asahi Glass Corporation, Co. Ltd.

According to a preferred embodiment, the inorganic material of the second layer comprises any one of the following materials, or a combination thereof: \(\text{Al}_2\text{O}_3\), \(\text{SiN}_x\), \(\text{TiO}_2\), \(\text{HIO}_3\), \(\text{Ta}_2\text{O}_5\), \(\text{SiO}_2\), \(\text{Y}_2\text{O}_3\), \(\text{ZrO}_2\) or any other suitable material. A particularly preferred material is \(\text{Al}_2\text{O}_3\). According to another embodiment the second layer is fabricated from an organic material, and for example any one of the following materials: polymers comprising a polymer matrix having a charge distribution with orientable and/or inducible dipoles or a polymer matrix doped with molecules with permanent dipoles. The presence of such permanent or inducible dipoles will cause the dielectric constant of the second layer to vary over time under continuous bias stress as a consequence of a varying electric field over the second layer. Hence, by an appropriate choice of materials with dipole behavior for the second layer, the above mentioned second effect can be reached.

According to a preferred embodiment the second layer is deposited by any one of the following techniques: atomic layer deposition (ALD), electron beam deposition, RF-sputtering, chemical vapor deposition (CVD) or PECVD, pulsed-layer deposition (PLD), spin-coating, printing, lamination, doctor-blading or any other known suitable method. A particularly preferred technique is atomic layer deposition (ALD). \(\text{Al}_2\text{O}_3\) has a high relative dielectric constant and ALD makes it possible to deposit a very thin layer thereof. In that way a device can be obtained with a sufficiently high capacitance density allowing low voltage operation.

According to a preferred embodiment the thickness of the first layer is less than 200 nm, preferably less than 100 nm, and more preferably less than 50 nm. According to a preferred embodiment the thickness of the second layer is less than 500 nm, preferably less than 100 nm, and more preferably less than 50 nm. Typically, it is preferred to have a small thickness, however guaranteeing a sufficiently low leakage current and an improved stability under continuous bias stress. More in particular the choice of the thickness will typically depend on the interplay between the first and second thickness, and the first and second dielectric constant and on the threshold voltage shift in function of time under continuous bias stress that is produced at the interface between the first layer and the semiconductor layer.

According to a preferred embodiment the gate insulator is a bi-layer consisting of the first and second layer.

According to a preferred embodiment the gate insulator further comprises a third layer between the second layer and the gate. In a bottom-gate FET, this third layer will typically be deposited on top of the semiconductor layer to protect it from air. Such a third layer can further improve the barrier properties. The third layer can be formed from any barrier coating material such as an amorphous fluoropolymer which functions as a passivation layer for the underlying inorganic dielectric layer. The thickness of the third layer is preferably less than 100 nm, more preferably less than 50 nm, and most preferably less than 25 nm. For very specific applications, it is possible to use more than three layers, but usually it is preferred to limit the thickness of the gate insulator.

According to a preferred embodiment the semiconductor layer is an organic semiconductor layer, wherein the material of the first layer is soluble in an orthogonal solvent. Solvent orthogonality between fluoropolymers and commonly used organic semiconductor layers makes it possible to spin coat on top of the organic channel layer in case of a top gate geometry. According to a preferred embodiment the semiconductor layer is an organic semiconductor layer selected from any one of the following materials: a pentacene layer, a blend of triisopropylsilylethynyl (TIPS)-pentacene in polytriarylamine (PTAA), a blend of 5,11-Bis(triethylsilylethynyl)anthradithiophene (diF-TESADT) in PTAA. According to another embodiment the semiconductor layer is an inorganic semiconductor layer, such as a transition metal oxide.

According to a preferred embodiment the second relative dielectric constant is higher than 5, preferably higher than 7.

The invention further relates to a circuit, e.g. a backplane circuit for a display, an inverter circuit, a ring oscillator, a logic gate, etc, comprising a plurality of field-effect transistors according to any one of the embodiments disclosed above.

A further embodiment of the invention provides a process for manufacturing a top gate field-effect transistor comprising providing a source, a drain, a semiconductor layer between the source and the drain, and a gate insulator between said gate and said semiconductor layer. The providing of the gate insulator comprises depositing a first layer having a first dielectric constant and a first thickness. The first layer defines an interface with the semiconductor layer. The depositing of the first layer and the providing of the semiconductor layer is such that the interface comprises a plurality of traps causing a first effect on the drain source current over time under continuous bias stress. The providing of the gate insulator also comprises depositing a second layer having a second dielectric constant and a second thickness, said second dielectric constant being higher than said first dielectric constant and said second dielectric constant increasing over time under continuous bias stress causing a second effect on the drain source current over time under continuous bias stress.

According to a preferred embodiment of the process, the source and drain are patterned on a glass substrate and the semiconductor layer is deposited on said glass substrate burying the source and the drain.

According to a preferred embodiment of the process, the gate insulator is provided on top of a substrate and the semiconductor layer is deposited on top of the gate insulator.

According to a preferred embodiment of the process, the first layer is deposited by spin coating using a fluoro-solvent in combination with an amorphous fluoropolymer.

According to a preferred embodiment of the process, the second layer is deposited by atomic layer deposition (ALD). According to a preferred embodiment of the process, the providing of the gate insulator further comprises depositing a third layer of an amorphous fluoropolymer on top of said second layer.

In another embodiment, a composition is provided comprising at least one electron transport semiconductor and at least one polymer matrix. In one embodiment, the electron
transport organic semiconductor has a molecular weight of about 1,000 or less. In one embodiment, the polymer is a hole transporting material. In one embodiment, the polymer comprises an arylamine. In one embodiment, the polymer is an optionally substituted polystyrene, such as poly(c-methyl styrene). The amount of polymer can be, for example 10 wt. % to 90 wt. %, and the amount of semiconductor can be, for example, 10 wt. % to 90 wt. %.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1A and 1B are schematic section views of a top gate field-effect transistor (FET) and of a bottom gate FET, respectively, according to a first embodiment of the invention.

FIG. 2 is a schematic section view of a FET according to a second embodiment of the invention.

FIG. 3 illustrate the first, second, and third effects influencing the drain current under continuous bias stress in an embodiment of a FET according to the invention.

FIG. 4A shows a section view of a field-effect transistor with a CYTOP/Al2O3 dielectric; FIG. 4B shows a section view of a TIPS-pentacene and Poly (triarylamine) (PTAA) blend channel based OFET with a CYTOP/Al2O3 bi-layer (40 nm CYTOP; 50 nm Al2O3) using a glass substrate; FIG. 4C shows a section view of a TIPS-pentacene and PTAA blend channel based OFET with a CYTOP/Al2O3 bi-layer using a plastic substrate; FIG. 4D shows a section view of a TIPS-pentacene and PTAA blend channel based OFET with CYTOP/Al2O3 bi-layer (45 nm CYTOP; 50 nm Al2O3); FIG. 4E shows a section view of a diF-TESADT and PTAA blend channel based OFET with a CYTOP/Al2O3 bi-layer (45 nm CYTOP; 50 nm Al2O3); FIG. 4F shows a section view of a TIPS-pentacene and Poly PTAA blend channel based OFET with a CYTOP/Al2O3/CYTOP tri-layer (20 nm CYTOP; 50 nm Al2O3; 20 nm CYTOP); FIG. 4G shows a section view of a Pentacene and InGaZnO based inverters; and FIG. 4H shows a section view of a Polyera Activink N2200 based OFET with a CYTOP/Al2O3 bi-layer (45 nm CYTOP; 50 nm Al2O3) and evaporated Ag source/drain electrodes.

FIG. 5 illustrates the ratio of the drain current I ds with respect to the initial drain current I dso in function of the time under continuous bias stress in the OFET of FIG. 4A for three different CYTOP layer thicknesses.

FIGS. 6A and 6B illustrate the influence of the CYTOP layer thickness t CYTOP and of the Al2O3 dielectric constant k Al2O3 on the voltage V CYTOP over the CYTOP layer and on the voltage V Al2O3 over the Al2O3 layer.

FIGS. 7A and 7B show the capacitance density-electric field (C-E) and current density-electric field (J-E) characteristics of Al2O3 (100 nm), CYTOP (780 nm), and CYTOP/Al2O3 (50 nm) films, respectively.

FIGS. 8A and 8B show the transfer and output characteristics, measured for an OFET (W/L=2550/30 μm) using a CYTOP (40 nm)/Al2O3 (50 nm) gate dielectric, respectively.

FIG. 9A shows a table that summarizes the different conditions of environmental exposure and electrical stress to which sets of OFETs were subjected. FIGS. 9B and 9C show the variations of the mobility and the threshold voltage V th in time, respectively, for OFETs with Al2O3 (100 nm), CYTOP (780 nm), and CYTOP (40 nm)/Al2O3 (50 nm) films; and FIG. 9D shows the variations of the mobility and the threshold voltage V th for an OFET with a CYTOP (40 nm)/Al2O3 (50 nm) film.

FIGS. 10A and 10B show a sampling of the transfer curves measured in a CYTOP (40 nm)/Al2O3 (50 nm) OFET during multiple continuous scans from the "off" to the "on" region, before and after air exposure.

FIGS. 11A, 11B, and 11C shows the temporal evolution of the Ids measured in different OFETs normalized to the initial value before air exposure; after air exposure for 31 days and after air exposure for 31 days and O2 plasma for 5 minutes, respectively; FIG. 11D shows a transfer and output characteristics before and after DC bias stress for the device of FIG. 4A; and FIG. 11E shows the temporal evolution of the Ids over 24 h of electrical bias stress measured in an OFET with a CYTOP (40 nm)/Al2O3 (50 nm) film under various conditions.

FIGS. 12A and 12B show the transfer and output characteristics of amorphous InGaZnO FETs with the CYTOP/Al2O3 bi-layer after multiple scans of the transfer characteristic and after a constant DC bias stress for 18 hour, respectively.

FIGS. 13A-13B show the transfer and output characteristics measured from pristine devices under a nitrogen atmosphere, of OFETs (W/L=2550 μm/180 μm) using a CYTOP (40 nm)/Al2O3 (50 nm) gate dielectric and a plastic (PES) substrate.

FIG. 14A shows the temporal evolution of the Ids during DC bias stress measured in OFETs (W/L=2550 μm/180 μm) using a CYTOP (40 nm)/Al2O3 (50 nm) gate dielectric and a plastic (PES) substrate initially, after 4 months in air, and after bending for 30 minutes (tensile stress). FIG. 14B shows the bending apparatus used to bend the plastic substrate OFET. FIG. 15A shows the voltage transfer characteristics of a resistive-load inverters with the plastic substrate OFET initially, and after 2 hours of DC bias stress, after 4 months in air, and after bending for 30 minutes (tensile stress).

FIG. 16A-16C illustrate O2 and H2O effects on threshold voltage shift in the transfer characteristics of OFETs (Figs. 16A and 16B) and the variation of drain current under constant dc bias stress (FIG. 16C).

FIG. 17 illustrates an exposure sequence showing the conditions to which sets of OFETs were exposed to determine their environmental stability.

FIGS. 18A-18C show the capacitance C (μF/cm2), mobility μ (cm2/Vs), and threshold voltage V th(V) for each stage of the exposure sequence of FIG. 17.

FIGS. 19A and 19B show the variation in capacitance for frequencies ranging from 20 Hz to 1 million Hz, for the CYTOP/Al2O3 bi-layer OFET (45 nm CYTOP; 50 nm Al2O3) (FIG. 19A) and the CYTOP/Al2O3/CYTOP tri-layer OFET (20 nm CYTOP; 50 nm Al2O3; 20 nm CYTOP) (FIG. 19B), at each stage of the exposure sequence of FIG. 17.

FIGS. 20A and 20B show the transfer characteristics and temporal evolution of the Ids during DC bias for a TIPS-pentacene and PTAA blend channel based OFET with a CYTOP/Al2O3 bi-layer (45 nm CYTOP; 50 nm Al2O3), after each stage of the exposure sequence of FIG. 17.
FIGS. 22A and 22B show the transfer characteristics and temporal evolution of the $I_{DS}$ during DC bias for a TIPS-pentacene and P Tata blend channel based OFET with a CYTOP/Al$_2$O$_3$/CYTOP tri-layer (20 nm CYTOP; 50 nm Al$_2$O$_3$; 20 nm CYTOP), after each stage of the exposure sequence of FIG. 17.

FIGS. 23A-23D show the capacitance and current density-electric field (J-E) characteristics of capacitors with varying fluoropolymer bi-layers.

FIGS. 24A and 24B show the transfer characteristics and output characteristics for a CYTOP (45 nm)/Al$_2$O$_3$ (50 nm) bi-layer OFET. FIGS. 24C and 24D show the transfer characteristics and output characteristics for a Teflon (45 nm)/Al$_2$O$_3$ (50 nm) bi-layer OFET. FIGS. 24E and 24F show the transfer characteristics and output characteristics for a CYTOP (20 nm)/Al$_2$O$_3$ (50 nm)/CYTOP (20 nm) tri-layer OFET. FIGS. 24G and 24H show the transfer characteristic and output characteristics for a CYTOP (45 nm)/S,N$_x$ (50 nm) bi-layer OFET. FIGS. 24K and 24L show the transfer characteristic and output characteristics for a Teflon (45 nm)/S,N$_x$ (50 nm) bi-layer OFET. FIGS. 24M and 24N show the transfer characteristic and output characteristics for a CYTOP (20 nm)/S,N$_x$ (50 nm)/CYTOP (20 nm) tri-layer OFET.

FIGS. 25A and 25B show the drain current $I_{DS}$ with respect to gate voltage $V_{GS}$ for the pentacene and InGaZnO FETs of FIG. 4G after 500 consecutive sweeps. FIG. 25C shows the temporal evolution of the $I_{DS}$ measured in the pentacene and InGaZnO FETs, normalized to the initial value, under DC bias stress over 60 minutes.

FIGS. 26A and 26B show the transfer characteristics and output characteristics of the pentacene FETs of FIG. 4G after various stress conditions.

FIGS. 27A and 27B show the transfer characteristics and output characteristics of the InGaZnO FETs of FIG. 4G after various stress conditions.

FIGS. 28A and 28B show the voltage transfer characteristics and static gain of the inverter of FIG. 4G after various stress conditions.

FIGS. 29A and 29B show the transfer characteristics and output characteristics of a Polyera Activink N2200 based OFET with a CYTOP/Al$_2$O$_3$ bi-layer (45 nm CYTOP; 50 nm Al$_2$O$_3$) and evaporated Au source/drain electrodes, as discussed in Example 12.

FIGS. 30A and 30B show the transfer characteristics and output characteristics of a Polyera Activink N2200 based OFET with a CYTOP/Al$_2$O$_3$ bi-layer (45 nm CYTOP; 50 nm Al$_2$O$_3$) and evaporated Ag source/drain electrodes, as discussed in Example 13.

FIGS. 31A and 31B show the transfer characteristics and output characteristics of a Polyera Activink N2200 based OFET with a CYTOP/Al$_2$O$_3$ bi-layer (45 nm CYTOP; 50 nm Al$_2$O$_3$) and printed Ag source/drain electrodes, as discussed in Example 14.

FIGS. 32A and 32B show the transfer characteristics and output characteristics of an LEH-III-002a based OFET with a CYTOP/Al$_2$O$_3$ bi-layer (45 nm CYTOP; 50 nm Al$_2$O$_3$) and Au bottom contact source/drain electrodes in n-mode operation.

FIGS. 33A and 33B show the transfer characteristics and output characteristics of an LEH-III-002a based OFET with a CYTOP/Al$_2$O$_3$ bi-layer (45 nm CYTOP; 50 nm Al$_2$O$_3$) and Au bottom contact source/drain electrodes in p-mode operation.

FIGS. 34A and 34B show the transfer characteristics and output characteristics of an LEH-III-085g based OFET with a CYTOP/Al$_2$O$_3$ bi-layer (45 nm CYTOP; 50 nm Al$_2$O$_3$) and Au bottom contact source/drain electrodes.

FIGS. 35A and 35B show the transfer characteristics and output characteristics of an LEH-III-085g:PoMS based OFET with a CYTOP/Al$_2$O$_3$ bi-layer (45 nm CYTOP; 50 nm Al$_2$O$_3$) and Ag bottom contact source/drain electrodes.

FIGS. 36A and 36B show the transfer characteristics and output characteristics of an LEH-III-085g:PoMS based OFET with a CYTOP/Al$_2$O$_3$ bi-layer (45 nm CYTOP; 50 nm Al$_2$O$_3$) and Ag bottom contact source/drain electrodes in n-mode operation.

FIGS. 37A and 37B show the results of an ambient exposure study on the LEH-III-119a based OFET with a CYTOP/Al$_2$O$_3$ bi-layer (45 nm CYTOP; 50 nm Al$_2$O$_3$) and Au bottom contact source/drain electrodes.

FIGS. 38A and 38B show the results of an ambient exposure study on the LEH-III-119a:PoMS blend based OFET with a CYTOP/Al$_2$O$_3$ bi-layer (45 nm CYTOP; 50 nm Al$_2$O$_3$) and Au bottom contact source/drain electrodes.

FIGS. 39A and 39B show the transfer characteristics and output characteristics of a DRR-IV-209n based OFET with a CYTOP/Al$_2$O$_3$ bi-layer (45 nm CYTOP; 50 nm Al$_2$O$_3$).

**DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS**

FIG. 1A illustrates a first embodiment of a top gate field-effect transistor (FET) according to the invention. The illustrated FET embodiment comprises a substrate 101, a semiconductor layer 102, a source and a drain 109 buried or in contact with the semiconductor layer, a gate insulator 103, 104 on top of the semiconductor layer 102, and a gate 110 on top of the gate insulator. The gate insulator comprises a first layer 103 formed from a first material, e.g. an amorphous fluoropolymer and a second layer 104 formed from a second dielectric material, typically a high-k dielectric. The source and drain electrode 109 are typically patterned on the substrate 101, and the layer of semiconductor material 102 is deposited over the source and drain electrodes 109. Note that the top gate structure could be staggered (as illustrated in FIG. 1A) or coplanar where the source and drain 109 touch the gate insulator layer 103. The top gate metal electrode 110 is typically patterned on the second layer 104. FIG. 1B illustrates a similar embodiment for a bottom gate FET with a substrate 101, a gate 110, a bi-layer gate dielectric 103, 104, a semiconductor layer 102 and a drain and source 109.

The thickness of the first layer 103, 104 is preferably less than 200 nm, more preferably less than 100 nm, and most preferably less than 50 nm. Further, preferably the thickness of the second layer 104, 104’ is less than 500 nm, more preferably less than 100 nm, and most preferably less than 50 nm.

The use of an amorphous fluoropolymer/high-k oxide bi-layer combines the good chemical properties of amorphous fluoropolymer with the high film quality and large capacitance density of high-k oxides. In addition, for the top gate geometry, this bi-layer gate dielectric also has better encapsulation properties against environmental exposure than a single layer amorphous fluoropolymer.

The material of the first layer can e.g. be any one of the following materials: a copolymer of fluorinated 1,3-dioxole and tetrafluoroethylene (TFE), such as a copolymer of 4,5-
difluoro-2,2-bis(trifluoromethyl)-1,3-dioxole (PDD) and tetrafluoroethylene (TFE) or a copolymer of 2,2,4,4-tetrafluoro-5-
trifluoromethoxy-1,3-dioxole (TDD) and tetrafluoroethylene (TFE); a copolymer of perfluoro(4-vinyl-
loxy)-1-alkene. The first layer can e.g. be deposited from a
formulation with the fluoropolymer and one or more fluoro
solvents by any one of the following printing or coating
techniques: spin coating, doctor blading, wire bar coating,
spray or dip coating, ink jet printing, gravure printing, flexo
printing, or any other known suitable method.

The dielectric material of the second layer is preferably a
high-k inorganic dielectric, and can e.g. be any one of the following materials: Al₂O₃, SiO₂, TiO₂, HIO₃, Ta₂O₅, SiO₂,
Y₂O₃, ZrO₂, any other suitable materials. Alternatively the
second layer can be formed from an organic material, and for
example any one of the following materials: polymers com-
prising orientable and/or inducible dipoles or a polymer
matrix doped with molecules with permanent dipoles. The
second layer can e.g. be deposited by any one of the following
techniques: atomic layer deposition (ALD), electron beam
deposition, RF-sputtering or plasma-enhanced chemical
deposition, pulsed laser deposition (PLD), or any other
known suitable technique. According to a preferred embodi-
mation the second layer is an Al₂O₃ layer deposited by ALD.

The semiconductor layer

instability mechanisms that influence the drain source current in function of time

under continuous bias stress, see FIG. 3. The first effect
causes a decrease of the current while the second and third
effects cause an increase of the current. According to an
embodiment of the invention the thicknesses t1 and t2 of the
first and second layer and the dielectric constants k1 and k2
are chosen such that those effects at least partially compen-
sate each other, see the current curve drawn in a full line in
FIG. 3.

FIG. 2 illustrates a second embodiment of a FET according
to the invention which is similar to the first embodiment (the
elements 101-104, 109, 110 correspond with the elements
201-204, 209, 210) with this difference that a third layer 205
is added above the second layer. The third layer 205 is pref-
erably formed of an amorphous fluoropolymer. Such a third
layer forms a passivation layer for the underlying inorganic
dielectric layer 204 which can lead to a better long term
stability. The thickness of the third layer 205 is preferably
less than 100 nm, more preferably less than 50 nm, and most
preferably less than 25 nm. This thickness can be further
optimized to further improve the above described compen-
sation effect. Note however that it is usually preferred to keep
the gate insulator as thin as possible, and the stability of the
bi-layer gate insulator illustrated in FIG. 1A will typically
provide sufficient stability.

EXAMPLE 1

TIPS-Pentacene and Poly (Triarylamine) (PTAA)
Blend Channel Based OFET with CYTOP/Al₂O₃
Bi-Layer Using Glass Substrate (40 nm CYTOP, 50
nm Al₂O₃)

OFETs with a bottom-contact and top-gate structure were
fabricated on glass substrates (Corning 1737). Poly-4-vi-
nylphenol (PVP) buffer layers were prepared from a 2 wt. %
solutions of PVP (Mw~20,000) and poly (melamine-co-form-
alddehyde), as a cross-linking agent, in propylene glycol
monomethyl ether acetate (PGMEA), which were deposited
by spin coating at 3000 rpm for 40 sec and subsequently
cross-linked at 175°C on a hot plate for 1 h in a N₂-filled
glove box. Au (50 nm) bottom-contact source/drain elec-
trodes were deposited by thermal evaporation through a
shadow mask. A self-assembled monolayer of pentfluoro-
benzenethiol (PFBT) was formed on the Au electrodes by
immersion in a 10 mmol PFBT solution in ethanol for 15 min
in a N₂-filled dry box, rinsing with pure ethanol, and drying.
The TIPS-pentacene and PTAA blend solution was prepared
as follows: TIPS-pentacene and PTAA were individually dis-
solved in 1,2,3,4-Tetrahydrophthalic anhydride, 99%
(Sigma Aldrich) for a concentration of 30 mg/mL and the two
individual solutions were mixed to yield a weight ratio of 1:1.
TIPS-pentacene and PTAA blend active layers were depos-
ted by spin coating at 500 rpm for 10 sec and at 2000 rpm
for 20 sec. Then, samples were dried at room temperature for 5
min and annealed at 40°C for 16 h and at 100°C for 15 min
in a N₂-filled dry box. CYTOP (40 nm)/Al₂O₃ (50 nm) layers
were used as top-gate dielectrics. CYTOP solution (CTIL-
809M) was purchased from Asahi Glass with a concentration
of 9 wt. %. To deposit the 40 nm-thick CYTOP layers, the
original solution diluted with their solvents (CT-solv. 180) to
have solution:solvent ratios of 1:3.5. The 40 nm-thick
CYTOP layers were deposited by spin casting at 3000 rpm
for 60 sec. The CYTOP (40 nm) films were annealed at 100°C
for 20 min. All spin coating and annealing processes were
conducted in a N₂-filled dry box. Then, the Al₂O₃ dielectric
films (50 nm) were deposited on top of the CYTOP layer
using a Savannah 100 ALD system from Cambridge Nano-
tech Inc. Films were grown at 110°C using alternating expo-
sures of trimethyl aluminum [Al(CH₃)₃] and H₂O vapor at a
deposition rate of approximately 0.1 nm per cycle. Finally, Al
(150 nm) gate electrodes were deposited by thermal evapo-
ration through a shadow mask. The resulting OFET is de-
scribed in FIG. 4B.

EXAMPLE 2

Pentacene Channel Based OFET

The top gate pentacene OFETs were fabricated with a
geometry incorporating a bottom source/drain electrodes. Au
(80 nm) bottom contact source/drain electrodes were depos-
ted by electron-beam (e-beam) at room temperature on a
glass substrate through a shadow mask. A pentacene active layer (50 nm) was then deposited by thermal evaporation at room temperature through a shadow mask. CYTOP (40 nm)/Al₂O₃ (50 nm) layers were used as a top gate dielectric. CYTOP (40 nm) layers were coated by spin casting at 3000 rpm for 60 seconds. The CYTOP films were annealed at 100°C for 20 min. Al₂O₃ dielectric films were grown at 110°C using alternating exposures of trimethyl aluminum [Al(CH₃)₃] and H₂O vapor at a deposition rate of approximately 0.1 nm per cycle. Then, Al electrode was sequentially deposited by e-beam to form the gate electrode.

**EXAMPLE 3**

**InGaZnO Channel Based Oxide FET**

The top gate amorphous InGaZnO FET was fabricated with a geometry incorporating a bottom source/drain electrodes. First, a tri-layer of Ti (6 nm)/Au (50 nm)/Ti (6 nm) was deposited using electron-beam (e-beam) at room temperature on a glass substrate (Corning 1737) and patterned by photolithography followed by a lift-off process. A 40 nm-thick a-IGZO (Ga₂O₃:In₂O₃:ZnO=1:1:2 mol%) active layer was then deposited by radio frequency (RF) sputtering. After deposition of the a-IGZO layer, the device was annealed. To define the channel, the a-IGZO layer was patterned by a wet-etching process using hydrochloric acid (HCl:H₂O=1:1) diluted in DI water. CYTOP (40 nm)/Al₂O₃ (50 nm) layers were used as top gate dielectrics. Al₂O₃ dielectric films were grown at 110°C using alternating exposures of trimethyl aluminum [Al(CH₃)₃] and H₂O vapor. For 40 nm CYTOP layer, a 2 wt% solution was used, which was diluted with solvent. CYTOP (40 nm) layers were coated by spin casting at 3000 rpm for 60 seconds. The CYTOP films were annealed at 100°C for 20 min. Then, Ti (6 nm) and Au (120 nm) were sequentially deposited by e-beam and patterned by photolithography and lift-off process to form the gate electrode.

**EXAMPLE 4**

**TIPS-Pentacene and PTAA OFET with CYTOP/SiNₓ Bi-Layer**

Example 4 is identical to example 1, with this difference that, instead of depositing Al₂O₃, using an ALD process, an SiNₓ layer is deposited by plasma-enhanced chemical vapor deposition (PECVD) at a process temperature of 110°C. Note that it is also possible to work at a higher temperature depending on the glass transition temperature of the fluoropolymer and semiconductor layer in the case of an amorphous semiconductor layer.

**EXAMPLE 5**

**TIPS-Pentacene and PTAA OFET with Hyflon/Al₂O₃ Bi-Layer**

Example 5 is identical to example 1, with this difference that, instead of depositing CYTOP, a 40 nm layer of Hyflon AD 40X material is deposited.

**EXAMPLE 6**

**TIPS-Pentacene and PTAA OFET with Teflon/Al₂O₃ Bi-Layer**

Example 6 is identical to example 1, with this difference that, instead of depositing CYTOP, a 40 nm layer of Teflon material is deposited.

Although the examples above relate to top gate FETs, the skilled person will understand that bottom gate FETs can be fabricated in a more or less similar way.

**EXAMPLE 7**

**TIPS-Pentacene and Poly (Triarylamine) (PTAA) Blend Channel Based OFET with CYTOP/Al₂O₃ Bi-Layer Using Plastic Substrate**

OFETs with a bottom-contact and top-gate structure were fabricated on a flexible polyethersulfone (PES) substrate. Poly-4-vinylphenol (PVP) buffer layers were prepared from 2 wt% solutions of PVP (Mₙ=20,000) and poly (melamine-co-formaldehyde), as a cross-linking agent, in propylene glycol monomethyl ether acetate (PGMEA), which were deposited by spin coating at 3000 rpm for 40 sec and subsequently cross-linked at 175°C on a hot plate for 1 h in a N₂-filled glove box. Au (50 nm) bottom-contact source/drain electrodes were deposited by thermal evaporation through a shadow mask. A self-assembled monolayer of pentaffluorobenzenethiol (PFBT) was formed on the Au electrodes by immersion in a 10 mmol PFBT solution in ethanol for 15 min in a N₂-filled dry box, rinsing with pure ethanol, and drying. The TIPS-pentacene and PTAA blend solution was prepared as follows: TIPS-pentacene and PTAA were individually dissolved in 1,2,3,4-tetrahydroxiphophorus anhydrous, 99% (Sigma Aldrich) for a concentration of 30 mg/mL and the two individual solutions were mixed to yield a weight ratio of 1:1. TIPS-pentacene and PTAA blend active layers were deposited by spin coating at 500 rpm for 10 sec and at 2000 rpm for 20 sec. Then, samples were annealed at 100°C for 15 min in a N₂-filled dry box. CYTOP (40 nm)/Al₂O₃ (50 nm) layers were used as top-gate dielectrics. CYTOP solution (CTL-809/M) was purchased from Asahi Glass with a concentration of 9 wt%. To deposit the 40 nm-thick CYTOP layers, the original solution diluted with their solvents (CT-solv: 180) to have solution solvent ratios of 1:3.5. The 40 nm-thick CYTOP layers were deposited by spin casting at 3000 rpm for 60 sec. The CYTOP (40 nm) films were annealed at 100°C for 20 min. All spin coating and annealing processes were carried out in a N₂-filled dry box. Then, the Al₂O₃ dielectric films (50 nm) were deposited on top of the CYTOP layer using a Savannah 100 ALD system from Cambridge Nanotech Inc. Films were grown at 110°C using alternating exposures of trimethyl aluminum [Al(CH₃)₃] and H₂O vapor at a deposition rate of approximately 0.1 nm per cycle. Finally, Al (150 nm) gate electrodes were deposited by thermal evaporation through a shadow mask. The resulting OFET is depicted in FIG. 4C.

**EXAMPLE 8**

**TIPS-Pentacene and Poly (Triarylamine) (PTAA) Blend Channel Based OFET with CYTOP/Al₂O₃ Bi-Layer (45 nm CYTOP; 50 nm Al₂O₃)**

OFETs with a bottom-contact and top-gate structure were fabricated on glass substrates (Corning, Eagle 2000). Au (50 nm) bottom-contact source/drain electrodes were deposited by thermal evaporation through a shadow mask. A self-assembled monolayer of pentaffluorobenzenethiol (PFBT) was formed on the Au electrodes by immersion in a 10 mmol PFBT solution in ethanol for 15 min in a N₂-filled dry box, rinsing with pure ethanol, and drying. The TIPS-pentacene and PTAA blend solution was prepared as follows: TIPS-pentacene and PTAA were individually dissolved in 1,2,3,4-...
Tetrahydroanaphthalene anhydrous, 99%, (Sigma Aldrich) for a concentration of 30 mg/mL and two individual solutions were mixed to yield a weight ratio of 1:1. TIPS-pentacene and PTAA blend active layers were deposited by spin coating at 500 rpm for 10 sec and at 2000 rpm for 20 sec. Then, samples were annealed at 100°C for 15 min in a N₂-filled dry box. CYTOP (45 nm)/Al₂O₃ (50 nm) layers were used as top-gate dielectrics. CYTOP solution (CTL-809M) was purchased from Asahi Glass with a concentration of 9 wt. %. To deposit the 45 nm-thick CYTOP layers, the original solution diluted with their solvents (CT-solv. 180) to have solution:solvent ratios of 1:3.5. The 45 nm-thick CYTOP layers were deposited by spin casting at 3000 rpm for 60 sec. The CYTOP (45 nm) films were annealed at 100°C for 20 min. All spin coating and annealing processes were carried out in a N₂-filled dry box. Then, the Al₂O₃ dielectric films (50 nm) were deposited on top of the CYTOP layer using a Savannah 100 ALD system from Cambridge Nanotech Inc. Films were grown at 110°C using alternating exposures of trimethyl aluminum [Al(CH₃)₃] and H₂O vapor at a deposition rate of approximately 0.1 nm per cycle. Finally, Al (150 nm) gate electrodes were deposited by thermal evaporation through a shadow mask. The resulting OFET is depicted in FIG. 4D.

**EXAMPLE 9**

dif-TESADT and Poly (Triarylamino) (PTAA) Blend Channel Based OFET with CYTOP/Al₂O₃ Bi-Layer (45 nm CYTOP; 50 nm Al₂O₃)

Example 9 is identical to example 8, except 2,8-difluoro-5,11-bis(triethylsilylhexyl) anthradithiophene (dif-TESADT) was used rather than TIPS-pentacene. The structure of dif-TESADT is shown below:

![Image of dif-TESADT structure](image-url)

The resulting OFET is depicted in FIG. 4E.

**EXAMPLE 10**

TIPS-Pentacene and Poly (Triarylamino) (PTAA) Blend Channel Based OFET with CYTOP/Al₂O₃/CYTOP Tri-Layer (20 nm CYTOP; 50 nm Al₂O₃; 20 nm CYTOP)

OFETs with a bottom-contact and top-gate structure were fabricated on glass substrates (Corning, Eagle 2000). Au (50 nm) bottom-contact source/drain electrodes were deposited by thermal evaporation through a shadow mask. A self-assembled monolayer of pentafluorobenzethiol (PFBT) was formed on the Au electrodes by immersion in a 10 mmol PFBT solution in ethanol for 15 min in a N₂-filled dry box, rinsing with pure ethanol, and drying. The TIPS-pentacene and PTAA blend solution was prepared as follows: TIPS-pentacene and PTAA were individually dissolved in 1,2,3,4-Tetrahydroanaphthalene anhydrous, 99%, (Sigma Aldrich) for a concentration of 30 mg/mL and the two individual solutions were mixed to yield a weight ratio of 1:1. TIPS-pentacene and PTAA blend active layers were deposited by spin coating at 500 rpm for 10 sec and at 2000 rpm for 20 sec. Then, samples were annealed at 100°C for 15 min in a N₂-filled dry box. CYTOP (45 nm)/Al₂O₃ (50 nm) layers were used as top-gate dielectrics. CYTOP solution (CTL-809M) was purchased from Asahi Glass with a concentration of 9 wt. %. To deposit the 20 nm-thick CYTOP layers, the original solution diluted with their solvents (CT-solv. 180) to have solution:solvent ratios of 1:7. The 20 nm-thick CYTOP first layers were deposited by spin casting at 3000 rpm for 60 sec. The CYTOP (20 nm) films were annealed at 100°C for 20 min. Then, the Al₂O₃ dielectric films (50 nm) were deposited on top of the CYTOP layer using a Savannah 100 ALD system from Cambridge Nanotech Inc. Films were grown at 110°C using alternating exposures of trimethyl aluminum [Al(CH₃)₃] and H₂O vapor at a deposition rate of approximately 0.1 nm per cycle. The 20 nm-thick CYTOP third layers were deposited on the top of Al₂O₃ second layers. The CYTOP (20 nm) films were annealed at 100°C for 20 min. All spin coating and annealing processes were carried out in a N₂-filled dry box. Finally, Al (150 nm) gate electrodes were deposited by thermal evaporation through a shadow mask. The resulting OFET is depicted in FIG. 4F.

**EXAMPLE 11**

Pentacene and InGaZnO Based FETs and Inverters

Organic-inorganic hybrid complementary inverters were fabricated with a top gate and bottom-contact source and drain electrode geometry. First, Ti/Au (6 nm/50 nm) electrodes were deposited using electron-beam (e-beam) at room temperature on a glass substrate through a shadow mask to define the source and drain electrodes. Non-overlapping pentacene (hole transport) and a-IGZO (electron transport) channels horizontally distributed with different aspect ratios were fabricated on top of the source/drain electrodes. A 30 nm-thick a-IGZO (Ga₂O₃:In₂O₃:ZnO=1:1:1 mol %) active layer was deposited at room temperature by rf-sputtering through a shadow mask using a power of 125 W at a working pressure of 3 mtorr in an O₂/Ar (2%/98%) atmosphere. These structures were annealed at 300°C for 30 minutes in air. Then, a 50 nm-thick layer of pentacene was deposited through a shadow mask using thermal evaporation with a substrate temperature of 25°C and an initial pressure of 2×10⁻⁸ Torr. Prior to thermal evaporation, pentacene was purified using gradient zone sublimation. CYTOP (40 nm)/Al₂O₃ (50 nm) layers were used as top-gate dielectrics. CYTOP solution (CTL-809M) was purchased from Asahi Glass with a concentration of 9 wt. %. To deposit the 45 nm-thick CYTOP layers, the original solution diluted with their solvents (CT-solv. 180) to have solution:solvent ratios of 1:3.5. The 45 nm-thick CYTOP layers were deposited by spin casting at 3000 rpm for 60 sec. The CYTOP (45 nm) films were annealed at 100°C for 20 min. All spin coating and annealing processes were carried out in a N₂-filled dry box. Then, the Al₂O₃ dielectric films (50 nm) were deposited on top of the CYTOP layer.
using a Savannah 100 ALD system from Cambridge Nano­tech Inc. Films were grown at 110° C. using alternating exposures of trimethyl aluminum \([\text{Al(CH}_3\text{)}_3]\) and \(\text{H}_2\text{O}\) vapor at a deposition rate of approximately 0.1 nm per cycle. Finally, Al (50 nm) gate electrodes were deposited by thermal evaporation through a shadow mask. The resulting inverter is depicted in FIG. 4G.

**EXAMPLE 12**

Polyera ActivInk N2200 Based OPET with CYTOP/\(\text{Al}_2\text{O}_3\) Bi-Layer (45 Nm CYTOP; 50 nm \(\text{Al}_2\text{O}_3\)) and Evaporated Au Source/Drain Electrodes

OFETs with a bottom-contact and top-gate structure were fabricated on glass substrates (Corning, Eagle 2000). Au (50 nm) bottom-contact source/drain electrodes were deposited by thermal evaporation through a shadow mask. Inkjet printing semiconductor formulations are based on NDI polymer poly[[[N,N9-bis(2-octyldodecyl)-naphthalene-1,4,5,8-bis(dicarboximide)-2,6-diyl]alt-5,5-(2,2'-bithiophene)], (PNDI2OD-T2). Polyera ActivInk N2200. PNDI2OD-T2 ink was prepared as follows: NDI polymer was dissolved in a mixture of 1,2,3,4-tetrahydronaphthalene anhydrous, 99% (Sigma Aldrich) and mesitylene, 99% (Sigma Aldrich) with a ratio of 1:1 in volume in order to reach 0.5% concentration in active material. Formulation was stirred overnight in ambient. The structure of Polyera ActivInk N2200 is shown below:

A Dimatix DMP 2831 inkjet printing system was used to pattern semiconductor layers. Around 150 nm thick layer of active material was printing in air at room temperature. CYTOP (45 nm)/\(\text{Al}_2\text{O}_3\) (50 nm) layers were used as top-gate dielectrics. CYTOP solution (CTL-809M) was purchased from Asahi Glass with a concentration of 9 wt.%. To deposit the 45 nm-thick CYTOP layers, the original solution diluted with their solvents (CT-solv. 180) to have solution:solvent ratios of 1:3.5. The 45 nm-thick CYTOP layers were deposited by spin coating at 3000 rpm for 60 sec. The CYTOP (45 nm) films were annealed at 100° C, for 20 min. All spin coating and annealing processes were carried out in a \(\text{N}_2\)-filled dry box. Then, the \(\text{Al}_2\text{O}_3\) dielectric films (50 nm) were deposited on top of the CYTOP layer using a Savannah 100 ALD system from Cambridge Nanotech Inc. Films were grown at 110° C. using alternating exposures of trimethyl aluminum \([\text{Al(CH}_3\text{)}_3]\) and \(\text{H}_2\text{O}\) vapor at a deposition rate of approximately 0.1 nm per cycle. Finally, Al (100 nm) gate electrodes were deposited by thermal evaporation through a shadow mask. The resulting OFET is depicted in FIG. 4H.

**EXAMPLE 13**

Polyera ActivInk N2200 Based OPET with CYTOP/\(\text{Al}_2\text{O}_3\) Bi-Layer (45 Nm CYTOP; 50 nm \(\text{Al}_2\text{O}_3\)) and Evaporated Ag Source/Drain Electrodes

Example 13 is identical to example 12, except that Ag was used instead of Au in the bottom-contact source/drain electrodes.

**EXAMPLE 14**

Polyera ActivInk N2200 Based OPET with CYTOP/\(\text{Al}_2\text{O}_3\) Bi-Layer (45 Nm CYTOP; 50 nm \(\text{Al}_2\text{O}_3\)) and Printed Ag Source/Drain Electrodes

Example 14 is identical to example 14, except that the Ag bottom-contact source/drain electrodes were patterned by a Dimatix DMP 2831 inkjet printer.

**EXAMPLE 15**

LEH-III-002a Based OFET with CYTOP/\(\text{Al}_2\text{O}_3\) Bi-Layer (45 nm CYTOP; 50 nm \(\text{Al}_2\text{O}_3\))

OFETs with bottom contact and top gate structure were fabricated on glass substrates (Corning, Eagle 2000). Au (50 nm), Al (50 nm), and Ag (50 nm) bottom contact source/drain electrodes were deposited by thermal evaporation through a shadow mask. Thin films of organic semiconductors of LEH-III-002a (LEH-III-085g, LEH-119a) were deposited by spin coating with a 30 mg/ml solution prepared from dichlorobenzene at 500 rpm for 10 seconds followed by 2000 rpm for 20 seconds. LEH-III-002a (LEH-III-085g, LEH-III-119a) is shown in the formula below:

The blend for polymer matrix with poly(\(\alpha\)-methyl styrene) (P\(\alpha\)MS) (\(M_w\) = 100,000) was prepared from mixing separate 30 mg/ml solutions of LEH-III-119a (LEH-III-085g) and P\(\alpha\)MS. Poly(\(\alpha\)-methyl styrene) (P\(\alpha\)MS) (\(M_w\) = 100,000) is shown in the formula below:
The blend films were deposited by spin coating at 500 rpm for 10 seconds followed by at 2000 rpm for 20 seconds. The solvent and blend films were annealed at 100°C for 15 min. CYTOP (45 nm)/Al2O3 (50 nm) layers were used as top-gate dielectrics. CYTOP solution (CTL-809M) was purchased from Asahi Glass with a concentration of 9 wt. %. To deposit the 45 nm-thick CYTOP layers, the original solution diluted with their solvents (CT-solv. 180) to have solution:solvent ratios of 1:3.5. The 45 nm-thick CYTOP layers were deposited by spin casting at 3000 rpm for 60 sec. The CYTOP (45 nm) films were annealed at 100°C for 20 min. All spin coating and annealing processes were carried out in a N2-filled dry box. Then, the Al2O3 dielectric films (50 nm) were deposited on top of the CYTOP layer using a Savannah 100 ALD system from Cambridge Nanotech Inc. Films were grown at 110°C using alternating exposures of trimethyl aluminum [Al(CH3)3] and H2O vapor at a deposition rate of approximately 0.1 nm per cycle. Finally, Al (150 nm) gate electrodes were deposited by thermal evaporation through a shadow mask.

EXAMPLE 16

DRR-IV-209n Based OFET with CYTOP/Al2O3 Bi-Layer (45 nm CYTOP; 50 nm Al2O3)

OFETs with bottom contact and top gate structure were fabricated on glass substrates (Corning, Eagle 2000). Au (50 nm) bottom contact source/drain electrodes were deposited by thermal evaporation through a shadow mask. Organic semiconductor layers of DRR-IV-209n were formed on the substrates by spin coating from a solution prepared from 1,4-dioxane (20 mg/mL) and dichlorobenzene (20 mg/mL) at 500 rpm for 10 sec and at 2,000 rpm for 20 sec. DRR-IV-209n is shown in the formula below:

Then, samples were annealed at 100°C (1,4-dioxane sample) and 120°C (dichlorobenzene sample) for 10 min in a N2-filled dry box. CYTOP (45 nm)/Al2O3 (50 nm) layers were used as top-gate dielectrics. CYTOP solution (CTL-809M) was purchased from Asahi Glass with a concentration of 9 wt. %. To deposit the 45 nm-thick CYTOP layers, the original solution diluted with their solvents (CT-solv. 180) to have solution:solvent ratios of 1:3.5. The 45 nm-thick CYTOP layers were deposited by spin casting at 3000 rpm for 60 sec. The CYTOP (45 nm) films were annealed at 100°C for 20 min. All spin coating and annealing processes were carried out in a N2-filled dry box. Then, the Al2O3 dielectric films (50 nm) were deposited on top of the CYTOP layer using a Savannah 100 ALD system from Cambridge Nanotech Inc. Films were grown at 110°C using alternating exposures of trimethyl aluminum [Al(CH3)3] and H2O vapor at a deposition rate of approximately 0.1 nm per cycle. Finally, Al (150 nm) gate electrodes were deposited by thermal evaporation through a shadow mask.

As shown in FIG. 6B the effects on the change in voltage over the CYTOP layer in function of a change in dielectric constant of the Al2O3 layer is larger for smaller values of the CYTOP layer thickness. Such a slope is necessary in order to obtain the above described compensation effect. For thick CYTOP layers, e.g. the 500 nm curve in FIG. 6B, the curve is almost flat indicating that compensation will not be reached (wherein it is assumed that the other dielectric constants remain the same).

FIGS. 7A and 7B show the capacitance density-electric field (C-E) and current density-electric field (J-E) characteristics of Al2O3 (100 nm), CYTOP (780 nm), and CYTOP (40 nm)/Al2O3 (50 nm) films, respectively. The dielectric properties of all films were characterized using a parallel-plate capacitor geometry of gold (100 nm)/dielectric/indium thin oxide (ITO) coated glass with various areas ranging from 3.1x10-4 cm2 to 2.4x10-1 cm2. The measured capacitance densities (Cm) of the Al2O3 and CYTOP films at a frequency of 1 kHz were 78.6 and 2.3 nF/cm2, respectively. The...
extracted dielectric constant (k) values are 8.9 for Al2O3 and 2.0 for CYTOP. The CYTOP/Al2O3 bi-layer exhibited a C_m of 34.8 nF/cm2 at a frequency of 1 kHz, which is close to the theoretical value (34.6 nF/cm2) estimated from a series-connected capacitor of CYTOP and Al2O3. As shown in FIG. 7B, the leakage current densities of the Al2O3 and CYTOP/Al2O3 films remained below 3 × 10^-17 A/cm2 at applied fields with a magnitude up to 3 MV/cm. In contrast, the leakage current of a 780-nm-thick CYTOP film reached a value of 2 × 10^-7 A/cm2 at an applied field of 1.2 MV/cm.

FIGS. 8A-8B show the transfer and output characteristics, measured from pristine devices under a nitrogen atmosphere, of OFETs (W/L = 2550 μm/180 μm) using a CYTOP (40 nm)/Al2O3 (50 nm) gate dielectric. The OFETs showed no hysteresis and achieved a maximum value of μ = 0.6 cm2/Vs at a low voltage of 8 V due to the relatively high C_m of the bi-layer gate dielectric. Average values of the mobility μ = 0.46 ± 0.08 cm2/Vs, the threshold voltage V_th = -2.4 ± 0.1 V, and I_on/I_off = 10^5, the sub-threshold slope SS = 0.20 ± 0.06 V/decade and a maximum interfacial trap density of 5 × 10^11 cm^-2 were measured in these bi-layer devices. Compared with OFETs using the CYTOP single layer, OFETs using the bi-layer show similar values of μ but smaller values of V_th and SS and higher values of I_on/I_off at low operating voltages due to the high C_m.

FIG. 9A shows a table that summarizes the different conditions of environmental exposure and electrical stress to which each set of OFETs was subjected to study their long-term environmental and operational stabilities. To study their environmental stability, all OFETs were exposed to a nitrogen environment at a relative humidity between 30 and 50%. Variations of μ and V_th were monitored at discrete intervals. At each interval, each substrate was transferred back into a N2-filled glove box for electrical measurements and operational stability tests.

FIG. 9B shows that, in the different types of OFETs, no significant change in μ was observed after up to 31 days of exposure to air. As will be shown, the good air stability of TIPS-pentacene also contributes to the environmental stability of these OFETs. In OFETs with the Al2O3 gate dielectric, a gradual increase of the average value of μ from 5.5 (±2.0) × 10^-3 cm2/Vs up to 1.1 (±0.4) × 10^-2 cm2/Vs was observed. In the other OFETs, after an initial increase within the first eleven days, μ remained unchanged with average values of 0.60 ± 0.20 cm2/Vs for OFETs with the CYTOP gate dielectric and 0.52 ± 0.09 cm2/Vs for OFETs with the CYTOP/Al2O3 gate dielectric. On the other hand, the variations of V_th for the devices with different gate dielectrics are shown in FIG. 9C. In OFETs with the Al2O3 gate dielectric, the average value of V_th, measured from sweeps of V_GS from off-to-on regime, varied from -2.4 ± 0.3 V to -2.8 ± 0.5 V after 31 days in air. Despite this seemingly small change, strong hysteresis and large device-to-device variation of the magnitude and sign of V_th were observed in these devices. In contrast, in hysteresis-free OFETs with the CYTOP gate dielectric, a large positive shift in V_th from -2.3 ± 0.8 V to -4.0 ± 0.7 V was observed after 11 days in air. After this initial variation, no serious shift in V_th was observed, reaching a value of -3.7 ± 0.3 V after 31 days in air. Similar changes, albeit of a smaller magnitude, were observed in hysteresis-free OFETs with the CYTOP/Al2O3 bi-layer. After 31 days in air, only a minor shift in V_th from -2.5 ± 0.1 V to -1.4 ± 0.1 V was measured. As in devices with the CYTOP gate dielectric, most of these changes happened within the first 11 days.

FIG. 9D shows the variations of the mobility and the threshold voltage V_th for an OFET with a CYTOP (40 nm)/Al2O3 (50 nm) film.

To study the encapsulation properties of our top-gate dielectrics, Ca thin-film optical transmission tests were carried out. It was found that Ca films protected with a CYTOP single layer rapidly oxidized within an hour of being exposed to air, while Ca films protected with either a CYTOP/Al2O3 bi-layer or an Al2O3 single layer started degradation only after being exposed to air for more than a day. From these experiments, it is expected that CYTOP is a protective barrier for H2O diffusion due to its hydrophobic nature, so O2 diffusion should be responsible for the degradation of the Ca layers. OFETs using the bi-layer gate dielectric showed superior environmental stability compared with those using single-layer gate dielectrics.

The encapsulation properties of the dielectrics used in the top-gate OFETs were further tested, after 31 days in air, by exposing them to an O2 plasma for 5 min at a power of 750 W, a condition which is more severe than air exposure due to the high reactivity of the O2 plasma. To study the effects of the O2 plasma, no significant changes in μ or V_th were observed for all three types of OFETs. A significant change observed in the electrical characteristics of the different OFETs was a large positive change in I_on/I_off in the OFETs with a single CYTOP layer. On the other hand, Al2O3 acts as a protective layer to the energetic O2 plasma, so no significant changes in the I_on/I_off ratios were observed in the devices with Al2O3 and CYTOP/Al2O3 gate dielectrics. As described in FIG. 9A, after O2 plasma treatment, the electrical properties of the OFETs with a CYTOP/Al2O3 bi-layer were tested after an accumulated air exposure up to 210 days (7 months). FIGS. 9B and 9C show that the average values of μ and V_th remain practically unchanged.

In addition to the environmental stability, the operational stability is of critical importance for circuit design and overall device lifetime. The mechanisms of degradation under continuous operation are related to charge trapping and de-trapping events at all of the critical interfaces in an OFET and in the bulk of the semiconductor and gate dielectric. The degradation of the performance of an OFET during operation is reflected in changes of μ and V_th. Because the trap dynamics depend on the density of carriers flowing through the channel, a more severe degradation is expected when transistors are operated at higher powers. Other mechanisms like the diffusion of mobile impurities or the polarization of the gate dielectric could also contribute to the degradation of the performance. For these reasons, the operational stability of all OFETs was evaluated in two ways: 1) by multiple continuous scans of the transfer characteristic and 2) by applying a constant direct current (DC) bias stress, a more severe condition due to the higher current densities flowing through the channel.

FIGS. 10A and 10B show a sampling of the transfer curves measured in a CYTOP (40 nm)/Al2O3 (50 nm) OFET during multiple continuous scans from the "off" to the "on" region, before (FIG. 10A) and after (FIG. 10B) air exposure for 31 days. Negligible changes in the transfer characteristics, during the first 1000 scans, were observed in OFETs with a CYTOP/Al2O3 gate dielectric, as shown in the inset of FIG. 10A, before the OFETs were exposed to air. To further test the operational stability of these devices before exposing them to air, both were subjected to an additional 20,000 scans. FIG. 10A shows that even under such conditions, negligible changes were observed in the transfer characteristics of both kinds of OFETs. Even after being exposed to air for 31 days, the operational stability under multiple continuous scans was preserved, as shown in FIG. 10B. This remarkable stability is
a consequence of the excellent electrical properties of the CYTOP/TIPS-pentacene interface.

As shown in FIG. 9A, before exposing the OFETs to air and after 1000 scans, devices 1 of the different types of OFETs were subjected to 3600 s (1 h) of DC bias stress. FIG. 11A shows the temporal evolution of the \( I_{DS} \) measured in all OFETs normalized to the initial value. In the OFET with the Al2O3 gate dielectric, a drop in the normalized \( I_{DS} \) was measured, reaching a final value of 0.77 after 1 h. During the same interval, the current measured in a CYTOP device dropped to 0.9. However, the evolution of the CYTOP/Al2O3 bi-layer is different in that the current slightly increases, reaching a value of 1.04 after 1 h. FIG. 11B shows the evolution of the normalized \( I_{DS} \) measured in all OFETs for 1 h bias stress after 31 days of exposure to air (devices 2). In OFETs with the bi-layer gate dielectric, the mechanism driving the slight increase of \( I_{DS} \) is significantly different from the one observed in the other OFETs. Furthermore, the operational stability of OFETs with the bi-layer gate dielectric was tested after O2 plasma treatment by monitoring the current change over 24 h of electrical bias stress. FIG. 11C shows that changes in the normalized \( I_{DS} \) remain below 4% its original value. As shown in FIG. 11D, this remarkable stability results in negligible changes of the transfer and output characteristics before and after DC bias stress. It should be noted that, as found before, \( I_{DS} \) shows a slight increase during the initial stages of the DC bias stress but slowly decreased after prolonged stress. FIG. 11E shows the temporal evolution of the \( I_{DS} \) over 24 h of electrical bias stress measured in an OFET with a CYTOP (40 nm)/Al2O3 (50 nm) film for: a pristine OFET (Dev. 1), after 31 days of exposure in air (Dev. 2), after O2 plasma treatment (Dev. 3), after air exposure 90 days (Dev. 4), after air exposure for 150 days (Dev. 5), after air exposure for 210 days (Dev. 6), and after air exposure for 365 days (Dev. 7). As can be seen, the variation of \( I_{DS} \) under DC bias was less than ±10%.

The remarkable stability of the OFETs with the bi-layers under electrical bias arises from compensating effects: 1) a decrease in \( I_{DS} \) caused by intrinsic deep traps at the CYTOP/TIPS-pentacene interface and 2) an increase in \( I_{DS} \) caused by dipoles that can be oriented at the CYTOP/Al2O3 interface and/or by charge injection and trapping at the gate dielectric. Systematic Stability Study on OFETs with CYTOP/Al2O3 Bi-Layer Dielectric

For illustrating the advantages of the embodiments of the invention, the following study has been made on OFETs with CYTOP/Al2O3 bi-layer dielectric. The effects of O2 and H2O exposure on p-channel OFETs were studied. The generalized effects of O2 and H2O exposure on the transfer characteristics of such OFETs is depicted in FIGS. 16A and 16B. FIG. 16A shows that O2 has both doping and oxidation effects, the doping effect tending to shift the transfer characteristic curve to the right, and the oxidation effect tending to shift the transfer characteristic curve to the left. FIG. 16B shows that H2O increases dielectric polarization, which tends to shift the transfer characteristic curve to the right, but also has the effect of trap creation, which tends to shift the transfer characteristic curve to the left.

The generalized effects of O2 and H2O exposure on the temporal evolution of the \( I_{DS} \) during DC bias stress are shown in FIG. 16C. FIG. 16C shows that O2 exposure has little effect on \( I_{DS} \) during DC bias stress. H2O exposure, however, causes a decrease in \( I_{DS} \) over time during DC bias stress.

To test the extent of these effects, three different OFETs were tested. The first was a TIPS-pentacene and PTAA blend channel based OFET with a CYTOP/Al2O3 bi-layer (45 nm CYTOP, 50 nm Al2O3), as shown in FIG. 4D. The second was a PTAA blend channel based OFET with a CYTOP/Al2O3 bi-layer (45 nm CYTOP, 50 nm Al2O3, 20 nm CYTOP), as shown in FIG. 4F. The OFETs were subject to the exposure sequence shown in FIG. 17.

Figs. 18A-18C show the capacitance \( C_{p}(\mu F/cm^2) \), mobility \( \mu (cm^2/Vs) \), and threshold voltage \( V_{th}(V) \) for each stage of the exposure sequence. These results indicate that the effects of O2 and H2O are reversible for CYTOP/Al2O3 bi-layer and CYTOP/Al2O3/CYTOP tri-layer OFETs.

Figs. 19A and 19B show the variation in capacitance for frequencies ranging from 20 Hz to 1 million Hz for the CYTOP/Al2O3 bi-layer (45 nm CYTOP; 50 nm Al2O3) (FIG. 19A) and the CYTOP/Al2O3/CYTOP tri-layer OFET (20 nm CYTOP; 50 nm Al2O3; 20 nm CYTOP) (FIG. 19B), at each stage of the exposure sequence.

Figs. 20A and 20B show the transfer characteristics and temporal evolution of the \( I_{DS} \) during DC bias for the TIPS-pentacene and PTAA blend channel based OFET with a CYTOP/Al2O3 bi-layer (45 nm CYTOP; 50 nm Al2O3). The data obtained during testing of the OFET is summarized in the table below.

<table>
<thead>
<tr>
<th>Average 9 devices</th>
<th>( C_{p}(\mu F/cm^2) )</th>
<th>W/L</th>
<th>( \mu (cm^2/Vs) )</th>
<th>( V_{th}(V) )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pristine</td>
<td>35.2 ± 0.3</td>
<td>2550 nm/180 µm</td>
<td>0.57 ± 0.11</td>
<td>-3.4 ± 0.2</td>
</tr>
<tr>
<td>Dry O2</td>
<td>35.2 ± 0.3</td>
<td>2550 nm/180 µm</td>
<td>0.69 ± 0.14</td>
<td>-2.7 ± 0.3</td>
</tr>
<tr>
<td>Vacuum</td>
<td>35.0 ± 0.3</td>
<td>2550 nm/180 µm</td>
<td>0.61 ± 0.12</td>
<td>-3.4 ± 0.2</td>
</tr>
<tr>
<td>Humid air</td>
<td>37.5 ± 0.3</td>
<td>2550 nm/180 µm</td>
<td>0.61 ± 0.12</td>
<td>-2.6 ± 0.2</td>
</tr>
<tr>
<td>H2O (water)</td>
<td>34.0 ± 0.1</td>
<td>2550 nm/180 µm</td>
<td>0.64 ± 0.14</td>
<td>-3.4 ± 0.3</td>
</tr>
<tr>
<td>Vacuum</td>
<td>35.7 ± 0.3</td>
<td>2550 nm/180 µm</td>
<td>0.65 ± 0.15</td>
<td>-2.4 ± 0.2</td>
</tr>
<tr>
<td>Humid air</td>
<td>34.5 ± 0.3</td>
<td>2550 nm/180 µm</td>
<td>0.66 ± 0.14</td>
<td>-3.3 ± 0.3</td>
</tr>
</tbody>
</table>

of the \( I_{DS} \) during DC bias for the diF-TESADT and PTAA blend channel based OFET with a CYTOP/Al2O3 bi-layer (45 nm CYTOP; 50 nm Al2O3). The data obtained during testing of the OFET is summarized in the table below.

<table>
<thead>
<tr>
<th>Average 7 devices</th>
<th>( C_{p}(\mu F/cm^2) )</th>
<th>W/L</th>
<th>( \mu (cm^2/Vs) )</th>
<th>( V_{th}(V) )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pristine</td>
<td>35.2 ± 0.3</td>
<td>2550 nm/180 µm</td>
<td>1.21 ± 0.51</td>
<td>-3.1 ± 0.2</td>
</tr>
<tr>
<td>Dry O2</td>
<td>35.2 ± 0.3</td>
<td>2550 nm/180 µm</td>
<td>1.25 ± 0.51</td>
<td>-2.5 ± 0.2</td>
</tr>
<tr>
<td>Vacuum</td>
<td>35.0 ± 0.3</td>
<td>2550 nm/180 µm</td>
<td>1.21 ± 0.51</td>
<td>-3.0 ± 0.1</td>
</tr>
<tr>
<td>Humid air</td>
<td>37.5 ± 0.3</td>
<td>2550 nm/180 µm</td>
<td>1.19 ± 0.50</td>
<td>-2.5 ± 0.3</td>
</tr>
<tr>
<td>Vacuum</td>
<td>34.5 ± 0.3</td>
<td>2550 nm/180 µm</td>
<td>1.18 ± 0.50</td>
<td>-2.9 ± 0.3</td>
</tr>
</tbody>
</table>

FIGS. 22A and 22B show the transfer characteristics and temporal evolution of the \( I_{DS} \) during DC bias for the TIPS-pentacene and PTAA blend channel based OFET with a CYTOP/Al2O3/CYTOP tri-layer (20 nm CYTOP; 50 nm Al2O3; 20 nm CYTOP). The data obtained during testing of the OFET is summarized in the table below.
Comparative Study on Various Fluoropolymer (CYTOP, Hyflon, and Teflon)/Inorganic (Al₂O₃ and Si₃N₄) Bi-Layers

For illustrating the advantages of the embodiments of the invention, the following study has been made of capacitors deposited on fluoropolymer layers by plasma enhanced chemical vapor deposition (PECVD) at 110° C. For triple layer dielectrics, CYTOP films (20 nm) deposited on Al₂O₃ and Si₃N₄ films and annealed at 100° C. for 20 min. Finally, Al (150 nm) top electrodes were deposited by thermal evaporation through a shadow mask.

FIGS. 23A-23D show the capacitance and current density-electric field (J-E) characteristics of the tested capacitors. A summary of the dielectric properties of the tested capacitors is contained in the Table below.

<table>
<thead>
<tr>
<th>Dielectric type</th>
<th>Cᵣ (nF/cm²) at 1 KHz</th>
<th>Breakdown field (MV/cm) @ J = 10⁻⁶ A/cm²</th>
</tr>
</thead>
<tbody>
<tr>
<td>CYTOP (45 nm)/Al₂O₃(50 nm)</td>
<td>35.2 ± 0.3</td>
<td>Over 3.3 MV/cm</td>
</tr>
<tr>
<td>CYTOP (20 nm)/Al₂O₃(50 nm)</td>
<td>34.6 ± 0.1</td>
<td>Over 3.3 MV/cm</td>
</tr>
<tr>
<td>CYTOP (20 nm)/Al₂O₃(50 nm)/CYTOP (20 nm)</td>
<td>30.1 ± 0.1</td>
<td>3 MV/cm</td>
</tr>
<tr>
<td>CYTOP (45 nm)/Si₃N₄(50 nm)</td>
<td>34.7 ± 0.3</td>
<td>Over 3.3 MV/cm</td>
</tr>
<tr>
<td>CYTOP (45 nm)/Si₃N₄(50 nm)/CyTOP (20 nm)</td>
<td>32.2 ± 0.2</td>
<td>Over 3.3 MV/cm</td>
</tr>
<tr>
<td>CYTOP (45 nm)/Si₃N₄(50 nm)</td>
<td>32.1 ± 0.2</td>
<td>Over 3.3 MV/cm</td>
</tr>
<tr>
<td>CYTOP (45 nm)/Si₃N₄(50 nm)</td>
<td>31.1 ± 0.3</td>
<td>Over 3.3 MV/cm</td>
</tr>
<tr>
<td>CYTOP (45 nm)/Si₃N₄(50 nm)</td>
<td>32.3 ± 0.2</td>
<td>Over 3.3 MV/cm</td>
</tr>
</tbody>
</table>

To prepare the OFETs, a bottom-contact and top-gate structure were fabricated on glass substrates (Corning, Eagle 2000). Au (50 nm) bottom-contact source/drain electrodes were deposited by thermal evaporation through a shadow mask. A self-assembled monolayer of pentafluorobenzene thiol (PFBT) was formed on the Au electrodes by immersion in a 10 mmol PFBT solution in ethanol for 15 min in a N₂-filled dry box, rinsing with pure ethanol, and drying. The TIPS-pentacene and PTAA blend solution was prepared as follows: TIPS-pentacene and PTAA were individually dissolved in 1,2,3,4-Tetrahydrodronaphthalene anhydrous, 99%, (Sigma Aldrich) for a concentration of 30 mg/mL and the two individual solutions were mixed to yield a weight ratio of 1:1. TIPS-pentacene and PTAA blend active layers were deposited by spin coating at 500 rpm for 10 sec and at 2000 rpm for 20 sec. Then, samples were annealed at 100° C. for 15 min in a N₂-filled dry box. Various fluoropolymer (CYTOP, Hyflon, and Teflon)/Inorganic (Al₂O₃ and Si₃N₄) bi-layers and CYTOP/inorganic (Al₂O₃ and Si₃N₄)/CYTOP triple layers were used as dielectrics. CYTOP solution (CTL-809M) was purchased from Asahi Glass with a concentration of 9 wt. %. Hyflon solution (Hyflon® AD 40X) was received from Solvay, of which concentration is ~6.6 wt %. Teflon solution (601S2-100-6) was purchased from DuPont with a concentration of 6 wt %. To deposit the 45-nm-thick fluoropolymer layers, the original solutions were diluted with their solvents (CT-solv. 180 for CYTOP, LS165 for Hyflon, and FC-40 for Teflon) to have solution:solvent ratios of 1:3.5 for CYTOP, 1:2 for Hyflon, and 1:3 for Teflon. For 20 nm CYTOP layers, the solution:solvent ratio is 1:7. Fluoropolymer layers were deposited by spin coating at 3000 (for CYTOP) and at 4000 rpm (for Hyflon and Teflon) for 60 sec. After deposition, fluoropolymer layers were annealed at 100° C. for 20 min. Then, the Al₂O₃ dielectric films (50 nm) were deposited on top of the fluoropolymer layer using a Savannah 100 ALD system from Cambridge Nanotech Inc. Films were grown at 110° C. using alternating exposures of trimethyl aluminum [Al(CH₃)₃] and H₂O vapor at a deposition rate of approximately 0.1 nm per cycle. Si₃N₄ films (50 nm) were deposited by spin coating at 30000 (for CYTOP) and at 4000 rpm (for Hyflon, Teflon) for 60 sec. After deposition, fluoropolymer layers were annealed at 100° C. for 20 min. Then, the Al₂O₃ dielectric films (50 nm) were deposited on top of the fluoropolymer layer using a Savannah 100 ALD system from Cambridge Nanotech Inc. Films were fabricated at 110° C. using alternating exposures of trimethyl aluminum [Al(CH₃)₃] and H₂O vapor at a deposition rate of approximately 0.1 nm per cycle. Si₃N₄ films (50 nm) were deposited by spin coating at 30000 (for CYTOP) and at 4000 rpm (for Hyflon, Teflon) for 60 sec. After deposition, fluoropolymer layers were annealed at 100° C. for 20 min. Then, the Al₂O₃ dielectric films (50 nm) were deposited on top of the fluoropolymer layer using a Savannah 100 ALD system from Cambridge Nanotech Inc. Films were fabricated at 110° C. using alternating exposures of trimethyl aluminum [Al(CH₃)₃] and H₂O vapor at a deposition rate of approximately 0.1 nm per cycle. Si₃N₄ films (50 nm) were deposited by spin coating at 30000 (for CYTOP) and at 4000 rpm (for Hyflon, Teflon) for 60 sec. After deposition, fluoropolymer layers were annealed at 100° C. for 20 min. Then, the Al₂O₃ dielectric films (50 nm) were deposited on top of the fluoropolymer layer using a Savannah 100 ALD system from Cambridge Nanotech Inc. Films were fabricated at 110° C. using alternating exposures of trimethyl aluminum [Al(CH₃)₃] and H₂O vapor at a deposition rate of approximately 0.1 nm per cycle. Si₃N₄ films (50 nm) were deposited by spin coating at 30000 (for CYTOP) and at 4000 rpm (for Hyflon, Teflon) for 60 sec. After deposition, fluoropolymer layers were annealed at 100° C. for 20 min. Then, the Al₂O₃ dielectric films (50 nm) were deposited on top of the fluoropolymer layer using a Savannah 100 ALD system from Cambridge Nanotech Inc. Films were fabricated at 110° C. using alternating exposures of trimethyl aluminum [Al(CH₃)₃] and H₂O vapor at a deposition rate of approximately 0.1 nm per cycle. Si₃N₄ films (50 nm) were
0.1 nm per cycle. SiN films (50 nm) were deposited on fluoropolymer layers by plasma enhanced chemical vapor deposition (PECVD) at 110°C. For triple layer dielectrics, CYTOP films (20 nm) were deposited on top of Al$_2$O$_3$ and SiN films and annealed at 100°C for 20 min. Finally, Al (150 nm) gate electrodes were deposited by thermal evaporation through a shadow mask.

FIGS. 24A and 24B show the transfer characteristic and output characteristics for the CYTOP (45 nm)/Al$_2$O$_3$ (50 nm) bi-layer OFET. FIGS. 24C and 24D show the transfer characteristic and output characteristics for the Hyflon (45 nm)/Al$_2$O$_3$ (50 nm) bi-layer OFET. FIGS. 24E and 24F show the transfer characteristic and output characteristics of the Teflon (45 nm)/Al$_2$O$_3$ (50 nm) bi-layer OFET. FIGS. 24G and 24H show the transfer characteristic and output characteristics for the CYTOP (20 nm)/Al$_2$O$_3$ (50 nm)/CYTOP (20 nm) tri-layer OFET. FIGS. 24I and 24J show the transfer characteristic and output characteristics for the CYTOP (45 nm)/SiN$_x$ (50 nm) bi-layer OFET. FIGS. 24K and 24L show the transfer characteristic and output characteristics for the Hyflon (45 nm)/SiN$_x$ (50 nm) bi-layer OFET. FIGS. 24M and 24N show the transfer characteristic and output characteristics for the Teflon (45 nm)/SiN$_x$ (50 nm) bi-layer OFET. FIGS. 24O and 24P show the transfer characteristic and output characteristics for the CYTOP (20 nm)/SiN$_x$ (50 nm)/CYTOP (20 nm) tri-layer OFET.

A summary of the performance of the tested OFETs is contained in the below table.

<table>
<thead>
<tr>
<th>Dielectric</th>
<th>W/L</th>
<th>C$_{in}$ (μF/cm$^2$)</th>
<th>μ (cm$^2$/Vs)</th>
<th>V$_{th}$ (V)</th>
<th>I$_{on-off}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>CYTOP (40 nm)/Al$_2$O$_3$</td>
<td>2550 nm/180 μm</td>
<td>35.2</td>
<td>0.98 ± 0.17</td>
<td>−3.7 ± 0.6</td>
<td>3 x 10$^4$</td>
</tr>
<tr>
<td>(50 nm)</td>
<td>(ave. 7)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Hyflon (40 nm)/Al$_2$O$_3$</td>
<td>2550 nm/180 μm</td>
<td>39.1</td>
<td>0.70 ± 0.00</td>
<td>−3.7 ± 0.2</td>
<td>10$^3$</td>
</tr>
<tr>
<td>(50 nm)</td>
<td>(ave. 7)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Teflon (40 nm)/Al$_2$O$_3$</td>
<td>2550 nm/180 μm</td>
<td>34.7</td>
<td>0.67 ± 0.16</td>
<td>−4.1 ± 0.5</td>
<td>3 x 10$^3$</td>
</tr>
<tr>
<td>(50 nm)</td>
<td>(ave. 8)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CYTOP (20 nm)/Al$_2$O$_3$</td>
<td>2550 nm/180 μm</td>
<td>34.6</td>
<td>0.69 ± 0.22</td>
<td>−3.4 ± 0.4</td>
<td>5 x 10$^3$</td>
</tr>
<tr>
<td>(50 nm)</td>
<td>(ave. 7)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CYTOP (20 nm)</td>
<td>2550 nm/180 μm</td>
<td>32.2</td>
<td>0.044 ± 0.025</td>
<td>−8.5 ± 0.4</td>
<td>10$^4$</td>
</tr>
<tr>
<td>(50 nm)</td>
<td>(ave. 8)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Hyflon (40 nm)/SiN$_x$</td>
<td>2550 nm/180 μm</td>
<td>31.1</td>
<td>0.009 ± 0.005</td>
<td>−8.2 ± 0.4</td>
<td>5 x 10$^3$</td>
</tr>
<tr>
<td>(50 nm)</td>
<td>(ave. 7)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Teflon (40 nm)/SiN$_x$</td>
<td>2550 nm/180 μm</td>
<td>32.3</td>
<td>0.005 ± 0.001</td>
<td>−6.7 ± 0.5</td>
<td>10$^3$</td>
</tr>
<tr>
<td>(50 nm)</td>
<td>(ave. 8)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CYTOP (20 nm)/SiN$_x$</td>
<td>2550 nm/180 μm</td>
<td>32.1</td>
<td>0.019 ± 0.008</td>
<td>−8.2 ± 0.4</td>
<td>10$^3$</td>
</tr>
<tr>
<td>(50 nm)/CYTOP (20 nm)</td>
<td>(ave. 8)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

It should be noted that field-effect mobility values for fluoropolymer/SiN$_x$ bi-layer OFETs were 10-100 times lower than those for fluoropolymer/Al$_2$O$_3$ bi-layer OFETs. Results Yielded by Other Embodiments.

FIGS. 12A and 12B show the transfer and output characteristics of amorphous InGaZnO FETs with the CYTOP (40 nm)/Al$_2$O$_3$ (50 nm) bi-layer after multiple scans of the transfer characteristic up to 1,000 cycles and after a constant DC bias stress for 8 hour (V$_{gs}$=V$_{ds}$=7 V). Under continuous multiple scans or under a constant DC bias stress, the oxide FET shows no degradation of mobility but a slight change in the threshold voltage.

FIGS. 13A-13B show the transfer and output characteristics, measured from pristine devices under a nitrogen atmosphere, of OFETs (W/L=2550 nm/180 μm) using a CYTOP (40 nm)/Al$_2$O$_3$ (50 nm) gate dielectric and a plastic (PES) substrate, as discussed in Examiner 7. The OFETs showed no hysteresis and achieved a maximum value of μ=0.34 cm$^2$/Vs at a low voltage of 8 V. Average values of the mobility characteristics and output characteristics of the pentacene FETs discussed in Example 11. FIGS. 27A and 27B show the transfer characteristics and output characteristics of the InGaZnO FETs discussed in Example 11. FIGS. 28A and 28B show the voltage transfer characteristics and static gain of the inverter of FIG. 4G.

FIGS. 29A and 29B show the transfer characteristics and output characteristics of a Polyera ActivInk N2200 based OFET with a CYTOP/Al$_2$O$_3$ bi-layer (45 nm CYTOP; 50 nm Al$_2$O$_3$) and evaporated Ag source/drain electrodes, as discussed in Example 12. FIGS. 30A and 30B show the transfer characteristics and output characteristics of a Polyera ActivInk N2200 based OFET with a CYTOP/Al$_2$O$_3$ bi-layer (45 nm CYTOP; 50 nm Al$_2$O$_3$) and evaporated Au source/drain electrodes, as discussed in Example 13. FIGS. 31A and 31B show the transfer characteristics and output characteristics of a Polyera ActivInk N2200 based OFET with a CYTOP/Al$_2$O$_3$ bi-layer (45 nm CYTOP; 50 nm Al$_2$O$_3$) and printed Ag source/drain electrodes, as discussed in Example 14.
mary of the performance of the printed tested printed OFETs is contained in the table below.

<table>
<thead>
<tr>
<th>compound</th>
<th>W/L</th>
<th>C&lt;sub&gt;in&lt;/sub&gt; (nF/cm&lt;sup&gt;2&lt;/sup&gt;)</th>
<th>S/D electrode</th>
<th>µ (cm&lt;sup&gt;2&lt;/sup&gt;/V·s)</th>
<th>V&lt;sub&gt;TH&lt;/sub&gt; (V)</th>
<th>Ion/off</th>
</tr>
</thead>
<tbody>
<tr>
<td>P(ND203T2)-Polyera N2200</td>
<td>2000 µm/180 µm</td>
<td>34.8</td>
<td>evaporated Au</td>
<td>0.08</td>
<td>0.14</td>
<td>2 x 10^3</td>
</tr>
<tr>
<td></td>
<td>2000 µm/180 µm</td>
<td>34.8</td>
<td>evaporated Ag</td>
<td>0.11</td>
<td>0.22</td>
<td>8 x 10^3</td>
</tr>
<tr>
<td></td>
<td>2000 µm/180 µm</td>
<td>34.8</td>
<td>printed Ag</td>
<td>0.16</td>
<td>1.6</td>
<td>3 x 10^3</td>
</tr>
</tbody>
</table>

FIGS. 32A and 32B show the transfer characteristics and output characteristics of an LEH-III-002a based OFET with a CYTOP/Al<sub>2</sub>O<sub>3</sub> bi-layer (45 nm CYTOP; 50 nm Al<sub>2</sub>O<sub>3</sub>) and Au bottom contact source/drain electrodes in n-channel operation.

FIGS. 33A and 33B show the transfer characteristics and output characteristics of an LEH-III-085g based OFET with a CYTOP/Al<sub>2</sub>O<sub>3</sub> bi-layer (45 nm CYTOP; 50 nm Al<sub>2</sub>O<sub>3</sub>) and Au bottom contact source/drain electrodes in p-channel operation.

FIGS. 34A and 34B show the transfer characteristics and output characteristics of an LEH-III-085g:PaMS based OFET with a CYTOP/Al<sub>2</sub>O<sub>3</sub> bi-layer (45 nm CYTOP; 50 nm Al<sub>2</sub>O<sub>3</sub>) and Ag bottom contact source/drain electrodes in p-channel operation.

FIGS. 35A and 35B show the transfer characteristics and output characteristics of a DRR-IV-209n based OFET with a CYTOP/Al<sub>2</sub>O<sub>3</sub> bi-layer (45 nm CYTOP; 50 nm Al<sub>2</sub>O<sub>3</sub>) and Au bottom contact source/drain electrodes.

A summary of the performance of the LEH-III-002a, LEH-III-085g, LEH-III-119a, DRR-IV-209n based OFETs is shown in the tables below.

### LEH-III-002a and LEH-III-085g

<table>
<thead>
<tr>
<th>Batch</th>
<th>Mode</th>
<th>W/L</th>
<th>S/D electrode</th>
<th>C&lt;sub&gt;in&lt;/sub&gt; (nF/cm&lt;sup&gt;2&lt;/sup&gt;)</th>
<th>µ (cm&lt;sup&gt;2&lt;/sup&gt;/V·s)</th>
<th>V&lt;sub&gt;TH&lt;/sub&gt; (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LEH-III-002a</td>
<td>Ambipolar (n-mode)</td>
<td>6050 µm/180 µm</td>
<td>Au</td>
<td>34.8</td>
<td>1.1 ±0.3</td>
<td>13.1 ±1.1</td>
</tr>
<tr>
<td></td>
<td>Ambipolar (p-mode)</td>
<td>6050 µm/180 µm</td>
<td>Au</td>
<td>34.8</td>
<td>5.7 ±3.3 / 10&lt;sup&gt;-3&lt;/sup&gt;</td>
<td>-14.8 ±0.8</td>
</tr>
<tr>
<td>LEH-III-085g</td>
<td>Only n-channel</td>
<td>2550 µm/180 µm</td>
<td>Al</td>
<td>34.8</td>
<td>0.16 ±0.02</td>
<td>0.01 ±0.02</td>
</tr>
<tr>
<td>LEH-III-085g:PaMS</td>
<td>Ambipolar (n-mode)</td>
<td>6050 µm/180 µm</td>
<td>Ag</td>
<td>34.8</td>
<td>0.72 ±0.05</td>
<td>12.9 ±0.3</td>
</tr>
<tr>
<td></td>
<td>Ambipolar (p-mode)</td>
<td>6050 µm/180 µm</td>
<td>Ag</td>
<td>34.8</td>
<td>6.3 ±1.0 / 10&lt;sup&gt;-3&lt;/sup&gt;</td>
<td>-11.7 ±1.1</td>
</tr>
</tbody>
</table>

OFET with a CYTOP/Al<sub>2</sub>O<sub>3</sub> bi-layer (45 nm CYTOP; 50 nm Al<sub>2</sub>O<sub>3</sub>) and Ag bottom contact source/drain electrodes in p-channel operation.

### LEH-III-119a Ambient Stability

<table>
<thead>
<tr>
<th>Batch</th>
<th>Ambient exposure</th>
<th>W/L</th>
<th>S/D electrode</th>
<th>C&lt;sub&gt;in&lt;/sub&gt; (nF/cm&lt;sup&gt;2&lt;/sup&gt;)</th>
<th>µ (cm&lt;sup&gt;2&lt;/sup&gt;/V·s)</th>
<th>V&lt;sub&gt;TH&lt;/sub&gt; (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LEH-III-119a</td>
<td>Pristine</td>
<td>6050 µm/180 µm</td>
<td>Au</td>
<td>34.8</td>
<td>0.07</td>
<td>14.3</td>
</tr>
<tr>
<td></td>
<td>5 days in air</td>
<td>6050 µm/180 µm</td>
<td>Au</td>
<td>34.8</td>
<td>0.67</td>
<td>15.1</td>
</tr>
<tr>
<td></td>
<td>17 days in air</td>
<td>6050 µm/180 µm</td>
<td>Au</td>
<td>34.8</td>
<td>0.43</td>
<td>17.1</td>
</tr>
<tr>
<td></td>
<td>18 hrs vacuum annealing at 100° C.</td>
<td>6050 µm/180 µm</td>
<td>Au</td>
<td>34.8</td>
<td>0.51</td>
<td>17.0</td>
</tr>
<tr>
<td>LEH-III-119a:PaMS</td>
<td>Pristine</td>
<td>6050 µm/180 µm</td>
<td>Au</td>
<td>34.8</td>
<td>0.61</td>
<td>12.8</td>
</tr>
<tr>
<td></td>
<td>5 days in air</td>
<td>6050 µm/180 µm</td>
<td>Au</td>
<td>34.8</td>
<td>0.55</td>
<td>13.8</td>
</tr>
</tbody>
</table>

FIGS. 37A and 37B show the results of an ambient exposure study on the LEH-III-119a based OFET with a CYTOP/Al<sub>2</sub>O<sub>3</sub> bi-layer (45 nm CYTOP; 50 nm Al<sub>2</sub>O<sub>3</sub>) and Au bottom contact source/drain electrodes. FIG. 37A shows the transfer characteristics of this OFET initially, after 5 days, after 17 days, and after annealing. FIG. 37B shows the mobility and threshold voltages of this OFET initially, after 5 days, and after 17 days.

FIGS. 38A and 38B show the results of an ambient exposure study on the LEH-III-119a:PaMS based OFET with a CYTOP/Al<sub>2</sub>O<sub>3</sub> bi-layer (45 nm CYTOP; 50 nm Al<sub>2</sub>O<sub>3</sub>) and Au bottom contact source/drain electrodes. FIG. 38A shows the transfer characteristics of this OFET initially, after 5 days, before 17 days, and after annealing. FIG. 38B shows the mobility and threshold voltages of this OFET initially, after 5 days, and after 17 days.

FIGS. 39A and 39B show the transfer characteristics and output characteristics of a DRR-IV-209n based OFET with a CYTOP/Al<sub>2</sub>O<sub>3</sub> bi-layer (45 nm CYTOP; 50 nm Al<sub>2</sub>O<sub>3</sub>).
In conclusion, the multilayer approach of the invention opens up the opportunity to develop environmentally and operationally stable OFETs for many applications. Examples of such applications include: drivers for information displays and medical imaging arrays, complementary circuits, adaptive solar cell arrays, radio-frequency identification (RFID) tags, and chemical or physical sensors among many others. In voltage and mobility due to the degradation of driving transistor which is determined by the appended claims. This is because conventional AMOLED displays need a constant current supply is required, bias stress effects have a detrimental impact over the display performance. For such applications the embodiment of the invention will have substantial advantages over for instance, current amorphous silicon (a-Si) FET technologies which are very susceptible to bias stress effects. A particularly attractive application of the invention refers to backplane circuits of active matrix organic light emitting diode (AMOLED) displays for commercial use. This is because conventional AMOLED displays need more transistors to compensate variations of the threshold voltage and mobility due to the degradation of driving transistor to prevent non-uniformity of organic light-emitting diode. This invention will allow high integration density and excellent backplane stability to operate AMOLED displays.

While the principles of the invention have been set out above in connection with specific embodiments, it is to be clearly understood that this description is merely made by way of example and not as a limitation of the scope of protection which is determined by the appended claims.

The invention claimed is:
1. A field-effect transistor having operational stability comprising:
   a gate, a source and a drain;
   a semiconductor layer between the source and the drain; and
   a gate insulator between the gate and the semiconductor layer;
   wherein the gate insulator comprises:
   a first layer adjoining the semiconductor layer at an interface, the first layer comprising a fluoropolymer; and
   a second layer comprising \( \text{Al}_2\text{O}_3 \), the second layer deposited by atomic layer deposition (ALD) to provide increased operational stability compared to other field-effect transistors;
   the first layer having a first dielectric constant and a first thickness; wherein interfacial charge trapping at the interface causes a first effect on a current between the drain and the source over time under a continuous bias stress;
   the second layer having a second dielectric constant and a second thickness, the second dielectric constant being higher than the first dielectric constant; wherein a change in the polarizability of the second layer over time under continuous bias stress causes a second effect on the current between the drain and the source; and
   wherein selection of the first and second thickness and the first and second dielectric constant are such that the first effect compensates at least partly the second effect which provides the increased operational stability, such that variation of the current between the source and the drain under the continuous bias stress for a period of one hour is less than 5 percent.

2. The field-effect transistor of claim 1, wherein the variation in the current between the source and the drain under the continuous bias stress for a period of two hours is less than 5 percent.

3. The field-effect transistor of claim 1, wherein the first layer is formed from an amorphous fluoropolymer having a glass transition temperature above 80 degrees Celsius and the fluoropolymer is selected from the group consisting of: a copolymer of 4,5-difluoro-2,2-bis(trifluoromethyl)-1,3-dioxole (PDD) and tetrafluoroethylene (TFE), or a copolymer of 2,2,4-trifluoro-5-trifluoromethoxy-1,3-dioxole (TTD) and tetrafluoroethylene (TFE).

4. The field-effect transistor of claim 3, wherein the second layer consists of \( \text{Al}_2\text{O}_3 \).

5. The field-effect transistor of claim 1, wherein the thickness of the first layer is less than 200 nm.
6. The field-effect transistor of claim 1, wherein the thickness of the second layer is less than 500 nm.

7. The field-effect transistor of claim 1, wherein the thickness of the first layer is less than 200 nm and the thickness of the second layer is less than 100 nm.

8. A process for manufacturing a field-effect transistor having operational stability, the process comprising:
   providing a source, a drain, a gate, a semiconductor layer between the source and the drain, and a gate insulator between the gate and the semiconductor layer;
   wherein providing the gate insulator comprises:
   depositing a first layer comprising a fluoropolymer, wherein the first layer has a first dielectric constant and a first thickness, the first layer defining an interface with the semiconductor layer; wherein the depositing of the first layer is such that interfacial charge trapping at the interface causes a first effect on a current between the source and drain over time under a continuous bias stress; and
   depositing a second layer comprising Al₂O₃, wherein the second layer is deposited by atomic layer deposition (ALD), the second layer having a second dielectric constant and a second thickness, the second dielectric constant being higher than the first dielectric constant; wherein a change in the polarizability of the second layer over time under continuous bias stress causes a second effect on the current between the drain and the source; and
   wherein selection of the first and second thickness and the first and second dielectric constant are such that the first effect compensates at least partly the second effect to thereby provide increased operational stability compared to other field-effect transistors.

9. The field-effect transistor of claim 1, wherein the first layer is an amorphous fluoropolymer having a glass transition temperature above 80 degrees Celsius selected from the group consisting of: a copolymer of fluorinated 1,3-dioxole and tetrafluoroethylene (TFE), a copolymer of perfluorostyrene (PFS), and tetrafluoroethylene (TFE), a homo- or copolymer of perfluor(1-vinyloxyl)-1-alkenes, and combinations thereof.

10. The field-effect transistor of claim 1, wherein the second layer further comprises an inorganic material selected from the group consisting of Si₃N₄, TiO₂, HfO₂, Ta₂O₅, SiO₂, Y₂O₃, ZrO₂, and combinations thereof.

11. The field-effect transistor of claim 1, wherein the variation of the current between the source and the drain, normalized to the initial current at the end of a direct current (DC) bias test for a period of one hour, is less than 0.03 per hour.

12. The field-effect transistor of claim 1, wherein the thickness of the first layer is less than 50 nm and the thickness of the second layer is about 50 nm or less.

13. The field-effect transistor of claim 1, wherein the thickness of the first layer is less than 100 nm.

14. The process of claim 8, wherein the thickness of the first layer is less than 200 nm.

15. The process of claim 8, wherein the thickness of the second layer is less than 500 nm.

16. The process of claim 15, wherein the thickness of the first layer is less than 200 nm and the thickness of the second layer is less than 100 nm.

17. The process of claim 8, wherein the second layer consists of Al₂O₃.

18. The process of claim 8, wherein the thickness of the first layer is less than 50 nm and the thickness of the second layer is about 50 nm or less.

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