Disclosed is a gain boosting technique for use with millimeter-wave cascode amplifiers. The exemplary technique may be implemented using a 0.18 µm SiGe process (fT=140 GHz). It has also been shown that the technique is effective for CMOS processes with comparable fT. An exemplary gain-enhanced cascode stage was measured to have higher than 9 dB gain with a 1-dB bandwidth above 6 GHz with a DC power consumption of 13 mW. In addition, one cascade stage without gain boosting may be cascaded with two gain-boosted cascade amplifier stages to implement a three-stage LNA. The measured stable gain is higher than 24 dB at 60 GHz with a 3-dB bandwidth of 3.1 GHz for 25 mW of DC power consumption. It is believed that this is the first 60 GHz LNA with a higher than 20 dB gain using a 0.18 µm SiGe process.

20 Claims, 14 Drawing Sheets
OTHER PUBLICATIONS
S. K. Reynolds, “A 60GHz superheterodyne downconversion mixer in silicon-germanium bipolar technology.”
S. E. Gunnarsson, et al., “Highly Integrated 60GHz Transmitter and Receiver MMICs in a GaAs pHEMT Technology”.
* cited by examiner
Fig. 7

Port 2

\[ I_C = 4.2 \text{mA} \]

\[ V_{CE} = 1.8 \text{V} \]

Port 1

\[ V_{CE} = 1.5 \text{V} \]

Fig. 8

Base Inductance \( L \) (pH)

MAG (dB)
Fig. 9a

dB

-40
-30
-20
-10

0

0 20 40 60 80 100 120 140

Base Inductance L (pH)

--- S11 --- S12

Fig. 9b

dB

-4
-2
0
2
4
6
8

0 20 40 60 80 100 120 140

Base Inductance L (pH)

--- S21 --- S22
Fig. 10a

Fig. 10b
Fig. 11a

Simulated S11 - Measured S11
Simulated S22 - Measured S22

Frequency (GHz)

Fig. 11b

Simulated S21 - Measured S21

Frequency (GHz)
Fig. 12a
(Prior art)

Output Matching
RF in

Input Matching
DC bias network

Ibias

Vcc

RF out

Fig. 12b

Output Matching
Microstrip Inductance

Input Matching
DC bias network

Ibias

RF in

Vcc

RF out
Fig. 15

- Basic Cascode
- Gain-enhanced Cascode

Noise Figure (dB)

Frequency (GHz)

Fig. 16

- Measured Output Power (dBm)
- Simulated Output Power (dBm)

- Measured Gain (dB)
- Simulated Gain (dB)

Output Power (dBm)

Gain (dB)

Input Power (dBm)
Fig. 18a

Fig. 18b
Fig. 19

Noise Figure (dB) vs. Frequency (GHz)

Fig. 20

MAG (dB) vs. Base Inductance L (pH)
Disclosed is an exemplary gain boosting technique for millimeter-wave cascode amplifiers. In particular, an exemplary gain boosting technique for a single-stage cascode low noise amplifier (LNA) at 600 Hz is described. The exemplary
technique is implemented using a 0.18 µm SiGe process (fT = 40 GHz). However, the technique is also effective for CMOS processes with comparable fT. An exemplary gain-enhanced cascade stage was measured to have higher than 9 dB gain with a 1-dB bandwidth above 6 GHz with a DC power consumption of 13 mW. Measurement results indicate higher than 4 dB gain improvement compared to a conventional cascade stage with similar die area and DC power consumption. One cascade stage without any gain boosting may be cascaded with two gain-boosted cascade amplifier stages to implement a three-stage LNA. The measured stable gain is higher than 24 dB at 60 GHz with a 3-dB bandwidth of 3.1 GHz for 25 mW of DC power consumption. It is believed that this is the first 60 GHz LNA with a higher than 20 dB gain using a 0.18 µm SiGe process.

This technique is process independent, and can be used in any cascode structure. Theoretical formulations are derived for the given process and verified using simulations. Characterization of transmission lines is also discussed. Transmission line sections constitute the most part of impedance mismatching networks. Conductor-backed coplanar waveguide (CB-CPW) transmission lines are used to reduce radiation loss, and to achieve a better grounding throughout the chip. A good correlation between the measurements and the simulations has been observed. The performance of the LNA stages is discussed with and without gain improvement. A single stage cascode LNA has a measured gain of higher than 5 dB at 60 GHz and a greater than 7 GHz 1-dB bandwidth with a DC power consumption of 16.5 mW. The gain-enhanced cascode stage has been measured to have a higher than 9 dB gain at 60 GHz with a 1-dB bandwidth above 6 GHz with 13 mW of DC power consumption. Hence, the disclosed technique provides a -4 dB gain enhancement at 60 GHz for a single-stage cascode with similar die area and DC power consumption. The measured output PIN is -3.5 dBm. The simulated noise figure is <0.5 dB higher than that of a conventional design.

A three-stage LNA may be implemented by cascading one conventional and two gain-enhanced cascade stages. Measurement results for an exemplary three-stage LNA indicate a stable gain of 24 dB at 60 GHz with a 3.1 GHz 3-dB bandwidth with 26 mW DC power consumption. The measured noise figure is 7.9 dB at 60 GHz. This is the first 60 GHz LNA with a higher than 20 dB gain using a 0.18 µm SiGe BiCMOS process. Thus, implementation of a low noise amplifier in a 0.18 mm SiGe process using gain-boosting circuit techniques is achieved.

Cascade Gain Boosting Technique

Referring to the drawing figures, a cascode structure, stage or device (FIG. 2) was chosen as the basic LNA stage. The simulated maximum available gain (MAG) (See, D. M. Pozar, Microwave Engineering, Wiley and Sons, 1998) of the cascode device at 60 GHz for different emitter lengths of the HBTs is shown in FIG. 1. They correspond to their optimum current densities (corresponding to maximum F, as given by the models), assuming identical transistors in the common-emitter (CE) and common-base (CB) stages and a 3.3 V power supply (1.5 V across the CE stage and 1.8 V across the CB stage).

As is shown in FIG. 1, the MAG of a single cascode stage is approximately 9-10.5 dB at 60 GHz with the variation of the emitter length. Also, 50 ohm matching for maximum power gain increases the noise figure from its minimum (NFmin) value if the optimum noise matching conditions do not match with power matching conditions. To minimize this effect, medium sized HBTs (emitter length 6 µm) were chosen.

4 Mismatches in the matching networks, as well as transmission line losses reduce the actual available gain from a cascode stage. Thus, different available gain boosting techniques were evaluated. Gain boosting of a common gate (CG) LNA has been reported at a much lower RF frequency. See D. J. Allstot, et al., "Design Considerations for CMOS Low-Noise Amplifiers," Radio Frequency Integrated Circuits Symposium, pp. 97-100 June 2004, Fort Worth, Tex. However, this technique requires a number of additional circuit components, and even then is not suitable for the cascode structure preferred in 60 GHz LNAs. There is also a report of cascode gain boosting at lower RF frequencies, where a negative resistance generating circuit (MOS with gate inductance) is connected to the drain of the common-source (CS) MOS. See S. Asgarian, et al., "A Novel Gain Boosting Technique for Design of Low Power Narrow-Band RF CMOS LNAs," IEEE Northeast Workshop on Circuits and Systems, pp. 293-296 June 2004, Montreal, Canada. However, that requires a separate transistor with additional biasing, and the bandwidth is narrow (due to the tuned nature of the negative resistance generating circuit) with inherent instability with higher oscillation possibility (due to the parasitic effects at 60 GHz).

Disclosed herein is a gain boosting technique that needs just one additional inductive feedback element to facilitate layout and design complexity issues. This technique is process (SiGe/CMOS) independent, and can be used for any cascode stage as described herein. A simple small-signal HBT model was considered for theoretical formulations. See M. Rudolph, et al., "Direct Extraction of HBT Equivalently Circuit Elements," IEEE Trans. Microwave Theory & Tech., Vol. 47, No. 1, pp. 82-84, January 1999, and P. Sen, et al., "A Broadband, Small-Signal SiGe HBT Model for Millimeter-Wave Applications," European GaAs and other Compound Semiconductors Application Symposium, pp. 419-422, October 2004, Amsterdam, The Netherlands. FIG. 2 shows a Gunn-pool based model of an exemplary cascode stage with corresponding parameters.

Common Base Stage with Base Inductance

A single common base (CB) stage with a shorted inductance (L) in the base is shown in FIG. 3. The input impedance (IN) can be determined in terms of the two-port z-parameters and characteristic impedance (Zo) as follows:

\[ Z_{IN} = Z_0 \frac{Z_{12} \times Z_{21}}{Z_0 + Z_{22}} \]  

(1)

The values of the z-parameters are defined as

\[ Z_{ij} = Z_0 + jωL \] \[ Z_{0b} = Z_0 + jωL \]

where, \[ Z_0 \] defines the corresponding z-parameters in the absence of the inductance L and to is the frequency in radian. Hence, \[ Z_{IN} \] determined as

\[ Z_{IN} = Z_{0b} + jωL \]

(3)

where,

\[ A = \frac{1}{\left( Z_0 + R_0 \right) + jω \times \left( C_{Ge} + C_{Gs} \right)} \]

(4)

\[ \frac{1}{\left( Z_0 + R_0 \right) + jω \times \left( C_{Ge} + C_{Gs} \right)} = \frac{C_{Ge} + R_0}{C_{Ge} + C_{Gs}} \]
The model parameters are extracted from device (emitter length=6 μm) simulations and the corresponding real and imaginary parts of \( Z_{re} \) are plotted for different values of base inductance (L). FIGS. 4a and 4b show these plots along with the corresponding simulated values of \( Z_{pe} \).

As is shown in FIGS. 4a and 4b, the real part of the input impedance of the CB stage decreases, and the imaginary part of the input impedance of the CB stage increases with increasing base inductance (L) in an approximately linear fashion. This impedance acts as the load for the CE transistor in the cascode stage. To evaluate the effect of the base inductance (L), the voltage gain of the CE transistor with this varying load impedance is analyzed below.

Voltage Gain of the Common Emitter Stage

The voltage gain of the common emitter (CE) stage can be defined in terms of its \( z \)-parameters and the load impedance \( Z_L \) as follows:

\[
A_V = \frac{Z_L \times Z_L}{\Delta Z + Z_L + Z_L}
\]

where,

\[
\Delta Z = Z_L \times Z_{re} - Z_L \times Z_{im}
\]

The input impedance of the CB stage acts as the load impedance of the CE stage. FIG. 5 plots the voltage gain of the CE stage for different real and imaginary values of the \( Z_L \) over the entire range of input impedance of CB stage as shown in FIGS. 4a and 4b (VCE=1.8V, ic=4.2 mA). FIG. 6 shows the voltage gain at the specified impedances corresponding to the base inductance values of the CB stage. Simulated voltage gain is also plotted to compare with the theoretical values, and they match reasonably well.

FIGS. 5 and 6 illustrate that the voltage gain of the CE stage increases rapidly with the decrease in the real part of the load impedance, which, in turn, is caused by the base inductance in the CB stage. The power gain of the cascode increases due to the increase in the voltage gain of the CE stage. However, the voltage gain of the CB stage reduces (by a smaller extent), thus limiting the gain-enhancement using this technique as the base inductance values of the CB stage.

The input impedance of the CB stage increases with increasing load impedance, which, in turn, is caused by the base inductance in the CB stage. However, the voltage gain of the CB stage reduces (by a smaller extent), thus limiting the gain-enhancement using this technique as the base inductance values of the CB stage.

Gain Enhancement

FIG. 7 shows a schematic of a cascode core with the base inductance in the CB stage. The emitter length is 6 μm, and the DC conditions (derived from conditions of higher gain and lower DC power consumption) are shown in FIG. 7. The variation of MAG and the different s-parameters at 60 GHz are plotted with the variation of base inductance in FIGS. 8 and 9a and b, respectively.

FIG. 8 shows a significant improvement of MAG of the cascode core with increasing inductance at the base of the CB transistor. This is due to the increase in voltage gain of the CE transistor. However, at higher values of L, the MAG decreases by a small amount due to the reduction in gain of the CB stage. Hence, 90 pF was chosen as the optimum base feedback inductance to enhance the gain of this particular cascode core. This enhances the simulated MAG by approximately 5 dB for the same power consumption.

FIGS. 9a and 9b show an increasing trend in all the s-parameters with increasing L. This signifies a reduction in the overall stability factor (K) of the cascode stage, resulting in higher instability. Hence, the current consumption of the gain-enhanced cascode stage is reduced to increase the inherent stability factor.

Transmission Line and Matching Network Characterization

The input and the output matching networks of the single cascode stages, as well as the interstage matching networks of a multi-stage LNA are realized with conductor-backed coplanar waveguide (CB-CPW) transmission lines in order to minimize the radiation losses, when compared to a microstrip configuration. The base inductance in the cascode device is used to minimize the length of the transmission line. The transmission lines are characterized to match the measurements with the corresponding simulations. FIGS. 10a and 10b show simulated and the measured s-parameters of a 60 GHz 50 ohm L/4 CB-CPW transmission line and the measured capacitance of a 201.6 μf capacitor, used in the matching circuits as DC block components.

Test structures for input and output matching networks of single-stage LNAs with and without gain enhancement were measured. The matching characteristics correspond relatively well with the simulations. However, the insertion loss is higher by a significant amount as the resistive losses are not entirely captured by the simulation models (as evident from FIGS. 10a and 10b). FIGS. 11a and 11b show measured and simulated s-parameters of the input-matching network of the LNA cascode stage without gain boosting (including the effect of bond pads). The difference between measured and simulated \( S_{11} \) is primarily caused by the resistive and substrate losses in the transmission lines.

LNA Implementation

The exemplary gain boosting technique discussed above was implemented in an exemplary single-stage cascode LNA. A microstrip transmission line is used to realize the feedback inductance at the base of the CB transistor in the cascode configuration. FIG. 12a shows a schematic of a conventional single-stage LNA and FIG. 12b shows the schematic of an exemplary gain-enhanced single-stage LNA. The shorted stubs in the input and the output matching networks are used to provide base bias and supply voltage bias, respectively. Similar matching networks were implemented as discussed above. The device size is selected to minimize the noise figure for a 50 ohm input match, as well as to minimize the DC power dissipation for a given gain. The selected emitter length is 6 μm. An exemplary single-stage cascode LNA occupies an area of 0.86 mm x 0.83 mm, and the gain-enhanced LNA occupies 1.05 mm x 0.71 mm.

FIGS. 13a and 13b are graphs showing measured and simulated s-parameters of the single-stage cascode LNA (5 mA from 3.3V supply) without gain enhancement. The cascode stage without gain-boosting was measured to have a higher than 5 dB gain at 60 GHz band with a 1-dB bandwidth above 7 GHz as shown in FIGS. 13a and 13b with a DC power consumption of 16.5 mW (5 mA from 3.3V supply). The input and output matching correspond well with the simulation. Lossy transmission lines in the matching networks (discussed above) cause a ~2 dB difference between the measured and the simulated gains \( S_{11} \). The gain-enhanced cascode LNA was measured to have a higher than 9 dB stable gain (K factor>1.4 over the frequency range) with a 1 dB bandwidth greater than 6 GHz as shown in FIGS. 14a and 14b.
for a DC power consumption of 13 mW (3.5 mA from a 3.7V supply). Hence, the gain enhancement technique results in greater than 4 dB gain improvement at 60 GHz for a similar area and DC power consumption. The shift in the output matching is primarily caused by the parasitic inductance (~25-30 pH) in the feedback path and also higher than predicted inductive effects.

The simulated noise figure of the gain-enhanced cascode stage is slightly higher (~0.5 dB) than that of the basic cascode stage. FIG. 15 compares the simulated noise figures of the two different configurations.

The linearity measurements show similar input 1 dB compression point for two different configurations. The measured output P1dB is approximately ~3.5 dBm. FIG. 16 shows the measured and simulated linearity of the gain-enhanced cascode stage at 60 GHz. They correspond well with each other.

One basic cascode stage and two gain-enhanced cascode stages may be cascaded to implement a three-stage LNA that can be used in the 60 GHz front-end. The gain boosting technique is not applied to the first stage in order to minimize the noise figure of the integrated LNA. FIG. 17 shows a schematic of the 3-stage LNA. An exemplary die occupies an area of 2.05 mm x 0.71 mm.

The measurement results show a higher than 24 dB stable gain (K factor ~4 at the frequency band) at 60 GHz with a 3.1 GHz 3-dB bandwidth with 25 mW of DC power consumption. The measured noise figure is 7.9 dB at 60 GHz. The simulated output P1dB is ~3.5 dBm and that corresponds to the measured output P1dB of the gain-enhanced LNA. This is the first 60 GHz LNA with a higher than 20 dB gain using a 0.18 µm SiGe BiCMOS process. The measured and simulated s-parameters are shown in FIG. 18a and 18b. The measured noise figure is shown in FIG. 19.

Table 1 compares the performance of the exemplary LNA shown in FIG. 17 with reported silicon-based 60 GHz LNAs.

<table>
<thead>
<tr>
<th>Process</th>
<th>Topology</th>
<th>Frequency (GHz)</th>
<th>Gain (dB)</th>
<th>Noise Figure</th>
<th>Power consumption (mW)</th>
<th>Output P1dB (dBm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.12 µm SiGe HBT</td>
<td>1-stage cascaded</td>
<td>56-64</td>
<td>15</td>
<td>4.5</td>
<td>11</td>
<td>~5@61 GHz</td>
</tr>
<tr>
<td>0.13 µm CMOS</td>
<td>3-stage cascaded</td>
<td>51-57</td>
<td>&gt;20</td>
<td>8</td>
<td>72</td>
<td>1.8@56 GHz</td>
</tr>
<tr>
<td>0.13 µm CMOS</td>
<td>3-stage cascaded</td>
<td>51-65</td>
<td>12</td>
<td>8.8</td>
<td>54</td>
<td>2@60 GHz</td>
</tr>
<tr>
<td>0.18 µm SiGe HBT</td>
<td>3-stage cascaded (with feedback inductor)</td>
<td>58-63</td>
<td>&gt;20</td>
<td>7.9</td>
<td>25</td>
<td>~3.5@60 GHz</td>
</tr>
</tbody>
</table>

TABLE 1

Silicon-based 60 GHz LNA performance comparison.

The gain boosting technique may also be applied to a CMOS cascode core using a 0.13 µm CMOS process, for example. FIG. 20 shows the simulated enhancement of MAG with different lengths of the inductor at the gate of an exemplary cascode device. It shows a comparable enhancement as shown in FIG. 8 for SiGe HBT device.

Thus, a gain boosting technique for use with millimeter-wave cascode amplifiers has been disclosed. It is to be understood that the above-described embodiments are merely illustrative of some of the many specific embodiments that represent applications of the principles discussed above.

Clearly, numerous and other arrangements can be readily devised by those skilled in the art without departing from the scope of the invention.

What is claimed is:
1. Cascode core apparatus comprising:
a common emitter transistor;
a common base transistor cascaded with the common emitter transistor; and
an inductance having a first end coupled to a base of the common base transistor and having a second end coupled to a capacitively coupled RF ground, which inductance increases the maximum available gain of the apparatus in a predetermined bandpass frequency range, and wherein the inductance sets the predetermined bandpass frequency range.
2. The apparatus recited in claim 1 which further comprises:
an output matching network having an RF output coupled between a voltage source and the common base transistor;
an input matching network having an RF input that is coupled to a base of the common emitter transistor; and a DC bias network coupled to the input matching network.
3. The apparatus recited in claim 1 wherein the inductance comprises a microstrip inductance.
4. The apparatus recited in claim 3 wherein the inductance comprises a lumped inductance.
5. The apparatus recited in claim 3 wherein the inductance comprises a coplanar waveguide inductance.
6. The apparatus recited in claim 2 wherein the inductance comprises a microstrip inductance.
7. The apparatus recited in claim 1 further comprising:
an output matching network having an RF output coupled to a collector of the common base transistor;
an input matching network having an RF input that is coupled to a base of the common emitter transistor, and a DC bias network for providing bias for the common base and common emitter transistors; which apparatus comprises a one-stage gain-boosted cascode amplifier stage.
8. The apparatus recited in claim 7 which is configured to operate at a frequency range between 57 and 64 GHz.
9. The apparatus recited in claim 7 further comprising:
an unboosted one-stage cascode amplifier stage coupled to an input of the gain-boosted cascode amplifier stage; and
a second one-stage gain-boosted cascode amplifier stage coupled to an output of the one-stage gain-boosted cascode amplifier stage.
10. The apparatus recited in claim 9 which is configured to operate at a frequency range between 57 and 64 GHz.
11. A method for providing gain boosting in a cascode amplifier, comprising
fabricating a cascode amplifier comprising a common emitter transistor, a common base transistor cascaded with the common emitter transistor, an output matching network having an RF output coupled to a collector of the common base transistor, an input matching network having an RF input that is coupled to a base of the common emitter transistor, and a DC bias network for providing bias for the common base and common emitter transistors; and
coupling a first end of an inductance to a base of the common base transistor and coupling a second end of the inductance to a capacitively coupled RF ground, so as to increase the gain of the cascode amplifier in a
predetermined bandpass frequency range, and wherein
the inductance sets the predetermined bandpass frequen-
cy.
12. The method recited in claim 11 wherein the gain boost-
ing of the cascode amplifier is achieved without increasing
the area of the amplifier and without increasing the DC power
consumption.
13. The method recited in claim wherein fabricating the
cascode amplifier is achieved using a SiGe process.
14. The method recited in claim 11 wherein fabricating the
cascode amplifier is achieved using a 0.18 \( \mu \)m SiGe process.
15. The method recited in claim 11 wherein fabricating the
cascode amplifier is achieved using a CMOS process.
16. The method recited in claim 10 wherein fabricating the
cascode amplifier is achieved using a 0.13 \( \mu \)m CMOS pro-
cess.
17. The method recited in claim 11 wherein the cascode
amplifier comprises a one-stage gain-boosted cascode ampli-
fier stage, and wherein the method further comprises:
fabricating a second cascode amplifier comprising a com-
mon emitter transistor, a common base transistor cas-
caded with the common emitter transistor, an output
matching network having an RF output coupled to a
collector of the common base transistor, an input match-
ing network having an RF input that is coupled to a base
of the common emitter transistor, and a DC bias network
for providing bias for the common base and common
emitter transistors, which second cascode amplifier
comprises an unboosted one-stage cascode amplifier
stage;
coupling the unboosted one-stage cascode amplifier stage
to an input of the gain-boosted cascode amplifier stage;
fabricating a third cascode amplifier comprising a common
emitter transistor, a common base transistor cascaded with the common emitter transistor, an output matching
network having an RF output coupled to a collector of the
common base transistor, an input matching network having an RF input that is coupled to a base of the
common emitter transistor, and a DC bias network for
providing bias for the common base and common emit-
ter transistors;
coupling an inductance between a base of the common
base transistor and a capacitively coupled HF ground of
the third cascode amplifier so as to form a second gain
boosted cascode amplifier, and
coupling the second gain boosted cascode amplifier to an
output of the gain-boosted cascode amplifier.
18. The method recited in claim 17 wherein fabricating is
achieved using a SiGe process.
19. The method recited in claim 17 wherein fabricating is
achieved using a CMOS process.
20. The method recited in claim 17 wherein fabrication
produces an amplifier structure that operates at a frequency
range between 57 and 64 GHz.