ELECTRICAL MODELING, DESIGN, AND HIGH-FREQUENCY CHARACTERISATION OF FINE-PITCH THROUGH-PACKAGE-VIAS IN ULTRA-THIN 3D GLASS INTERPOSER PACKAGES

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To my beloved sister
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SUMMARY

System scaling by 3D packaging is now considered a critical technology enabler for continued increases in system data bandwidth, at lowest power and cost. Ultra-high chip-to-chip interconnect bandwidth is required for variety of new applications including 5G communications, V2V (vehicle-to-vehicle) and V2N (vehicle-to-network) connectivity, gaming, server and data center traffic. The best approach to increase bandwidth between multiple ICs is to interconnect them at the shortest path length possible. Although direct chip stacking with through silicon vias (TSV) was developed as the primary approach for 3D integration, thermal and cost problems have limited their applicability [1]. Georgia Tech previously proposed and demonstrated 3D interposers as a superior alternative to achieve 3D-IC like interconnect lengths at much lower cost and without the thermal problems [2]. Glass is the best material for 3D interposer packages due to its superior dimensional stability and flatness compared to organic laminates, and large panel scalability and lower loss compared to silicon. The single biggest barrier to 3D glass interposers is the formation of through package vias (TPVs) in ultra-thin glass substrates at the same pitch and height as TSVs. Although initial research into formation methods and metallization processes for ultra-thin glass TPVs was reported by Georgia Tech researchers, this dissertation represents the first complete study on the electrical modeling of TPVs at 50 µm pitch in 50 µm ultra-thin glass up to 30 GHz. Two major applications are expected to have major impact from this research, namely, (a) logic-memory high density interconnections for digital bandwidth, and (b) mm-wave IC to antenna low loss interconnections for small form factor 5G modules.

The objectives of this research are to perform detailed and accurate high frequency electrical modeling of small-TPVs at ultra-fine pitch ( < 30 µm diameters at 50 µm pitch) in ultra-thin glass (50 µm) substrates, develop handling methods to fabricate metallized TPVs and validate
the electrical models through high frequency characterization. The key technical challenges in meeting these objectives are i) High – frequency effects in the accurate evaluation of low-loss parasitics in ultra-short TPVs ii) Impedance mismatch between the transmission lines (TLs) and the TPVs iii) Ease of ultra-thin (50 µm) glass handling iv) Precise model-measurement correlation. To overcome these challenges, this study focuses on the following tasks: i) Wave-dimensional analysis of signal TPVs, TL and TPV transition structures, ii) Impedance mismatch reduction by developing tighter design rules for small-diameter TPVs iii) Ultra-thin glass-handling technique and reliable copper metallization of high-aspect ratio TPVs, and iv) Use of Through-Reflect-Load (TRL) calibration technique, for precise model-measurement correlation.

This study represents the first demonstration of ultra-low loss through package interconnects with <0.03 dB/mm insertion loss, on a two-metal layer ultra-thin (50 µm) glass substrate with TPVs. Accurate electrical modeling was performed with 3D full wave Electro-Magnetic (EM) solvers, and a unique structure was proposed to extract the parasitics of the TPVs, based on transmission line theory. This technique is less computationally intensive and incorporates more efficient de-embedding methodologies than previous approaches. It is also scalable to frequencies beyond 50 GHz, for radar and THz communication structures.

Low-loss polymer lamination on thin glass substrates was developed by GT-PRC, as a means for defect-free handling of thin-glass [2]. The polymer films also provide stress-buffering between the copper interconnections and the glass. This research extends this handling technique to 50 µm thick glass, through additional edge-protection accomplished by creating edge-beading with polymer-laminated frames. A brief warpage analysis of the resulting stack-up is presented, along with the guidelines to scale it to larger panel fabrication.
Semi-additive patterning was utilized to metallize TPVs, starting with electro-less Cu seed-layer deposition on polymer-laminated glass, followed by electrolytic plating of Cu. Significant improvement in electrical performance, due to the reduction in the interconnection length in ultra-thin glass substrates compared to thicker glass substrates, was validated through 3D EM simulations and Vector Network Analyzer (VNA) measurement of demonstration test vehicles.

The key contributions and the novelty of this research are:

i) First comprehensive study of the electrical performance of high-aspect ratio TPVs at 50 µm pitch, in ultra-thin glass (50 µm) substrates.

ii) New technique for the accurate high frequency electrical characterization of TPV parasitics including its resistance, inductance and capacitance, and measurement correlation up to 30 GHz.

iii) Demonstration of the electrical benefits of ultra-fine TPVs at fine pitch, using 3D full wave electromagnetic (EM) modeling, for high-speed digital and mm wave systems.

iv) Demonstration of an improved ultra-thin glass handling technique, by means of edge beading with polymer-laminated frames.
CHAPTER 1
INTRODUCTION

Evolving cellular network generations and cloud computing systems drive the demand for highest data bandwidth at lowest power consumption and smaller form factors. Although transistor scaling, driven by Moore’s law, has enabled higher functionality and miniaturization at the device level for the past several decades, there are increasing technical, yield and cost challenges with heterogeneous integration on a single chip. Two major factors have fueled the rise of multi-die packaging architectures as a primary approach to system bandwidth scaling, (a) the escalating design and yield driven manufacturing cost of implementing large SoCs, and (b) the continuing increase in functional diversity in electronic systems requiring multiple types of wafers. To illustrate this growth, the industry road map for wireless cellular networks and the corresponding evolution of systems packaging concepts are shown in Figure 1. Traditional 3D packages such as flip-chip package on package (PoP) have been limited to bandwidths of approximately 25 GB/s, mainly due to the coarse pitch and long die-to-die interconnections (~3-5 mm and longer), significantly lower than the escalating bandwidth needs (~55 GB/s) of emerging smart systems. 3D IC stacking was developed as a compelling alternative solution to single chip scaling, by providing a 3rd dimension for connecting ICs with fine pitch and ultra-short interconnections.

1.1 3D Interposers vs. 3D ICs and 2.5D Interposers:

3D ICs provide very high bandwidth due to ultra-short vertical connections, at extremely fine- pitch and thinned die-to-die bonding. However, much of the potential of 3D IC stacking was not realized, due to thermal and cost barriers. Hence, the industry began to develop 2.5D interposers with side-by-side chips assembled at fine pitch on BEOL silicon substrates. 2.5D silicon interposers were introduced by Xilinx for packaging their FPGA modules [3, 5]. It involves
side by side integration of ICs with multi-layer RDL copper traces with tight tolerances, for high density interconnections.

![Diagram showing package architecture and technology roadmap]

**Figure 1: Semiconductor industry’s roadmap and the motivation for 3D integration technologies**

There is still a growing gap between memory bandwidth and overall system requirements, clearly creating an I/O bottleneck and the so called “memory wall”, as depicted in Figure 1. Silicon interposers with back end of the line (BEOL) wafer processes can achieve the required wiring and I/O density, as shown in Figure 2a. Yet, they lack optimum electrical performance due to the semiconducting nature of Si, as shown in Figure 2b. The interconnect lengths in 2.5D interposer architecture are also significantly longer than 3D IC interconnections, leading to bandwidth limits. Georgia Tech PRC pioneered the concept of panel scalable 3D glass interposers with small diameter through package interconnections, combining the ultra-short interconnect lengths of 3D ICs, but without the associated thermal and cost challenges. A conceptual schematic of a glass based 3D interposer for mixed signal applications, such as mobile terminals, is shown in Figure 3.
This is implemented through the double side IC assembly on glass substrates, interconnected by ultra–short and ultra-fine through via connections. This architecture can efficiently meet the performance requirements of the emerging smart systems. Moreover, this technology eliminates the need for TSVs to stack chips in double sided, allowing designers to put dies next to each other as well on both sides of the interposer, in a high performance and low loss configuration. This system scaling concept promises the integration of disparate technologies in a small foot print, at lowest power and highest performance.

Figure 2: 2.5D silicon interposer introduced by Xilinx a) Concept View b) Eye diagram of digital interconnections [3], [4]

Figure 3: Perspective view of a 3D glass based interposer with ultra-fine TPVs, for heterogeneous integration in smart electronics
1.2 Glass as a 3D High-Density Interposer Material:

Glass has exceptional integration potential as an interposer, compared to other materials, because of its dimensional stability under thermal load and CTE match to silicon ICs and PCB. Basically, glass exhibits the combined performance benefits of silicon and organic interposers through the potentiality for fine pitched RDLs, small diameter through – vias and the high alignment accuracy. The following properties makes glass, a distinguishing candidate for electronics integration:

i) Large availability of the thin glass substrates in panel form, engineered to a value between 30 – 100 µm, as shown in Figure 4.

ii) Superior electrical performance due to

   a. High electrical resistivity (10^{12} – 10^{16} Ω.cm)
   b. Low dielectric constant (5 – 7)
   c. Low loss tangent (0.006 @ 10 GHz)

iii) Affordability for ultra-fine line lithography to form high-density interconnects due to

   a. High modulus (50 – 90)
   b. Excellent surface finish with < 1 nm roughness

iv) Low thermo - mechanical stress at die – interposer and interposer – board interconnection due to

   a. Tailorable CTE
   b. High rigidity leading to high dimensional stability
Figure 4: Thin glass technologies from leading glass manufacturers, reported in [6], [7] and [8] respectively

Also, ultra-thin glass offers potential advantages in the manufacturing of ultra-small TPVs at fine-pitch, to achieve the shortest interconnection length between the connected components. This property of thin-glass enables the high I/O density integration for digital interposers, by matching the TPV dimension to the high-density bump pitch at the die level, which is required for optimum routability. Figure 5 illustrates the integration benefits of thin-glass. The low profile of a 3D ultra-thin glass package with TPVs, makes it a new paradigm for interposer technology competing against coreless packaging.

Figure 5: Ultra-thin glass with fine-pitch TPVs, as an enabler of high density integrated packages
1.3 Through-Package-Vias (TPVs) in Glass Interposers:

The term through-package-vias (TPVs), was coined by the GT-PRC, to represent high performance vertical through interconnections in glass packages and interposers, as shown in Figure 6. TPVs are an integral part of the 3D interposer technology, enabling the low loss signal transition between the metal layers on the core substrate.

![Figure 6: TPVs as key enablers of 3D Glass interposer technology](Picture Courtesy: Dr. Venky Sundaram, GT-PRC)

The key aspect that distinguishes glass vias from its silicon or organic counterparts, is the accurate layer to-layer registration with smaller capture pads. This is a major enabler for building high density integrated packages. The TPV surface geometry, its taper angle and side wall roughness are some of the post – drilling metrics that notably dictate the quality of the signal transition through them. Different approaches are being pursued for drilling high aspect ratio glass vias with smooth side wall as shown in Figure 7, simultaneously improving the throughput to about 1,00,000 vias/second.
Figure 7: Optical image of TPV drilled by different methods reported in [9], [10],[11] respectively

1.4 Continuous Scaling in Glass Substrate Thickness and the Through-Via Dimensions:

A steady scaling in the interposer thickness and the through interconnect dimensions is a strategic need, to keep up with the miniaturization and the performance demand in the emerging smart electronic systems. Similar trends are applicable to 3D glass interposers as shown in Figure 8. Combined with Cu-polymer re-distribution layers (RDL), ultra-thin glass provides an excellent platform for 3D active and passive component integration. Multi-layer RDL at 20-40µm bump pitch has been demonstrated, leveraging the ultra-smooth surface and exceptional dimensional stability during RDL processing. Ultra-thin glass is also flexible for conformal electronics applications such as wearables, and is hermetic for packaging of sensors and other moisture-sensitive devices. Recently, Vijay Sukumaran in his PhD Thesis, has demonstrated the 30-50 µm glass based 3D interposers with fine-pitch TPVs, for high-speed digital applications [12], as shown in Figure 9. However, a detailed high frequency electrical modeling and characterization of the through interconnects, considering the signal and power integrity aspects, has not been well-documented. This research goes beyond prior research to establish the electrical superiority of ultra-thin glass substrates (50 µm) with fine-pitch TPVs and performs a detailed microwave analysis of the signal transitions through the vias.
Figure 8: Scaling trend in the substrate thickness and via dimensions in 3D glass interposer technology

Figure 9: a) Snapshot of 30 µm glass core based 2ML test vehicle b) SEM Image of cross-section showing TPV transitions [12]

1.4.1 Compelling benefits of ultra–thin glass substrates with fine pitch TPVs:

a) **Thinner form factor:** Thin glass substrates can be produced in large sheets or rolls of 30-50µm thicknesses by down draw processes without the need to grind and polish, as shown in Figure 4. Ultra-thin glass with fine-pitch TPVs offer potential opportunities for building ultra-miniaturized and cross – functional modules with high electrical performance and thermo-mechanical reliability.

b) **Reduced defect propagation:** Failures mode propagation in glass substrates are a function of defect density within the material. Prior studies on the Weibull distribution
plot [13] showed greater strength values for thinner glass substrates, in the range of 300-500 MPa, an order of magnitude greater than thicker glass substrates.

c) **Improved electrical performance:** Thinner substrates have ultra – short through package interconnections, for 3D interposer applications. This in turn offer outstanding benefits for both the signal and power integrity of the packages.

   a. **Signal Integrity:** Lower insertion and return loss due to short interconnection length for planar and vertical through interconnects.

   b. **Power Integrity:** Higher plane capacitance and lower inductance path length.

d) **Better EMI Isolation:** The fine pitch TPVs have the following advantages in isolating noise interferences, as also depicted in Figure 10.

e) **Better termination of E-Fields:** At fine – pitch, there is more room for ground TPVs that can enhance the proper termination of E-fields between the vertical through interconnections.

f) **Smaller Aperture:** Small diameter TPVs with small aperture size in the reference plane, enhance the power integrity of the package by greatly reducing the ground bounce effects, as shown in Figure 10. Ground bounce usually occurs in high density system integration, where the signal I/O is not provided low resistance (or high capacitance) path to the ground plane.
1.5 Research Objectives, Challenges and Tasks:

The main objectives of this research are two-fold:

i) Detailed and accurate high-frequency electrical modeling of the small-diameter (20-60 µm) TPVs, in 50 µm thin glass based 3D interposer.

ii) Provide tighter via design guidelines, to achieve < 0.07 dB/mm interconnect loss, in a 2ML 50 µm thin glass based 3D interposer, for mixed-signal systems.

Accordingly, the primary focus of this research is on the detailed microwave analysis of the small diameter TPVs (20–60 µm) at fine-pitch (50 – 150 µm) in ultra-thin (50 µm) glass substrates, considering signal and power integrity aspects. The design focus along with the metrics and specifications are shown in Table 1.

Table 1: Design targets for ultra-small TPVs at fine pitch in ultra-thin glass interposers

<table>
<thead>
<tr>
<th>Focus</th>
<th>Design Metric</th>
<th>Target specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ultra – low loss vertical through interconnects in 3D glass interposer</td>
<td>Insertion loss</td>
<td>Planar interconnect: &lt; 0.04 dB/mm @ 28 GHz&lt;br&gt;Vertical interconnect: &lt; 0.03 dB/mm @28 GHz</td>
</tr>
<tr>
<td>VSWR</td>
<td>&lt;1.5 @ 28 GHz</td>
<td></td>
</tr>
<tr>
<td>Delay</td>
<td>&lt;5 ps @ 28 GHz</td>
<td></td>
</tr>
</tbody>
</table>
Given these objectives, the challenges that are identified in the design and demonstration of the proposed technology are summarized in Table 2, along with the research tasks to overcome the challenges. They are also labelled in Figure 11.

![Figure 11: Challenges in the design and demonstration of ultra-thin glass with TPVs](image)

**Table 2: Challenges and the research tasks in the design and demonstration of ultra-thin glass with TPVs**

<table>
<thead>
<tr>
<th>Label</th>
<th>Challenges</th>
<th>Tasks</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td><strong>High-Frequency Electrical Modeling</strong></td>
<td>• Study the impact of via diameter and pitch on impedance variation</td>
</tr>
<tr>
<td></td>
<td>• Impedance Discontinuity</td>
<td>• Maximum signal return path</td>
</tr>
<tr>
<td></td>
<td>• Resonance effects in PDN in mixed signal systems</td>
<td></td>
</tr>
<tr>
<td>B</td>
<td><strong>Panel Process Development</strong></td>
<td>• Edge protection techniques</td>
</tr>
<tr>
<td></td>
<td>1. Handling ability of thin glass</td>
<td>• Investigate different adhesion promotions</td>
</tr>
<tr>
<td></td>
<td>2. Reliable metallization of high aspect ratio TPVs</td>
<td></td>
</tr>
<tr>
<td>C</td>
<td><strong>Electrical Characterization</strong></td>
<td>• Accurate frequency discretization in wide band</td>
</tr>
<tr>
<td></td>
<td>• Estimation of low loss of TPVs with ≤5% measurement error</td>
<td>• TRL calibration</td>
</tr>
<tr>
<td></td>
<td>• Model to hardware correlation</td>
<td></td>
</tr>
</tbody>
</table>
1.6 Thesis Organization:

This dissertation is organized into six chapters:

   In chapter 1, the driver for 3D glass interposer technology and the strategic need for fine-pitch TPVs in ultra-thin glass substrates, was discussed. The next five chapters are organized as follows:

   **CHAPTER 2**: In Chapter 2 the relevant prior research on electrical modeling, TPV metallization and high frequency RF characterization in glass substrates is presented.

   **CHAPTER 3**: In Chapter 3, the detailed electrical modeling techniques for ultra-small TPVs in thin glass is discussed. Based on the 3D EM modeling results, design guidelines are outlined for building digital and analog RF systems in thin-glass substrates.

   **CHAPTER 4**: This chapter is divided into two sections. In the first section, a unique edge protection technique is investigated for better handling of thin – glass substrates. In the second section, the details of the customized test vehicle design that consists of high-aspect ratio TPVs are discussed.

   **CHAPTER 5**: This chapter describes the signal and power integrity analysis of the ultra-small, fine-pitch TPVs through S-parameter measurements.

   **CHAPTER 6**: The concluding chapter summarizes the key contributions, milestones and the scope for further extension of the research presented in this dissertation.
CHAPTER 2
LITERATURE SURVERY

Chapter 1 introduced the focus of this research on detailed electrical modeling, demonstration, high frequency electrical and thermal reliability characterization of small diameter (20 – 60 µm) Through Package Vias (TPVs) at fine-pitch (50 – 150 µm) in thin glass substrates (50, 100 µm). It also established the electrical significance of ultra-thin glass substrates with fine-pitch TPVs, for mixed signal integrated systems. The three major challenges identified were: a) Lack of wave-dimensional analysis technique for detailed and accurate modeling of ultra-low loss through interconnects in thin glass b) Handling-ability of thin-glass substrates and c) Reliable metallization technique for high aspect-ratio TPVs. This chapter will provide a comprehensive review of published literatures addressing these three challenges. The concluding section in this chapter will present a summary of published work on glass interposers with emphasis on the high frequency electrical characterization of glass vias.

2.1 Prior Art on Electrical Modeling of Through-Glass-Vias (TGVs):

Glass as an interposer technology has attracted much attention in the recent past, due to its favorable properties including high resistivity, CTE tailoring ability, dimensional stability and panel processing capability. Particularly, the high electrical resistivity of glass enables efficient transmission of signals with minimal insertion loss and cross-talk. Although the signal propagation in Through Silicon Vias (TSVs) has been studied in detail, through analytical methods and simulations, the behavior of through vias in glass has been studied to a lesser extent. This research is the first comprehensive analysis of the high frequency electrical behavior of small-diameter TPVs in thin glass (50 µm) substrates. This section provides an overview of the circuit and full
wave techniques, proposed in the literature, that were used to model the electrical behavior of TGVs in digital and analog integrated systems.

2.1.1 Modeling through 3D full wave EM solver:

The Microstrip Line (MSL) and the Coplanar WaveGuide (CPWG) based 3D modeling technique reported in [15] estimated the electrical behavior of TGVs using finite element principles. The model and the results are shown in Figure 12. The thickness of the substrate was greater than 100 µm and tungsten was used as the via filling material. The effects of variations in the TGV diameter, via length and inter-layer and intra-layer via coupling were considered. Parameters S21, S11 and electric field distribution were calculated for RDL with pads and TGVs. However, this model wasn’t verified for ultra-short vias in thinner glass substrates.

![Figure 12: Finite Element Modeling of TGVs with varying TGV diameter [15]](image)

2.1.2 High-density TGV array modeling:

The authors in [16] have proposed a wideband circuit modeling approach based on a cylindrical mode expansion of electromagnetic field around perfect magnetic conductors (PMCs), to analyze the electrical properties of high-density TGV arrays. The equivalent circuit model of the SGS TGVs and the S- Parameter results are shown in Figure 13. Figure 14 shows the TGV
arrays used for EM modeling and the Re-Distribution Layer (RDL) to TGV transition used in the study. The results are shown in Figure 15.

Figure 13: a) Perspective view of the equivalent circuit model for SGS TGVs b) Inductance value of the proposed via configuration [16]

Figure 14: a) Perspective view of the TGV arrays b) 3D EM model developed for studying the RDL-TGV transition [16]

The literature claims that, the PMC boundary used in the cylindrical mode method greatly simplifies the corresponding equivalent circuit of TGV arrays. However, the taper effect and other manufacturing and metallization induced effects are not included in the study.
Similarly, 3D full wave EM solvers have been used to study the insertion loss and cross-talk behavior of TGVs at higher frequencies [17,18]. However, the glass thickness was greater than 100 µm and the manufacturing induced effects are not modeled. In addition, the effect of the via pad and the aperture size was not included in the study. Chien [19] from Industrial Technology Research Institute in Taiwan studied the TPV array that is constituted by six ground TPVs with one signal TPV (G6S1). This study involved simulations and measurements in the frequency range of 0.1 - 20 GHz. It was concluded that without ground planes or signal pads, the G6S1 array had identical characteristics with coaxial TPV. Also, Hwang [20] from KAIST of South Korea studied the TPV-to-TPV noise coupling to a 2.4 GHz low-noise amplifier (LNA) in Radio-frequency (RF) glass interposers. A modified noise figure equation was proposed to include the TPV-to-TPV noise. However, this study lacks a detailed high frequency analysis of the TPVs.

### 2.1.3 Π-circuit Model of TGVs:

Recently, Kim from University of Florida [21] proposed a π- circuit model for electrical parasitic estimation of TGVs, shown in Figure 16 and the lumped element parameters (RLGC) were extracted from 3D EM simulations. It was pointed out that the TPV with a diameter of 90
μm and a height of 500 μm, buried in a glass substrate with \( \varepsilon_r = 7.9 \) and \( \tan\delta = 0.008 \), had a resistance of 2.2 Ω, an inductance of 0.3 nH, a conductance of 0.01 S, and a capacitance of 1.8 pF at 1 GHz.

![Figure 16: a) π-circuit model and b) Dual via chain CPW-MSL transition proposed in [21]](image)

Also, Kim [22] from KAIST of South Korea proposed a precise RLGC circuit model, as shown in Figure 17. In addition, many different RF test fixtures and de-embedding methods have been reported to extract the lumped elements (RLGC) of via interconnections [23], [24]. In [23], a simple structure consisting of 50 Ω impedance matched Transmission Lines [TLs] on both sides of the glass substrate were connected through a via. This structure is suitable for analytical and full wave EM modeling; however, the network analyzer characterization becomes challenging, due to the need of the wafer probes on both sides of the substrate. In literature [24], T circuit model was used to extract the lumped elements of the via by printing the TLs on the same side of the substrate with a single via placed in the middle of the transmission line. However, this model requires a shunt capacitor between the via and ground plane, which induces additional parasitics in the evaluation of the lumped element values of the vias.
2.1.4 Modeling of TPVs in polymer laminated glass substrates:

The electrical behavior of TPVs (via parasitic, insertion loss, NEXT and FEXT) in polymer laminated glass substrates has been studied by T. Bandhyopadhyay in his PhD thesis through modeling and characterization, considering TPV geometry and polymer material variations [25]. The thickness of the glass substrate used for modeling and characterization was 75µm-180µm with TPV diameter greater than 30µm. However, the study lacks a comprehensive analysis of the high frequency electrical behavior of small diameter TPVs in thin glass substrates (<75 µm). Also, a preliminary electrical simulation results of small pitch TPVs (< 30 µm) in thin glass substrates (30 – 50 µm) were reported by Vijay Sukumaran in his PhD thesis [12]. However, this study was a preliminary investigation of microwave behavior of the fine pitch TPVs and lacked a comprehensive analysis. Also, the author has mentioned about the worthiness of performing a high frequency analysis of TPVs for high performance systems. Similarly, Gokul Kumar in his PhD thesis [26] has proposed novel power noise suppression techniques in glass interposers, considering the effect of the glass vias, for high bandwidth memory applications. However, this study wasn’t focused on the detailed electrical modeling of the via parasitics for RF and 5G systems. In the module level design, the low loss associated with glass vias was exploited to design RF filters and phase-shifters using MEMS [28 -31].
2.2 Prior work on thin glass handling methods:

Most of the prior work on glass interposers has focused on thicker glass substrates (300-500μm) with process steps implemented on bare glass. In contrast, this research studies and explores ultra-thin glass (50 – 100 μm) for interposer applications. The electrical significance of thin glass substrates was clearly described in the previous chapter. However, ease of thin glass handling is identified as one of the major challenges in its demonstration. This section overviews some of the most popular methodologies for handling bare and polymer laminated glass substrates.

2.2.1 Bare glass handling:

Glass panels (100 – 500 μm) are readily available in large panel formats for display and telescope purposes [32, 33]. However, processing thin glass substrates for electronic packaging involves many chemical processing steps and this underlines the need for the protection of thin substrates from crack formation and propagation. Asahi Glass Company from Japan has recently developed a carrier based methodology for handling thin glass panels upto 0.1mm thickness [34]. However, this approach cannot be used for double-sided processing of glass substrates for 3D interposer applications. The thickness of the carrier substrate is typically 500μm or higher. Corning, one of the leading manufacturers of Glass and Glass ceramics published an article in Microsystems, Packaging, Assembly and Circuits Technology Conference (IMPACT) about the development of thin glass substrates and handling methodologies for reliable metallization of copper interconnects[35]. In addition, Corning Glass has also studied the mechanical properties of glass substrates , in comparison to the silicon substrates in [36]. All these literature serve as a guidance in understanding the failure mechanisms in glass processing, as a function of defect density within the material.
2.2.2 Low – loss polymer lamination on glass substrates:

The use of polymeric coatings on glass for handling is well known in the display industry. GT-PRC introduced the concept of using novel polymer dielectrics on the glass surface for improved handling [37]. Also, the polymer acts as a buffer between the low-CTE glass (3 ppm/K) and copper metal (17 ppm / K). This is important for the thermo – mechanical reliability of the planar and vertical through interconnects. The effect of polymer coatings on glass surfaces subjected to indentation loads has been studied [38, 39]. The lower modulus of the polymer was reported to cause reduction in the indentation stresses generated on the surface of the glass. In addition, experiments have been performed which confirm the improvement in the strength of thin glass substrates upon the use of thin organic polymer films upon them [40-43]. However, this step introduces an additional process in the opening of vias on the polymer, to access the glass vias. The laser opening of the polymer requires that the glass vias be drilled with μm level positional accuracy.

2.3 Prior work in Copper-metallization of through-package-vias (TPVs):

Reliable copper metallization of fine pitch and high aspect ratio Through Package Vias (TPVs) in glass is challenging due to the high degree of mismatch in Co-efficient of thermal expansion (CTE) between glass (3 ppm/K) and copper (17 ppm/K) as well as poor adhesion due to their contrasting chemical structures, and ultra-smooth surface of glass. Physical vapor deposition (PVD) metallization using an adhesion layer of Titanium or Chromium, followed by deposition of copper has been demonstrated for metallizing glass substrates with TPVs [44]. However, this approach suffers from aspect ratio limits due to line of sight deposition, as well as lack of a stress buffer between Cu and glass. Few copper – glass adhesion enabling technology
including the process of using sol gel, to enable conformal TPV coverage is highlighted in [45 - 49].

2.4 Prior-work on high frequency characterization of TGVs:

Cheolbok Kim in [21] has developed a micro machined Microstrip ring resonator to extract the RLCG parasitics of the TGVs upto 10 GHz. However, the emerging RF and 5G systems require the through interconnect characterization upto 30 GHz. Jialing Tong in his PhD thesis [27] defense has used Microstrip ring resonator based test fixtures to extract the RLCG parameters from the resonance effects. However, this method gives accurate values only at specific basis and harmonic frequencies. Lee [50] from Dankook University of South Korea developed a novel fabrication method of copper-filled TPVs in glass for wafer-level RF MEMS packaging. Such fabrication process was applied to the building of a coplanar waveguide (CPW) transmission line to investigate their RF performance. The measured insertion loss of the whole package was 0.197 dB and the return loss was 20.032 dB at 20 GHz as plotted in Figure 2.6, showing minor impact from TPVs.

It can be noted that most of the prior literature on electrical modeling and demonstration has focused on thicker glass substrates (> 100 µm) with larger via diameters (> 30µm). This research goes beyond the prior art in studying the signal integrity of small-diameter vias (20 – 60 µm) in two-metal layer, ultra-thin glass substrates (50µm). This study represents the first demonstration of a wave dimensional analysis technique for accurate evaluation of the electrical parasitics of small diameter TPVs (20 – 60 µm) in thin glass substrates (50 µm). Also, a precise model – measurement correlation is reported using Through Reflect and Load (TRL) calibration technique, upto 30 GHz.
CHAPTER 3

ELECTRICAL MODELING AND DESIGN OF SMALL -DIAMETER, FINE-PITCH TPVs

Through-Glass-Vias (TGVs) are a critical component in 3D glass interposer technology and the accurate estimation of their electrical parasitics is a key requirement for obtaining high performance in digital and analog RF modules, on 3D glass packages. Wide band circuit modeling techniques have already been proposed, for evaluating the loss characteristics. These approaches are less computationally intensive and scalable for various through-package-via (TPV) dimensions. Yet, they lack accurate representation of their high frequency behavior and highest achievable model -measurement correlation. This is due to the limitation of the models in incorporating manufacturing, metallization and measurement induced errors. To overcome these limitations, this research proposes wave dimensional analysis of the TPVs in frequency ranges up to 50 GHz. Precise model – measurement correlation is reported up to 30 GHz. Also, this technique can be extended to THz frequency applications.

This chapter presents a detailed study of the electrical modeling of the TPVs and is divided into three sections. First section reports a unique and scalable technique for the accurate estimation of electrical parasitics of TPVs including AC resistance and inductance. The fundamental working principle, electromagnetic simulation model and the results are discussed in detail. The second section analyses the behavior of TPVs when integrated with 50Ω Transmission Lines (TLs). The effects of impedance discontinuity and reference plane interference are analyzed through 3D EM models built and simulated using Ansys HFSS™. Finally, the results from both the sections are utilized to establish the need for small diameter TPVs at fine pitch, along with tighter design rules, for improved signal and power integrity of 3D glass packages.
3.1 Overview of TPV losses:

Ideally, the through-vertical interconnections connecting the metal layers on top and bottom of the core substrate, should have the following characteristics:

i) Zero values for parasitic Resistance, Inductance, Capacitance and Conductance (RLCG) parameters for improved power integrity, with no simultaneous switching noises.

ii) Insertion loss = 0 dB, for lossless delivery of high frequency signals through the vertical interconnections.

However, during implementation, the electrical losses from a TPV arise from the conductor, dielectric, and the impedance mismatch losses, as shown in Figure 18. It is quite challenging to distinguish the parasitic contributions from each factor. Hence this study estimates the losses, as an amalgamation of the factors listed in Figure 19. Additionally, any defect, in the manufacturing including the crack formation, and the metallization can cause the behavior of TPVs to deviate from the normal.

Figure 18: Cross section of 2ML stack up with TPVs, on a 3D glass package
From the electrical design perspective, impedance discontinuity between TPVs and 50 Ω TLs, is the major optimization parameter. The impedance mismatch can cause additional transmission losses, increased delay and ultimately affecting the bandwidth. A simple examination of these effects can be done, by comparing the performance of the Co-planar waveguide (CPW) structures, with and without TPVs, as shown in Figure 20. 3D EM models were built, to simulate the S-parameters of the two structures. The CPWs were modeled for 50 Ω characteristic impedance and the diameter of the glass vias was kept at 60 µm. Both the structures were simulated for a total length of 2.4 mm. The insertion loss values are plotted in Figure 21. As can be observed, CPWs with TPVs suffer additional losses upon the ones without TPVs. This can be attributed to any combination of the factors listed in Figure 19. As frequency of data transmission signals increase, it becomes very critical to characterize the behavior of through interconnections in a sufficiently accurate way, to be able to consider high frequency effects that may occur. Detailed study of these effects and demonstration of ultra-low loss (< 0.03 dB/mm) through interconnects is the focus of this research. The accurate measurement of these parasitics is also important to reduce the design iteration cycles for building 3D digital / RF modules.
Estimation of TPV parasitics:

A unique and simplified technique based on transmission line theory is proposed, to estimate the parasitic effects of the vertical through interconnections. This approach incorporates proper de-embedding techniques and is also scalable to mm-wave regime. This becomes very critical in the co-integration of high density digital and high-performance RF components on the 3D packages.

A single glass via could be effectively modeled as series resistance and inductance, as shown in and the total impedance is given in Equation I. This includes the assumption that the capacitive coupling between the TPVs and the reference ground plane is negligible. As the
thickness of the substrate is further reduced for building ultra-miniaturized modules, these effects become significant and need to be estimated accurately.

\[ Z = R + j*\omega*L \]  --  Equation I

Figure 22: Input impedance method to estimate TPV parasitics

3.2.1 Wave-Dimensional Analysis:

The proposed approach known by input impedance method consists of a 50 Ω CPW shorted to the ground plane, by means of a TPV of specific diameter and capture pad size. Ideally, the input impedance of such a shorted network should equal Equation II, which essentially excludes the via parasitics.

\[ Z_{in} = j * Z_o * \tan(\beta l) \]  --  Equation II

At GHz frequencies, such approximations don’t hold true and this study focuses on evaluating the electrical parasitics of such through interconnections. Post – inclusion of the via load, the input impedance of the network in Figure 22 can modified as in Equation III.

\[ Z_{in} = Z_o \frac{Z_l + j Z_o \tan \beta l}{Z_o + j Z_l \tan \beta l} \]  --  Equation III

where \( Z_l = R + j\omega L \), R – resistance, L – inductance, is the impedance of the TPV connecting the signal trace to the ground plane. \( \beta = (2*\pi) / \lambda \) is the propagation constant of the wave travelling in
the medium. \( l \) is the length of the CPW before its signal trace gets terminated with the ground plane. \( Z_o \) is the characteristic impedance of the CPW, which is equal to 50 \( \Omega \).

**Table 3: Electrical properties of Glass**

<table>
<thead>
<tr>
<th>Glass Properties (@ 5GHz)</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dielectric Constant</td>
<td>5.1</td>
</tr>
<tr>
<td>Loss Tangent</td>
<td>0.0049</td>
</tr>
<tr>
<td>Electric volume resistivity</td>
<td>( 7.9 \times 10^{11} \Omega \cdot \text{cm} )</td>
</tr>
</tbody>
</table>

3D Electromagnetic (EM) models based on this approach were built using Ansys HFSS™. The electrical properties of glass, used in the simulation model are given in Table 3. For a one port measurement, \( S_{11} \) is given by Equation IV [51].

\[
S_{11} = \frac{Z_{11} - 1}{Z_{11} + 1}
\]

--- *Equation IV*

This agrees with the result for the reflection co-efficient seen, looking into a load with a normalized input impedance of \( Z_{11} \). By appropriately substituting the values for \( \beta, l \) and \( Z_o \) in Equation III, the value of \( Z_l \) can be calculated. The real and imaginary parts of \( Z_l \) can be duly disseminated, as the resistance and the self-inductance of the vias. The inductance is considered a parasitic, because it opposes any alternating change in the current, and this causes a delay in the signal transmission. The resistance, which is the combination of AC and DC values can cause reduction in the signal amplitude, whereas the delay effect of the inductance affects the bandwidth. The physical parameters used in 3D EM modeling are tabulated in Table 4 and the results of the parasitic estimation are plotted in Figure 23 and Figure 24. The graph shows clear distinction between the via properties in 50, 130 \( \mu \text{m} \) glasses.

**Table 4: 2ML stack up details considered in this study**
These parasitics account for the skin and the proximity effect, when high alternating current is passed through the via. The gradual increase in the resistance value, as can be observed in Figure 23 is due to the skin effect and the skin depth is given by Equation V. The skin depth, denoting the region of current flow, decreases with frequency and this causes the conductor losses to ramp up.
\[ \delta = \frac{1}{\sqrt{\pi \ast f \ast \mu \ast \sigma}} \] \quad \text{--- Equation V}

Consequently, the self-induced EMF will be greater towards the center of the conductor, thus causing the current density to be less at the center than the conductor surface. This extra concentration at the surface, also known as proximity effect results in a decreased value for the TPV inductance at higher frequencies.

3.2.2 Loop Inductance Retrieval and Pitch effect:

In circumstances where signal and ground vias are placed next to one another, the estimation of their loop inductance become critical. The circuit model in Figure 25, representing Ground – Signal via configuration was used to extract the loop parasitics.

\[ Z_{11} = 2(R + j(2\pi fL - \frac{1}{2\pi fC})) \]

![Figure 25: Loop Inductance retrieval in GS vias](image)

The capacitance of the GS via structure, for a fixed diameter and pitch is considered negligible because glass is an excellent dielectric, with lower dielectric constant value, as given in Table 3. The loop inductance variation with TPV pitch is shown in Figure 26. The results indicate a decreased loop inductance for smaller TPV pitch, which is attributed to the reduced magnetic flux storage around the fine-pitch GS vias.
All these parasitics, show up as the impedance, given by the analytical Equation I and plotted in the Figure 27. It is inferred from the graph that, TPV dimensions with proper combinations of diameter and pitch can lead to 50 Ω impedances, to achieve the target of < 5% impedance discontinuity between the transmission lines and the vertical interconnections. In case of the stack up used in this study, as shown in Figure 18, signal TPVs of diameter ~25 µm at ~50 µm pitch can give the desired impedance.
3.3 Transmission Line – TPV signal transition:

This section discusses the interfacial losses when high frequency signals transition from a planar to a vertical through interconnection. This effect can be characterized using a dual via chain structure, as shown in Figure 28.

**Figure 28 Dual via chain structure to characterize losses in TL – TPV interface**

In this study, dual via chain consisting of Coplanar WaveGuide (CPWG) – CPWG structures is enabled by two sets of GSG via transitions. As calculated in the previous section, these vias exhibit parasitic losses including AC resistance, inductance cumulating to a specific value of impedance, as given in Figure 27. One of the focus areas of this research is to reduce the impedance discontinuities between the 50 Ω Transmission Lines and the TPVs, by adjusting the TPV diameter and the pitch. Figure 29 shows the simulated insertion loss value of the entire dual via chain structure for three varying via diameters. The resonance effects seen around 25 GHz in glass interposers suggests that systems need to be avoid operated at that frequency. The resonant effects are explained in detail in section 3.3.1.
Figure 29 Insertion loss of CPWG – CPWG dual via transition

It is clearly observed that smaller vias show better performance in terms of lowered insertion and return loss values. It is because, the impedance of the smaller vias match well with the transmission lines, as compared to the larger diameter. This is confirmed by plotting the respective VSWR values, shown in Figure 30.

Figure 30 VSWR of CPWG – CPWG dual via transition

The VSWR values play a major role in determining the amount of reflected power to the source as sown in Figure 31. The standing wave ratio values should be below 2 to design a low power consuming device.
Due to the better impedance match of 20µm diameter vias to the CPWG lines, their Voltage Wave Standing Ratio (VSWR) is nearly equal to one. This greatly reduces the signal bounce back to the source and hence a lesser delay, greater bandwidth, as depicted in Figure 32. For this reason, smaller vias are preferred for connecting the antenna on one side to the mm wave ICs on the other side in a Glass Fan out or a 3D package architecture.
3.3.1 Resonance effects in GSG vias:

One another significant effect that can be recognized with via chain structures is the resonance shown in Figure 29. It is attributed to the series RL, parallel RC network configurations between the TLs and the GSG via structures. To analyze this effect in detail, the impact of the capture pad and the aperture size of the TPVs are studied using the 3D model shown in Figure 33.

![Figure 33 3D view of vias penetrating the ground reference plane](image1)

Figure 33 3D view of vias penetrating the ground reference plane

Figure 34 shows the vias penetrating the ground and power reference planes, As can be observed, the capture pad size has significant role in resonance effect in the via chain structures. Also, keeping the capture size at its minimum significantly improves the signal transmission performance, by offering lower parasitics and decreased resonance effect at around 25 GHz.

![Figure 34 3D view of vias penetrating the ground and power reference plane](image2)
3.4 Extraction of TPV losses from TL-TPV transitions:

The insertion loss of the GSG TPVs are obtained by de-embedding the effects of the CPW transmission lines from the dual – via-chain structure shown in Figure 28. Cascaded ABCD parameters shown in Equation VI are used in calculating the loss characteristics of the GSG TPVs. They consist of ABCD values of CPW dual via chain structure (d), CPW TLs (t), CPW-via transition effects arising from the 90 degree bends, the impedance discontinuity and the pad effects(t-v), parasitic effects of the TPVs only(v). The ABCD values of the dual via chain structures are estimated from the corresponding S parameters. The insertion loss values of the GSG TPVs including the impedance discontinuity, 90 bends and pad effects are plotted in Figure 35. To de-embed the effects of 90 bends and the pad effects, 3D EM model shown in Figure 36 was used. It consists of two ports places on the either side of the GSG TPVs. Since the high-frequency signals are directly launched into the vias, the 90° bends and the pad parasitic effects are eliminated. But it shall be noted that the ports are re-normalized to 50 Ω to include the impedance discontinuity effects. The results for varying TPV diameters are plotted in Figure 37.

\[
\begin{bmatrix}
A^d & B^d \\
C^d & D^d
\end{bmatrix} = \begin{bmatrix}
A^t & B^t \\
C^t & D^t
\end{bmatrix} \ast \begin{bmatrix}
A^{t-v} & B^{t-v} \\
C^{t-v} & D^{t-v}
\end{bmatrix} \ast \begin{bmatrix}
A^v & B^v \\
C^v & D^v
\end{bmatrix} \ast \begin{bmatrix}
A^{t-v} & B^{t-v} \\
C^{t-v} & D^{t-v}
\end{bmatrix} \ast \begin{bmatrix}
A^t & B^t \\
C^t & D^t
\end{bmatrix} \ast \begin{bmatrix}
A^{t-v} & B^{t-v} \\
C^{t-v} & D^{t-v}
\end{bmatrix} \ast \begin{bmatrix}
A^v & B^v \\
C^v & D^v
\end{bmatrix} \ast \begin{bmatrix}
A^t & B^t \\
C^t & D^t
\end{bmatrix} \ast \begin{bmatrix}
A^{t-v} & B^{t-v} \\
C^{t-v} & D^{t-v}
\end{bmatrix} \ast \begin{bmatrix}
A^v & B^v \\
C^v & D^v
\end{bmatrix} \ast \begin{bmatrix}
A^t & B^t \\
C^t & D^t
\end{bmatrix} \ast \begin{bmatrix}
A^{t-v} & B^{t-v} \\
C^{t-v} & D^{t-v}
\end{bmatrix} \ast \begin{bmatrix}
A^v & B^v \\
C^v & D^v
\end{bmatrix} \ast \begin{bmatrix}
A^t & B^t \\
C^t & D^t
\end{bmatrix} = \text{Equation VI}
\]
Figure 35 Insertion loss (dB) of GSG TPVs including the impedance discontinuity pad effects and 90° bends

Figure 36 3D EM model used to de-embed the effects of pad parasitics and 90° bends, includes impedance discontinuity
3.5 Electrical Benefits of Small-diameter TPVs at Fine – pitch:

3.5.1 High Frequency Antenna Feed Lines:

Conductor Backed Co-planar Waveguides (CB–CPWGs) and Substrate Integrated WaveGuides (SIWs) are gaining much interest, as antenna feed lines, for their low loss and high shielding benefits. The high performance is largely enabled by the via arrays, used for shorting the ground lines and the ground planes, as shown in Figure 38. For better efficiency in shorting, it is preferred that the vias are placed at a pitch of $\lambda_{eff}/20$. For the applications involving RADAR at 77 GHz and above, the effective wavelength calculations suggest that minimum of 90 $\mu$m pitch is preferred between the vias, in the via array. For reliability concerns, it is suggested that the TPV pitch should be minimum of twice the diameter. Hence, smaller via diameters at fine pitch is a strategic need for the high frequency and high performance antenna feed lines. The insertion loss values for CB-CPWg of length 3.6 mm with TPV arrays of diameter 45 $\mu$m placed varying pitches are plotted in Figure 39.

Figure 37 Insertion loss (dB) of GSG TPVs excluding the pad parasitics and 90° bends, including the impedance discontinuity effects
3.5.2 Noise Coupling in Mixed Signal Systems:

Heterogenous integration involves side by side or double-sided assembly of digital and analog ICs in 2.5D / 3D package architectures. In this scenario high switching digital signals can couple with high performance RF signals through the vertical interconnections and degrade the performance of the latter. To analyse these effects, analytical study on the inductive and capacitive coupling effects, is performed using Equation VI and VII respectively. Both the digital and analog vias are considered for the study, with different voltage levels, running parallel, as shown in Figure 40. The inferential results are tabulated in Table 5. It is noted that the smaller via diameter
exhibits less inductive and capacitice coupling with neighbouring signal vias and very effectively reduces the noise coupling effects.

\[
K_L = \frac{L_m}{L_{TPV} + \frac{1}{2} L_{TPV}}
\]  \hspace{1cm} \text{--- Equation VI}

\[
K_C = \frac{C_m}{C_{GLS} + C_m}
\]  \hspace{1cm} \text{--- Equation VII}

Figure 40 Inductive and capacitive noise coupling in TPVs

**Table 5: Noise coupling in TPVs with varying diameters**

<table>
<thead>
<tr>
<th>TPV Dia.</th>
<th>(L_{TPV})</th>
<th>(C_{GLS})</th>
<th>(C_m)</th>
<th>(K_C)</th>
<th>(K_L)</th>
</tr>
</thead>
<tbody>
<tr>
<td>(\uparrow)</td>
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</table>

In addition, it is proposed that having multiple ground vias, adjacent to the signal vias can be effective in supressing the noise coupling in RF signals. To study this proposal in detail, eye–diagram simulations were performed for Signal–Signal and G4S2 via configurations, as shown in Figure 41 and Figure 42 respectively. The eye diagram simulation for G4S2 is given in Figure 42. It is observed that the ground vias surrounding the signal vias act as a shielding cage for better field termination. The via configuration Figure 42 with ground via caging, shows wider eye opening, as compared to the one with only signal vias. This could be attributed to the supression
of resonance effects in the signal transmission, as well as the enhanced field terminations. This is one of the major drivers for small diameter vias at fine pitch for 3D glass packages.

Figure 41 Eye Diagram simulation of SS Via configuration

Figure 42 Co-axial ground TPVs to reduce noise coupling between signal TPVs
3.6 Summary

3.6.1 Design Guidelines for Small Vias at Fine – pitch in Ultra – thin glass:

The detailed electrical modeling of the smaller via diameters at fine pitch, in 50 µm thin glass substrates led to the following design rules. The proposed via dimensions and configuration satisfy the target of achieving less than 5% impedance discontinuity, reduced noise coupling, and enhanced shorting efficiency.

i) Through Glass Vias could be represented as series combination of resistance and inductance. The capacitance effect could be considered negligible due to the lower value of dielectric constant of glass.

ii) The choice of optimal via diameter and the pitch, to achieve less than 5% impedance discontinuity with 50 Ω transmission lines, is dictated by the TPV’s inductive behavior. The modeling results suggest that smaller via diameters (~25 µm) at fine pitch (~50 µm) gives the near 50 Ω impedance for TPVs. When integrated with transmission lines,
the VSWR value was approximately equal for a wide range of frequencies up to 50 GHz, indicating a perfect impedance match, leading to lesser delay and higher bandwidth.

iii) The resonance effect in TPVs integrated with transmission lines, can be greatly reduced by keeping the capture pad and the aperture size at its minimum, also considering its manufacturability. The high potentiality for smaller via capture pads and aperture sizes, is one of distinguishing advantages of glass vias as compared to its organic counterparts. This is enabled by the exceptional dimensional stability of the glass substrates.

iv) A via cage with co-axial ground TPVs around the signal TPV, is proposed as an efficient technique for noise coupling reduction, in high density, heterogeneous integrated systems. This is confirmed through the eye diagram simulations of the proposed configuration of ground and signal via.
CHAPTER 4
ULTRA-THIN GLASS HANDLING AND TPV METALLIZATION

Ultra – thin glass is an outstanding candidate for building ultra-miniaturized and high-performance 3D packages. Glass possesses high dimensional stability, enabling fine line lithography and precision RDL structures, with accurate layer to layer via registration. Yet they face two main fundamental challenges in terms of its handling ability and highly reliable copper metallization including Through-Package-Vias (TPVs). This is due to the stresses caused by the high degree of mismatch in Co-efficient of Thermal Expansion (CTE) between glass (3 ppm/K) and copper (17 ppm/K). Proper surface activation using adhesion promoter is essential in achieving highly reliable metallization [7].

Low-loss polymer lamination on thin glass substrates was developed by the GT-PRC, as a means for defect-free handling of thin-glass [8]. The polymer films also provide stress-buffering between the copper interconnections and the glass. This research extends this novelty further, to an edge-protection technique on 50 µm ultra-thin glass substrate and is accomplished by edge-beading through polymer frame lamination.

The first section describes the proposed edge beading technique for 6” * 6” glass panels, along with the warpage analysis of the resulting stack-up. The second section discusses about the test vehicle design and fabrication process flow, for high frequency electrical characterization of TPVs in 50 µm glass core interposers.

4.1 Edge Protection for Thin Glass Processing:

Glass, being a brittle material faces fundamental challenge with the ease of handling and defect- free substrate patterning and metallization. The stress – strain graph, shown in Figure 44
[12] indicate that failures in glass occur due to brittle fracture. The strain values are significantly smaller (0.1%) at the corresponding stress values. Also, it is observed that the crack formation is prone to occur at the edges, especially in ultra-thin substrates. Furthermore, the cracks can easily propagate across the panel during each step of the fabrication process.

![Stress-strain relationship in glass and copper materials](image)

**Figure 44 Stress – strain relationship in glass and copper materials [12]**

### 4.1.1 Technique:

The concept of edge beading of polymers is introduced, to enhance the handling ability and mitigate the propagation of cracks in thin glass substrates. The mechanism consists of building a frame alike polymer beading, upon the low loss polymer laminated glass core, as shown in Figure 45. This proposal is basically an extension of the GT-PRC developed concept of low loss polymer lamination upon glass [12]. For the demonstration, the base polymer and the edge beading polymer were selected to be 5 µm and 20 µm thick respectively. The glass panel chosen for the study was 6” * 6” in size. Initially, the pristine glass substrate is surface activated using a customized silane treatment, for enhanced polymer adhesion. The vacuum lamination and curing of the base polymer
is followed by a similar procedure for the edge beading. The resultant stack up is 90 µm thick, as shown in Figure 46 and is easy to handle for further processing, due to the increased thickness at the edges.

![Figure 45](image1.png)

**Figure 45 Low loss polymer lamination on glass substrates, developed by GT-PRC**

![Figure 46](image2.png)

**Figure 46 Conceptual view of edge beading technique for 50 µm thin glass core processing**

4.1.2 Warpage Analysis:

One of the concerns during the edge beading process was the significant warpage, which was noticed in the resultant stack up in Figure 46, after lamination and curing. The occurrence of warpage during the manufacturing processes can further lead to misalignment of parts, reduced tolerances, and a variety of operational failures such as delamination and die cracking. To accurately study the warpage behavior, the laminated glass core was subjected to warpage analysis, using Shadow Moire tool, shown in Figure 47. It is a non-contact, full-field optical technique that uses geometric interference between a reference grating and its shadow on a sample, to measure relative vertical displacement at each pixel position in the resulting image [52].
Two edge laminated samples were prepared for sharp contrast imaging and placed in the Shadow Moire chamber for warpage analysis. The results of the study are shown in Figure 48 and Figure 49 respectively. The contour suggests the deformation in -Z direction. This is attributed to the imbalance in the polymer thickness across the area of the panel and the warpage is further increased during the process of curing. This research presents the initial work on the proposed technique of edge beading and there is a vast scope to expand the concept by varying the polymer thickness, to reduce the warpage and enhance the ease of handling.
Figure 48 3D Warpage analysis of the sample 1 of 50 µm glass core with edge beading

Max = 314 microns   Min = -144 microns   Bow = n/a   JEDECFullFiel

Figure 49 3D Warpage analysis of the sample 2 of 50 µm glass core with edge beading

Max - Min = 490 microns

Figure 49 3D Warpage analysis of the sample 2 of 50 µm glass core with edge beading

4.2 Electrical Characterization test-vehicle (TV) Design:

To validate the simulation models that were discussed in Chapter 3, Radio Frequency (RF) test fixtures were laid out using AutoCAD, considering Design for Manufacturability and Testability requirements. The stack up that was used for building the RF demonstrator Test Vehicle (TV) is shown in Figure 50a. The TV shown in Figure 50b is built on 50 µm low CTE glass core, with electrical properties given in Table 3.
4.2.1 Fabrication process flow:

The glass substrate with TPVs involve double-sided patterning and careful handling through each processing step. A via – first process, named via – in – via approach followed by semi-additive patterning, was utilized to metallize the TPVs. The metallization process comprises of electro less Cu seed layer deposition on polymer-laminated glass, followed by electrolytic plating of Cu. The entire process flow for the fabrication of the double sided ultra-thin glass substrate is depicted in Figure 51.

It was observed that the via – in – via approach offers significant advantages in terms of i) Reducing the stress effect due to the CTE mismatch between the glass and Copper. This is because the polymer lining in the via side wall acts as a buffer between the interacting surfaces. ii) Reducing the effect of the tapering effect of glass vias, by adjusting the profile of polymer lining on the side wall. However, this approach requires that the glass vias be drilled with high alignment accuracy, for symmetric lining of the polymer on the side walls.
4.2.2 Fabrication results:

The optical microscopic image of 50 µm glass substrate with pre-dilled vias of varying diameters is shown in Figure 53 and Figure 54. These glass substrates are supplied by leading glass suppliers.
Figure 53 Microscopic images of glass vias of entry diameter 70 µm and taper angle 75°

Figure 54 Microscopic images of glass vias of entry diameter 60 µm and taper angle 87°

Figure 55 shows the Zeta 3D microscopic image of the via opening on the polymer laminated glass. The via opening diameter on the polymer is usually around 15 µm lesser than that of the glass via, to allow for the polymer flow inside the vias. Figure 55b shows the crack formation around the exit of the through vias, due to the heating effect of the laser. Subsequently, it was removed through desmear, which also aids in the enhanced adhesion of seed layer Cu to the side walls of the vias, through electro less process.
Figure 55 Microscopic images of a) front & b) back, of 50 µm glass core, after polymer lamination and polymer via opening

Figure 56 Microscopic image of the cross section of a TPV after E-less seed layer deposition

From the Figure 56 it can be observed that the process of polymer via opening and the subsequent E-less Cu seed layer deposition is symmetric around the center axis of the glass vias. This also confirms the µm level accuracy of the glass via drilling. The 50 µm glass core RF demonstrator test vehicle fabricated using the process flow depicted in Figure 51, is shown in Figure 57 along with the TPV characterization structures. Entire 4” * 4” panel, also consisting of high Q inductor designs was yielded successfully for further electrical performance characterization. The results are discussed in Chapter 5.
4.3 Summary:

The need for edge protection of thin glass substrates was identified, to improve its handling ability. The low – loss polymer lamination approach, developed by GT-PRC was extended further to edge – beading of polymers. The implementation and warpage analysis of the resultant stack up was discussed in detail. The proposed approach is in the initial stages of development and needs further investigation to reduce the warpage and adopt for large scale panel fabrication.

RF text fixtures with TPVs were designed on 50µm thick glass core laminated with polymers, to validate the 3D EM models described in Chapter 3. A via first metallization techniques named via – in – via was utilized, followed by semi-additive patterning, for achieving highly reliable metallization of through vias in thin glass substrates (50 µm). Further, the side wall of the metallized through-vias in ultra-thin glass was analyzed through optical imaging of via cross sections.
CHAPTER 5:
HIGH-FREQUENCY ELECTRICAL CHARACTERIZATION

This chapter presents a detailed analysis of the electrical measurements of the metallized Through-Package-Vias (TPVs) in ultra-thin glass core (50 µm) packages. An in-depth analysis of the network analyzer measurement of the TPV structures, in a 50 µm thick glass core package is presented. The modeling and fabrication details of the Radio Frequency (RF) structures, designed for evaluating the electrical parasitics of the through interconnections, were discussed in Chapters 3 and 4 respectively. Wave dimensional analysis is used for the accurate characterization and model – measurement correlation of the electrical parasitics and dB/mm losses, of the through vertical interconnections, in 50 µm ultra-thin glass core substrates. This is also important to reduce the design iteration cycles for RF components and modules, involving TPVs.

5.1 mm-wave Characterization of TPV Parasitics:

Increased I/O density, bandwidth, and improved signal integrity are the key requirements for 2.5D and 3D package systems. The data rate consumption in today’s fast paced electronics world has reached a spot, where, even the low parasitics of via transitions in a 3D package, with inductances in ranges of pH has considerable impact on the system speed. Hence the accurate estimation of TPV parasitics including resistance, inductance and capacitance plays a significant role in the demonstration of high performance packages.
5.1.1 Through Reflect Load (TRL) Calibration:

Figure 58 Error box in the Vector Network Analyzer (VNA) measurement of RF structures [51]

RF characterization of low loss structures, including TPVs, demand high accuracy measurement with low calibration error. Figure 58 shows the error box between the VNA and the TPV characterization structures as the device-under-test (DUT). The error box consists of the parasitic effects of the cables and the probes. The objective is to remove these effects using calibration such that the reference plane is at the two ports of the DUT.

Figure 59 Reference plane for DUT in Through, Reflect and Line calibration steps [51]

Given this objective, this research utilizes the Through Reflect and Load (TRL) calibration technique that measures two transmission standards and one reflection standard to determine the 2-port 12-term error coefficients. Figure 59 shows the reference plane for the DUT in all the three steps of the TRL calibration. The Through (T) calibration, shown in Figure 59a consists of connecting the ports of the VNA together and performing S parameter measurements. The
measured values are substituted in the Equation VIII. By symmetry, $T_{11}$ should equal $T_{22}$ and $T_{12}$ should equal $T_{21}$.

$$T_{11} = s_{11} + \frac{s_{22} s_{12}^2}{1 - s_{22}^2} \quad \text{--- Equation VIII}$$

$$T_{12} = \frac{s_{12}^2}{1 - s_{22}^2} \quad \text{--- Equation IX}$$

The Reflect (R) task of the calibration process, consists of terminating a 50 Ω impedance matched Microstrip Line (MSL) with an open circuit, allowing high reflection from the load end and is shown in Figure 59b. The measured S parameters are substituted in the Equation IX. By symmetry, $R_{11}$ should equal $R_{22}$.

$$R_{11} = s_{11} + \frac{s_{12}^2 \Gamma_L}{1 - s_{22} \Gamma_L} \quad \text{--- Equation X}$$

The last step consists of connecting a 50 Ω impedance matched Transmission Line (TL) to the two ports of the VNA, as shown in Figure 59c. Subsequently, the measured S parameters are substituted in Equation XI, to obtain the through and reflect values of the TRL calibration parameters. By symmetry, $L_{11}$ should equal $L_{22}$ and $L_{12}$ should equal $L_{21}$. Cumulatively, this leads to five equations and five knowns and solving for them provides the $S_{11}, S_{12}$ of the cables and the probes. These values can then be appropriately deducted from the total measurement values including DUT, using [ABCD] to [S] transformation and vice-versa, as given in Equation XII.
TRL technique doesn’t require the values of $\Gamma_L$, $e^{-\gamma l}$ to be appropriate and this is one of the major benefits of using this technique.

\[ l_{11} = s_{11} + \frac{s_{12}^2 e^{2\gamma l}}{1 - s_{22}^2 e^{2\gamma l}} \quad \text{--- Equation XI} \]

\[
\begin{bmatrix} A^m & B^m \\ C^m & D^m \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \times \begin{bmatrix} A' & B' \\ C' & D' \end{bmatrix} \times \begin{bmatrix} A & B \\ C & D \end{bmatrix}^{-1} \quad \text{--- Equation XII}
\]

5.1.2 Evaluation of TPV Parasitics:

As discussed in Chapter 3, a transmission line model based on input impedance calculations, was developed to accurately capture the electrical parasitics of a single TPV. In this research, focusing on through interconnections in glass core, a single TPV can be safely assumed to be a series combination of a resistor and an inductor. The resistance and inductance values of a single TPV with varying diameters, in a 50 µm glass core which is double side laminated with 15 µm low-loss polymer, are estimated using a Vector Network Analyzer (VNA). The 3D EM model and the fabricated structure are shown in Figure 60.

![3D EM Model and fabricated structure for estimating RF losses of a TPV](image)

\[ Z_{in} = \frac{Z_0^2}{Z_l} \quad @ \frac{\lambda}{4} \]

Figure 60 3D EM Model and fabricated structure for estimating RF losses of a TPV
This technique is unique and beneficial in two ways:

1. As shown in Figure 60, at $\lambda_{\text{eff}} / 4$, the input impedance seen by the EM wave is given by

$$Z_{\text{in}} = \frac{Z_0^2}{Z_l}$$

where $Z_0 = 50 \, \Omega$ is the characteristic impedance of the CB-CPW, $Z_l$ is the desired value of the TPV impedance and $\lambda_{\text{eff}}$ is the effective wavelength of the EM wave travelling in the medium. This eliminates the need to consider the length of the TL and hence reduces the computation time, as compared to Equation III.

2. This characterization methodology has the de-embedding solution, rooted in the input impedance equation and eliminates the need for separate de-embedding structures, which require high accuracy.

The input impedance of the Transmission line shorted to the ground using a TPV, can be calculated from the S-parameter measurements from the VNA, using Equation XIII [51].

$$S_{11} = \frac{Z_{11} - 1}{Z_{11} + 1}$$  \hspace{1cm}  \text{Equation XIII}

The real part of the impedance corresponds to the resistance offered by a single TPV, when high frequency signal is passed through it. Both the simulation and measurement results of the AC resistance of a signal TPV of glass diameter 60 $\mu$m, are plotted in Figure 61. The results indicate an increasing value, attributed to the skin effect in the via, as high frequency AC signal is passed
through it. The skin effect forces the current to constrain to few µms of its surface cross-section, also known as skin depth, leading to an increased value of resistance as well as inductance.

The imaginary part of the input impedance is a summation of inductive and capacitive reactance, as shown in Equation XIV. Owing to the low dielectric permittivity of the glass and polymer dielectric materials, the capacitance of GS and GSG TPVs is safely assumed to be negligible. Subsequently the self-inductance of a single TPV is extracted from Equation XIV, post-substitution for the assumption of negligible capacitance. The TPV inductance values from 3D EM model and two measured coupons are plotted in Figure 62.

\[ Im(Z_{11}) = j \omega l - \frac{j}{\omega \varepsilon} \quad -- -- -- \text{Equation XIV} \]

The inductance of the conformally plated vias, decreases with increasing diameter. This is due to the reduced opposition to the changing current, with increased conductor cross-section in larger vias. However, this increase in impedance is beneficial in matching the 50 Ω impedance.
matched TLs to the TPVs, with reduced reflection losses at the interfacial surface, and is discussed in the next section.

5.2 TL – TPV Transition:

Through-package-vias (TPVs) are an integral part, in connecting the mm Wave ICs on one side and antenna on the other side, in low loss 3D package configuration. In most realistic designs, the TPVs are integrated with 50 Ω impedance matched TLs including Microstrip Line(MSL), Co-Planar Wave Guide(CPWG) and Conductor-Backed Co-Planar Waveguide (CB-CPWG), to serve as antenna feed lines and signal carriers. Given this interconnect network, the dominant loss factor is the impedance mismatch between the TLs and the TPVs.

![Figure 62: Modeling and measurement values of TPV inductance for glass diameter 60 µm](image)

Figure 62 Modeling and measurement values of TPV inductance for glass diameter 60 µm

One of the main objectives of this research is to reduce this impedance mismatch to ≤ 5%, by varying the signal and ground via diameters. To study these effects, CPWs without vias and dual via chain structures with Co-Planar Wave Guides with glass via diameter 60 µm were designed and fabricated. The polymer via diameters were kept at 45 µm. The length of the entire structure including the TPVs was kept at 3.46mm. The insertion loss values from the 3D EM model
and the VNA characterization are plotted in Figure 63. The structures exhibit total insertion loss of 0.24 dB. This is by large attributed to the impedance mis-match between the TLs and TPVs, in case of larger via-diameters. Further reduction in the signal transmission loss can be achieved by exploring sub 20 µm diameter TPVs.

The insertion loss of a 50 Ω impedance matched CPW line of length 3.2mm is characterized to be 0.13 dB. The insertion loss of the CPW segment was de-embedded from the CPW-CPW dual via chain structure to obtain an insertion loss of 0.028 dB/mm for the GSG vias. It shall be noted that these loss values also include the parasitic effects of the pads and the effects caused by the 90° bend in the TL-TPV transition. From these results, it can be concluded that reduced impedance discontinuity is beneficial in limiting the magnitude of the signal reflections at the TL-TPV junction, which can be confirmed through VSWR calculations.

Figure 63 Insertion loss values of CPW and dual via chain structures

From the phase information of the dual via chain structures shown in Figure 64, the delay of a signal TPV can be calculated, by de-embedding the effect of 50 Ω TLs. For calculation purposes, [ABCD] to [S] parameter conversion is used and the delay of a signal TPV is measured
to be 0.32 ps for the glass via diameters of 60 µm. The precise model to measurement correlation is achieved by 3D EM modeling using HFSS by including:

i) The varying via diameters in polymer and the glass including the different entry and exit via diameters due to the tapering effect.

ii) Conformal via metallization.

iii) Via pad and anti-pad size.

Figure 64 Phase of S$_{21}$ (Deg) of CPW and dual via chain structures

5.3 Summary:

In this chapter, the high frequency measurements of TPVs, in a 50 µm glass core package, were analyzed in detail, besides reporting precise model-measurement correlation up to 30 GHz. The precision was attributed to the high accuracy of the unique Transmission Line (TL) based model, which was proposed to evaluate the RF losses of small-diameter TPVs. The new methodology based off input impedance calculations, was used to capture the resistance and reactance of a signal TPV. It was observed that vias with smaller diameters exhibit better
impedance match to the 50 Ω TLs and hence offer reduced reflection losses at the interfacial surface between TLs and TPVs. This establishes the rationale behind the need for smaller via diameters in 3D RF packages.
CHAPTER 6:

RESEARCH SUMMARY AND SUGGESTIONS FOR FUTURE WORK

This dissertation represents the first comprehensive study of the high-frequency electrical modeling and characterization of small-diameter (20 - 60 µm) through-package-vias (TPVs) in 50 µm ultra-thin 3D glass interposer packages, up to 30 GHz. As a result, high speed package planar and vertical interconnects with insertion loss as low as 0.04 dB/mm and 0.028 dB/mm, were achieved—a 6X reduction compared to a similar study reported with silicon interposer [53].

To achieve highest data rate per unit of power, at lowest cost and smallest form factor, ultra-thin 3D glass interposers (30 -100 µm) with fine-pitch TPVs were proposed and demonstrated by GT-PRC, as a compelling alternative to 3D stacks with TSVs [12]. This approach achieves high logic – memory bandwidth and requires frequent use of vias to connect signal lines between different layers. However, a detailed signal, power integrity analysis and design guidelines for through-vertical interconnects, in thin glass substrates (30 – 100 µm) has not been well-documented. Another important development is that most analog and digital signal transmissions in emerging smart systems belong to the Radio Frequency (RF) regime from a few hundred MHz to several GHz. This research identified the electrical significance of ultra-thin glass substrates with small diameter TPVs and went beyond the prior work, by performing a systematic and fundamental microwave analysis of the small – diameter, fine-pitch TPVs in thin glass (50 µm) substrates. As a result, tighter design guidelines were provided for TPVs, in building high-performance 3D glass based mixed signal integrated systems.

The following fundamental challenges were identified in the design and demonstration of low-loss through vertical interconnects in thin-glass substrates i) High – frequency effects in the accurate evaluation of low-loss parasitics in ultra-short TPVs ii) Impedance mismatch between the
Transmission Lines (TLs) and the TPVs iii) Handling of ultra-thin (50 µm) glass iv) Precise model-measurement correlation. The data and analysis presented in the previous chapters prove that the research objectives were met successfully.

The strategic need for thinner glass substrates, with ultra-short and ultra-low loss vertical interconnects, was identified through detailed 3D Electromagnetic (EM) modeling. Subsequently, a novel electrical modeling technique based on transmission line theory, was developed to estimate the parasitics of the ultra-short signal TPVs, upto 50 GHz. The fundamental analysis on the results, led to the proposal of small – diameter TPVs for achieving <5% impedance discontinuity, when integrated with 50 Ω impedance matched TLs. In addition, precise model-measurement correlation was obtained in the high frequency electrical measurements upto 30 GHz, thus confirming the accuracy of the proposed wave-dimensional modeling technique. This led to the first-time demonstration of ultra-low loss vertical interconnects in 50 µm thin glass substrates

The results and analysis of each of the above research tasks were documented and discussed in separate chapters within this dissertation. This chapter presents the summary of this dissertation with key contributions and identifies future research directions.

6.1 Research Summary:

6.1.1 High-frequency Electrical Modeling of Small-diameter TPVs at Fine-pitch in Ultra-thin glass:

A unique wave – dimensional analysis technique was proposed, to model the high frequency electrical behavior of the vertical through interconnects in 50 µm thin-glass core 3D interposer package. This approach, based on input impedance calculations, was used to accurately estimate the electrical parasitics of the TPVs including its resistance and inductance.
i) TPVs in glass, that is double-side laminated with low loss polymer, were modelled using 3D full wave EM solver (Ansys-HFSSTM). 3D full wave solver was chosen instead of circuit modeling techniques, to be able to incorporate the manufacturing and fabrication induced deviations. Also, EM field termination solutions were obtained for detailed electrical behavior analysis.

ii) Using the proposed modeling technique, the resistance and inductance of a TPV, with glass entry diameter of 60 µm and exit diameter of 56 µm were estimated to be 33 mΩ and 35 pH respectively, at a frequency of 10 GHz. Whereas in a 130 µm thin glass based 3D interposer, the resistance and inductance values were estimated to be 49 mΩ and 71 pH respectively.

iii) Also, the electrical parasitics were extracted for varying via diameters from 20 µm to 60 µm, in a 50 µm thin glass substrate. It was observed that the via parasitics decrease with increasing diameters. Based on this important result, larger via diameters are proposed for component integrations including filters, whereas smaller via diameters are preferable for integration with 50 Ω impedance matched TLs.

iv) Using the input impedance calculations, it was confirmed that the capacitance of the vias in 50 µm thin glass can be safely assumed to be negligible, owing to the high electrical resistivity of the glass substrate.

v) Further analysis on S-parameter modeling results of TLs terminated with TPVs, revealed that smaller via diameters exhibited reduced reflection losses at the TL-TPV interface, which was also confirmed through VSWR calculations. This is a significant milestone in achieving 2ML package interconnects with < 0.07 dB / mm insertion loss.
vi) Among the different parameters of via signaling, including the via pad and the aperture size, the latter played a dominant role in determining the resonance frequency and peak values.

6.1.2 Design Guidelines for Small- diameter vias at Fine – pitch in Ultra – thin glass:

The detailed electrical modeling of the smaller via diameters at fine pitch, in 50 µm thin glass substrates led to the following design rules. The proposed via dimensions and configurations satisfy the target of achieving less than 5% impedance discontinuity, reduced noise coupling and enhanced shorting efficiency.

v) Through-Glass-Vias could be represented as a series combination of resistance and inductance. The capacitance effect could be considered negligible due to the higher electrical resistivity of glass.

vi) The choice of optimal via diameter and the pitch, to achieve less than 5% impedance discontinuity with 50 Ω transmission lines, is dictated by the TPV’s inductive behavior. The modeling results suggest that smaller via diameters (~25 µm) at fine pitch (~ 50 µm) gives the near 50 Ω impedance for TPVs in a 50 µm thin glass core interposer. When integrated with transmission lines, the VSWR value was approximately equal to one, for a wide range of frequencies up to 50 GHz, indicating a perfect impedance match, leading to lesser delay and higher bandwidth.

vii) The resonance effect in TPVs integrated with transmission lines, can be greatly reduced by keeping the capture pad and the aperture size at its minimum, also considering its manufacturability. The high potentiality for smaller via capture pads and aperture sizes, is one of distinguishing advantages of glass vias as compared to its organic...
counterparts. This is enabled by the exceptional dimensional stability of the glass substrates.

viii) A via cage, with co-axial ground TPVs around the signal TPV, is one of the most efficient techniques for noise coupling reduction, in a high density, heterogeneous integrated system.

6.1.3 Ultra-thin Glass Handling and Metallization:

Lack of ease in the handling of thin glass panels was identified as one of the major challenges, in the demonstration of double – sided ultra- thin glass packages. This is attributed to the brittleness of the thin glass materials.

i) The first step in the systematic failure analysis consisted of identifying the locations of initial crack formations and their propagation in further fabrication steps. It was observed that the crack formation is prone to occur at the edges.

ii) Accordingly, an edge protection technique based on side-beading of polymers was proposed and demonstrated. The implementation details and the warpage analysis of the resultant stack-up were discussed in detail. The proposed approach is in the initial stages of development and needs further investigation to reduce the warpage and to adopt for large scale panel fabrication.

iii) RF text-fixtures with TPVs, were designed on a 50µm thick glass core laminated with low-loss polymer, to validate the 3D EM models. A via-first metallization technique named via – in – via is utilized, followed by semi-additive patterning, for achieving highly reliable metallization of through vias in thin glass substrates (50 µm). Further, the side wall of the metallized through-vias in ultra-thin glass is analyzed through optical imaging of via cross sections.
6.1.4 Electrical Characterization:

To validate the 3D EM models, the fabricated test fixtures were measured for high frequency electrical behavior, using a wafer probe based Vector Network Analyzer (VNA).

i) The high-frequency measurements of TPVs, in a 50 µm glass core package, were analyzed in-detail besides reporting precise model-measurement correlation up to 30 GHz. This precision is attributed to the high accuracy of the proposed TL based modeling technique and the Through, Reflect and Load (TRL) calibration process.

ii) It was observed that vias with smaller diameters exhibit better impedance match to the 50 Ω TLs and hence offer reduced reflection losses at the interfacial surface between TLs and TPVs. This establishes the rationale behind the need for smaller via diameters in 3D RF packages.

Hence, the proposed 3-D glass interposer approach with smaller diameter vias at fine-pitch, serves as a compelling alternative to contemporary approaches including organic and silicon interposers, for building high performance, low cost mixed signal systems. This is achieved by means of i) low substrate loss properties of glass core and epoxy build up polymer ii) high density TPVs in glass, with high quality metallization for thermo-mechanical reliability iii) small – diameter TPVs (~ 25 µm) for ultra-low loss package interconnection iv) Ample ground vias for power noise suppression at resonant frequencies, in a mixed signal system.

6.2 Key Contributions:

This research represents the first comprehensive study of the high frequency electrical modeling (20 – 60 µm) TPVs at fine pitch (50 – 150 µm), in ultra-thin glass substrates (50 µm). In addition, the following key engineering contributions are identified:
i) The high-frequency electrical benefits of ultra-fine TPVs at fine pitch in thin glass substrates were demonstrated for high-speed digital and mm wave applications, using 3D EM modeling and VNA measurements.

ii) The advantages of smaller-diameter TPVs in thin glass over the coarser TPVs in thicker glass substrates, in terms of processability, performance and cost aspects were duly identified.

iii) A unique and novel technique was proposed for accurate electrical characterization of TPV parasitics including its resistance, inductance and capacitance.

iv) An ultra-thin glass handling technique with polymer-laminated frame as an edge beading, was proposed and demonstrated.

v) Precise model – measurement correlation with less than 5% error was demonstrated with high-frequency electrical characterization of ultra-short TPVs.

The design metrics, targets and the key results obtained through this study, are summarized in Table 6.

<table>
<thead>
<tr>
<th>Design Metric</th>
<th>Objective</th>
<th>Result</th>
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| Insertion loss| < 0.08 dB/mm @ 28 GHz | Planar: 0.04 dB/mm  
Vertical: 0.28 dB/mm |
| VSWR          | <1.5 @ 28 GHz | 1.18 @ 28 GHz |
| Delay         | <5 ps @ 28 GHz | 0.32 ps for TPVs @ 28 GHz |

6.3 Future Extensions

This dissertation explored “50 µm ultra-thin glass” with Through Package Vias (TPVs) as a next-generation interposer and substrate technology, to meet the bandwidth, power and form-
factor requirements of emerging RF and 5G systems. The following studies are proposed as future extensions of this research:

a) **Electrical Modeling and Design:**

The electrical benefits of small – diameter vertical through-interconnections in TL – TPV signal transitions was clearly identified, supported with modeling and characterization results. However, double-side RF component integration demands larger vias for reduced resistance and inductance parasitics. Also, glass manufacturers prefer single via dimensions across the same panel in order increase the hole formation throughput and decrease the process defects. To address this manufacturing constraint, design innovations in the form of parallel via architectures with smaller diameters could be explored, to achieve the same electrical performance as of larger vias, in RF components integration. Capacitive coupling between the vias and the reference plane was ignored in this research but as the substrate thickness is further reduced, accurate estimation of capacitive coupling becomes critical.

b) **TPV Metallization and Reliability:**

The proposed handling technique for 50 µm thin glass could be enhanced to reduce the warpage for fine-line lithography. This technique is in the initial stages of development and needs further investigation to adopt for large-scale panel fabrication. The thermo-mechanical reliability of TPVs after board-level assembly is a major concern and therefore, a more detailed and exhaustive study on reliability and failure analysis of metallized TPVs can be undertaken after board-level assembly.
c) **Electrical Characterization:**

Microelectronic systems require the characterization of entire channel of signal transmission, including TPVs, RDLs and microvias. Hence, it is worthwhile to perform a detailed signal and power integrity analysis of the entire system interconnection. This would give a broader view of the impact of TPVs in the system performance. Further, the improvement in the performance of a functional 5G module with antennas and mm-wave ICs which utilizes the proposed design rules can be validated.

### 6.4 Journal and Conference Publications:

This work resulted in the following conference proceeding and peer reviewed journal publication:


REFERENCES


