MULTI-INPUT MULTI-OUTPUT (MIMO) DETECTION SYSTEMS

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References Cited
U.S. PATENT DOCUMENTS

“Low Complexity Fast Lattice Reduction Algorithm for MIMO Detection”, by Kanglian Zhao, Yang Li, Shuai Jiang. SID 2012 IEEE 23rd international symposium on personal, indoor and Mobile radio communications—(PIMRC)*

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ABSTRACT

Embodiments of the present invention provide efficient greedy LLL algorithms that not only converge faster but also exhibit much lower complexity than the existing greedy LLL variants while similar error performance is maintained. First, a relaxed Lovász condition is designed for searching the candidate set of LLL iterations with column swap operations. This relaxation does not need size reduction operations so that it can save complexity compared to the existing greedy LLL algorithms. Further, a relaxed criterion of the decrease in LLL potential is designed to select the optimal one in the candidate set of LLL iterations, which also exhibits lower complexity than the existing greedy LLL algorithms. Furthermore, simulations show that the inventive algorithm needs less LLL iterations compared to the existing greedy LLL algorithms.

18 Claims, 6 Drawing Sheets
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* cited by examiner
Fig. 1. BER performance comparisons of the different LR algorithms in dual-LR-aided MMSE and LR-aided MMSE-SIC detectors for $4 \times 4$ MIMO systems with 64-QAM.
Convergence comparisons of different LR algorithms in a 4 x 4 MIMO system.

Fig. 2
(a) Different LRs used for dual-IR-aided MMSE detectors.

(b) Different LRs used for LR-aided MMSE-SIC detectors.

Complexity comparisons of different LR algorithms from $3 \times 3$ to $8 \times 8$ MIMO systems.

Fig. 3
BER versus maximum number of LLL iterations of different LRs with early termination in a $4 \times 4$ MIMO system with 64-QAM.

Fig. 4
(a) Different LRAs used for dual-LR-aided MMSE detectors with Eb/N0=26.5dB.

(b) Different LRAs used for LR-aided MMSE-SIC detectors with Eb/N0=25.5dB.

Complexity versus maximum number of LLL iterations of different LRAs with early termination in a 4 x 4 MIMO system with 64-QAM.

Fig. 5
602 Receive transmit signal vectors

604 Generate channel matrix

606 Channel matrix QR decomposition (optionally other preprocessing)

608 Search candidate set of LLL iterations using relaxed condition

610 Select first selection from candidate set using relaxed criterion

612 Compare first selection to termination condition

614 Perform size reduction on matrices

616 Perform column swap on size reduced matrices

618 Search reduced matrix candidate set of LLL iterations using relaxed condition

620 Select next selection from candidate set using relaxed criterion

622 Compare next selection to termination condition

624 Generate reduced basis channel matrix

626 Provide reduced basis channel matrix to detector

628 Detect particular transmit signal vectors

630 Forward detected transmit signal vectors for processing

Fig. 6
MULTI-INPUT MULTI-OUTPUT (MIMO) DETECTION SYSTEMS

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to the following system model.

\[ y = Xs + n \]  

where \( y \) is an \( N \times 1 \) complex received signal vector, \( X \) is an \( N \times N \) complex channel matrix, \( s \) is an \( N \times 1 \) complex transmitted signal vector drawn from the QAM constellation set, whose real and imaginary parts are \( \{ \pm \sqrt{2}, \pm 1, \ldots, -1 \} \) with \( n \) being the constellation size, and \( w \) is the additive white Gaussian noise vector with zero mean and covariance matrix \( \sigma_n^2 I_N \). In the most general case, the invention is an improved complex lattice reduction (LR) technique used in the LR-aided detectors to find the near-optimal solution to (1).

2. Description of Related Art

Multi-input multi-output (MIMO) systems have been adopted in recent wireless standards (e.g., IEEE 802.11n/ac, 3GPP LTE/LTE-A) because of the high spectral efficiency and large coverage. The system model (1) can be applied to multi-input multi-output (MIMO) systems, generalized signal carrier frequency division multiple access (GSC-FDMA) system, and precoded FDMA (P-FDMA) system as special cases, with different realizations of the H matrix corresponding to different systems. To recover the signal vector \( s \) given the model (1), different detection methods can be adopted. The optimal detection is the maximum likelihood (ML) detector, but it exhibits exponential complexity. To alleviate the complexity of the ML detector, linear detectors (LDs), successive interference cancelation (SIC) detector, and K-best detector, have been proposed. However, these detectors degrade performance due to diversity loss. To obtain high error performance with low complexity in the detection of problem (1), lattice reduction (LR) techniques have been added to the existing LDs, SIC, and K-best detectors to collect full receive diversity.

LLL/ELL Algorithm

Among different LR schemes, LLL/ELL algorithm is a commonly adopted technique in LR-aided detectors. The detailed complex LLL algorithm based on QR preprocessing (the preprocessing part can also be sorted QR decomposition (SQRD) or MISE-SQRD to reduce LLL's complexity) can be found in Table I. The LLL/ELL iteratively performs three steps: 1) size reduction for LLL or effective size reduction for ELL (lines 4-10); 2) Lovász condition evaluation (line 11); and 3) column swap (lines 12-15) if the Lovász condition is not satisfied. The \( \frac{1}{2} \delta s_1 \) used in the LLL/ELL is a quality parameter selected to control the performance-complexity tradeoff (larger \( \delta \) leads to better performance with higher complexity).

BRIEF SUMMARY OF THE INVENTION

It is thus an intention of the present invention to design efficient greedy LLL algorithms that not only converge faster but also exhibit much lower complexity than the existing greedy LLL variants while the error performance is maintained. First, a relaxed Lovász condition for searching the candidate set of LLL iterations with column swap operations is designed. This relaxation does not need size reduction operations so that it can save complexity compared to the existing greedy LLL algorithms. Further, a relaxed criterion of the decrease in LLL potential is designed to select the optimal one in the candidate set of LLL iterations, which also exhibits lower complexity than the existing greedy LLL algorithms. Furthermore, simulations
show that the inventive algorithm needs less LLL iterations compared to the existing greedy LLL algorithms. Throughout the present application, we adopt the complex-valued versions for the LLL and different LLL variants.

In one embodiment, a method is provided comprising: receiving, at each one of a plurality of receiving sources, a plurality of transmit signal vectors, each of the plurality of transmit signal vectors originating from one of a plurality of transmitting sources; generating a channel matrix based on the received plurality of transmit signal vectors; decomposing the channel matrix to generate at least one alternate matrix; performing lattice reduction on the at least one alternate matrix to generate a transformed channel matrix comprising a reduced basis, the lattice reduction comprising: using a relaxed condition, searching a candidate set of LLL iterations with column swap operations in the at least one alternate matrix, wherein the relaxed condition provides for searching the candidate set of LLL iterations without performing size reduction operations on the at least one alternate matrix; using a relaxed criterion of decrease in LLL potential, selecting a first selection from the candidate set of LLL iterations; comparing the first selection to a predetermined termination condition; responsive to determining that the termination condition is not met, iteratively selecting a next selection from the candidate set of LLL iterations, each selection iteration comprising: performing a size reduction of the at least one alternate matrix to obtain at least one reduced matrix; performing a column swap on the at least one reduced matrix; using the relaxed condition, searching at the at least one reduced matrix for a candidate set of LLL iterations with column swap operations; using the relaxed criterion of decrease in LLL potential, determining the next selection from the candidate set of LLL iterations; and comparing the next selection to the termination condition. The method also comprises, responsive to determining that the termination condition is met, generating the reduced basis transformed channel matrix from the at least one alternate matrix; providing the reduced basis transformed channel matrix to a detector; and based on the reduced basis transformed channel matrix, detecting particular transmit signal vectors for processing.

In some embodiments, the method further comprises wherein the transmitting sources comprise transmitting antennas in a multiple-input, multiple-output system and the receiving sources comprise receiving antennas in a multiple-input, multiple-output system.

In some embodiments, the method further comprises wherein the relaxed condition for searching the candidate set of iterations comprises

$$\frac{[R_{k,d}]}{[R_{k-1,d}]} \leq \frac{1}{2}, \quad \forall k \in [2, N].$$

In some embodiments, the method further comprises wherein the relaxed criterion of decrease in LLL potential comprises

$$k = \arg \min_{k \in [2, N]} \frac{[R_{k,d}]}{[R_{k-1,d}]}.$$

In some embodiments, the method further comprises wherein the predetermined termination condition comprises $n_{d} \times 1/\sqrt{2}$. In some embodiments, the method further comprises wherein the predetermined termination condition further comprises an iteration count being less than a predefined maximum count.

In some embodiments, the method further comprises wherein the relaxed condition for searching the candidate set of iterations comprises $\forall k \in 2, N]$. In some embodiments, the method further comprises wherein the relaxed criterion of decrease in LLL potential comprises

$$k = \begin{cases} \arg \min_{k \in [2, N]} \frac{[R_{k,d}]}{[R_{k-1,d}]} & \text{if Dual-LR-aided LD} \\ \arg \min_{k \in [2, N]} \frac{[R_{k,d}]}{[R_{k-1,d}]} & \text{if LR-aided SIC/K-best} \end{cases}$$

In some embodiments, the method further comprises wherein the predetermined termination condition comprises $\forall k \in 2, N]$. In some embodiments, the method further comprises wherein the predetermined termination condition further comprises an iteration count being less than a predefined maximum count.

In another embodiment, a transmission system is provided comprising: a plurality of transmitting antennas; a plurality of receiving antennas; and an apparatus comprising: at least one processor; and at least one memory comprising computer program instructions, the computer program instructions when executed by the at least one processor, causing the apparatus to: receive, at each one of the plurality of receiving antennas, a plurality of transmit signal vectors, each of the plurality of transmit signal vectors originating from one of the plurality of transmitting antennas; generate a channel matrix based on the received plurality of transmit signal vectors; decompose the channel matrix to generate at least one alternate matrix; perform lattice reduction on the at least one alternate matrix to generate a transformed channel matrix comprising a reduced basis, the lattice reduction comprising: using a relaxed condition, searching a candidate set of LLL iterations with column swap operations in the at least one alternate matrix, wherein the relaxed condition provides for searching the candidate set of LLL iterations without performing size reduction operations on the at least one alternate matrix; using a relaxed criterion of decrease in LLL potential; generating the reduced basis transformed channel matrix from the at least one alternate matrix; providing the reduced basis transformed channel matrix to a detector; and based on the reduced basis transformed channel matrix, detecting particular transmit signal vectors for processing.

In some embodiments, the method further comprises wherein the transmitting sources comprise transmitting antennas in a multiple-input, multiple-output system and the receiving sources comprise receiving antennas in a multiple-input, multiple-output system. In some embodiments, the method further comprises wherein the predetermined termination condition comprises $n_{d} \times 1/\sqrt{2}$. In some embodiments, the method further comprises wherein the predetermined termination condition further comprises an iteration count being less than a predefined maximum count.
receiving antennas comprise receiving antennas in a multiple-input, multiple-output system.

In some embodiments, the system further comprises wherein the relaxed condition for searching the candidate set of iterations comprises

$$\frac{|\hat{R}_{k,\ell}|}{|\hat{R}_{k,\ell-1}|} \leq \frac{1}{\sqrt{2}}, \quad \forall \ k \in [2, N_k].$$

In some embodiments, the system further comprises wherein the relaxed criterion of decrease in LLL potential comprises

$$k = \arg\min_{0 < k \leq N} \frac{|\hat{R}_{k,\ell}|}{|\hat{R}_{k-1,\ell-1}|}.$$

In some embodiments, the system further comprises wherein the predetermined termination condition comprises $n_{\text{const}} = 1/\sqrt{2}$. In some embodiments, the system further comprises wherein the predetermined termination condition further comprises an iteration count being less than a predefined maximum count.

In some embodiments, the system further comprises wherein the relaxed condition for searching the candidate set of iterations comprises $\forall k \in [2, N_k]$. In some embodiments, the system further comprises wherein the relaxed criterion of decrease in LLL potential comprises

$$k = \left\{ \begin{array}{ll}
\arg\min_{0 \leq k < N_{\text{const}}(\phi)} & \text{if Dual-LR-aided LD} \\
\arg\min_{0 \leq k < N_{\text{const}}(\phi)} & \text{if LR-aided SIC-K-best}
\end{array} \right.$$  

In some embodiments, the system further comprises wherein the predetermined termination condition comprises $\forall k \in [2, N_k]$.

These and other objects, features and advantages of the present invention will become more apparent upon reading the following specification in conjunction with the accompanying drawing figures.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 depicts the uncoded BER performance of different LR algorithms in dual LR-aided MMSM-SIC and LR-aided MMSM-SIC detectors for a 4x4 MIMO system with 64-QAM.

FIG. 2 illustrates the convergence of different LR algorithms by the complementary cumulative distribution function (CCDF) of the number of LLL iterations.

FIG. 3 depicts the complexity of different LR algorithms from 3x3 to 8x8 MIMO systems by average equivalent real floating-point operations (flops).

FIG. 4 depicts the results of BER of different LR algorithms with early termination.

FIG. 5 depicts the results of complexity of different LR algorithms with early termination.

FIG. 6 provides a flowchart of exemplary operations according to an example embodiment of the present invention.

DETAIL DESCRIPTION OF THE INVENTION

To facilitate an understanding of the principles and features of the various embodiments of the invention, various illustrative embodiments are explained below. Although exemplary embodiments of the invention are explained in detail, it is to be understood that other embodiments are contemplated. Accordingly, it is not intended that the invention is limited in its scope to the details of construction and arrangement of components set forth in the following description or illustrated in the drawings. The invention is capable of other embodiments and of being practiced or carried out in various ways. Also, in describing the exemplary embodiments, specific terminology will be resorted to for the sake of clarity.

It must also be noted that, as used in the specification and the appended claims, the singular forms "a," "an" and "the" include plural references unless the context clearly dictates otherwise. For example, reference to a component intended also to include a composition of a plurality of components. References to a composition containing "a" constituent is intended to include other constituents in addition to the one named.

Also, in describing the exemplary embodiments, terminology will be resorted to for the sake of clarity. It is intended that each term contemplates its broadest meaning as understood by those skilled in the art and includes all technical equivalents which operate in a similar manner to accomplish a similar purpose.

Ranges may be expressed herein as from "about" or "approximately" or "substantially" one particular value and/or to "about" or "approximately" or "substantially" another particular value. When such a range is expressed, other exemplary embodiments include from the one particular value and/or to the other particular value.

Similarly, as used herein, "substantially free" of something, or "substantially pure," and like characterizations, can include both being "at least substantially free" of something, or "at least substantially pure," and being "completely free" of something, or "completely pure".

By "comprising" or "containing" or "including" is meant that at least the named compound, element, particle, or method step is present in the composition or article or method, but does not exclude the presence of other compounds, materials, particles, method steps, even if the other such compounds, material, particles, method steps have the same function as what is named.

It is also to be understood that the mention of one or more method steps does not preclude the presence of additional method steps or intervening method steps between those steps expressly identified. Similarly, it is also to be understood that the mention of one or more components in a composition does not preclude the presence of additional components than those expressly identified.

The materials described as making up the various elements of the invention are intended to be illustrative and not restrictive. Many suitable materials that would perform the same or a similar function as the materials described herein are intended to be embraced within the scope of the invention. Such other materials not described herein can include, but are not limited to, for example, materials that are developed after the time of the development of the invention.

With regard to notations as used herein, boldface upper- and lower-case letters represent matrices and column vectors, respectively. $A_{ij}$ denotes the (i, j)th entry of matrix A. $A_{a,b,c,d}$ indicates a submatrix of A including entries from
rows a to b and from columns c to d. If only : is used, this corresponds to entries in a complete row or column. Index notation expressed as n: is an integer.

Various aspects of the complex number are represented as $\Re[\cdot]$ and $\Im[\cdot]$, and $\sqrt{-1}$. [a] indicates rounding to the nearest integer of a.

In some instances, a computing device may be referred to as a mobile device, mobile computing device, a mobile station (MS), terminal, cellular phone, cellular handset, personal digital assistant (PDA), smart phone, wireless phone, organizer, handheld computer, desktop computer, laptop, computer, tablet computer, set-top box, television, appliance, game device, medical device, display device, or some other like terminology. In other instances, a computing device may be a processor, controller, or a central processing unit (CPU). In yet other instances, a computing device may be a set of hardware components.

Various aspects described herein may be implemented using standard programming or engineering techniques to produce software, firmware, hardware, or any combination thereof to control a computing device to implement the disclosed subject matter. A computer-readable medium may include, for example: a magnetic storage device such as a hard disk, a floppy disk or a magnetic strip, an optical storage device such as a compact disk (CD) or digital versatile disk (DVD); a smart card; and a flash memory device such as a card, stick or key drive, or embedded component. Additionally, it should be appreciated that a carrier wave may be employed to convey computer-readable electronic data including those used in transmitting and receiving electronic data such as electronic mail (e-mail) or in accessing a computer network such as the Internet or a local area network (LAN). Of course, a person of ordinary skill in the art will recognize many modifications may be made to this configuration without departing from the scope or spirit of the claimed subject matter.

It will be understood by those of skill in the art that the present invention may incorporate various types computing device architectures. They may be embodied in a computing device (for example, a dedicated server computer or a mobile computing device). It will be understood that the computing device architecture is provided for example purposes only and does not limit the scope of the various embodiments of the present disclosed systems, methods, and computer-readable mediums.

The computing device architecture may include a CPU, where computer instructions are processed; a display interface that acts as a communication interface and provides functions for rendering video, graphics, images, and text on the display. According to certain some embodiments of the disclosed technology, the display interface may be directly connected to a local display, such as a touch-screen display associated with a mobile computing device. In another example embodiment, the display interface may be configured for providing data, images, and other information for an external/remote display that is not necessarily physically connected to the mobile computing device. For example, a desktop monitor may be utilized for mirroring graphics and other information that is presented on a mobile computing device. According to certain some embodiments, the display interface may wirelessly communicate, for example, via a Wi-Fi channel or other available network connection interface to the external/remote display.

In an example embodiment, the network connection interface may be configured as a communication interface and may provide functions for rendering video, graphics, images, text, other information, or any combination thereof on the display. In one example, a communication interface may include a serial port, a parallel port, a general purpose input and output (GPIO) port, a game port, a universal serial bus (USB), a micro-USB port, a high definition multimedia (HDMI) port, a video port, an audio port, a Bluetooth port, a near-field communication (NFC) port, another like communication interface, or any combination thereof.

The computing device architecture may include a keyboard interface that provides a communication interface to a keyboard. The computing device architecture may be configured to use an input device via one or more of input/output interfaces (for example, the keyboard interface, the display interface, the presence sensitive display interface, network connection interface, camera interface, sound interface, etc.) to allow a user to capture information into the computing device architecture. The input device may include a mouse, a trackball, a directional pad, a trackpad, a touch-verifiable track pad, a presence-sensitive track pad, a presence-sensitive display, a scroll wheel, a digital camera, a digital video camera, a web camera, a microphone, a sensor, a smartcard, and the like. Additionally, the input device may be integrated with the computing device architecture or may be a separate device. For example, the input device may be an accelerometer, a magnetometer, a digital camera, a microphone, and an optical sensor.

Example embodiments of the computing device architecture may include an audio interface that provides a communication interface to an audio interface network connection interface that provides a communication interface to a network. According to certain embodiments, a camera interface is provided that acts as a communication interface and provides functions for capturing digital images from a camera or other image/video capture device. According to certain embodiments, a sound interface is provided as a communication interface for converting sound into electrical signals using a microphone and for converting electrical signals into sound using a speaker. According to example embodiments, a random access memory (RAM) is provided, where computer instructions and data may be stored in a volatile memory device for processing by the CPU.

According to an example embodiment, the computing device architecture includes a read-only memory (ROM) where invariant low-level system code or data for basic system functions such as basic input and output (I/O) startup, or reception of keystrokes from a keyboard are stored in a non-volatile memory device. According to an example embodiment, the computing device architecture includes a storage device or other suitable type of memory (e.g., RAM, ROM, programmable read-only memory (PRROM), electrically programmable read-only memory (EPROM), electrically erasable programmable read-only memory (EEPROM), magnetic disks, optical disks, floppy disks, hard disks, removable cartridges, flash drives), where the files include an operating system, application programs (including, for example, a web browser application, a widget or gadget engine, and other applications, as necessary) and data files are stored. According to an example embodiment, the computing device architecture includes a power source that provides an appropriate alternating current (AC) or direct current (DC) to power components. According to
an example embodiment, the computing device architecture includes a telephony subsystem that allows the device to transmit and receive sound over a telephone network. The constituent devices and the CPU communicate with each other over a bus.

According to an example embodiment, the CPU has appropriate structure to be a computer processor. In one arrangement, the CPU may include more than one processing unit. The RAM interfaces with the computer bus to provide quick RAM storage to the CPU during the execution of software programs such as the operating system application programs, and device drivers. More specifically, the CPU loads computer-executable process steps from the storage medium or other media into a field of the RAM in order to execute software programs. Data may be stored in the RAM, where the data may be accessed by the computer CPU during execution. In one example configuration, the device architecture includes at least 125 MB of RAM, and 256 MB of flash memory.

The storage medium itself may include a number of physical drive units, such as a redundant array of independent disks (RAID), a floppy disk drive, a flash memory, a USB flash drive, an external hard disk drive, thumb drive, pen drive, key drive, a High-Density Digital Versatile Disc (HD-DVD) optical disc drive, an internal hard disk drive, a Blu-Ray optical disc drive, or a Holographic Digital Data Storage (HDDS) optical disc drive, an external micro-dual in-line memory module (DIMM) synchronous dynamic random access memory (SDRAM), or an external micro-DIMM SDRAM. Such computer readable storage media allow a computing device to access computer-executable process steps, application programs and the like, stored on removable and non-removable memory media, to off-load data from the device or to upload data onto the device. A computer program product, such as one utilizing a communication system may be embodied in storage medium, which may comprise a machine-readable storage medium.

According to one example embodiment, the term computing device, as used herein, may be a CPU, or conceptualized as a CPU (for example, the CPU). In this example embodiment, the computing device may be coupled, connected, or in communication with one or more peripheral devices, such as display, camera, speaker, or microphone.

In some embodiments of the disclosed technology, the computing device may include any number of hardware or software applications that are executed to facilitate any of the operations. In some embodiments, one or more I/O interfaces may facilitate communication between the computing device and one or more input/output devices. For example, a universal serial bus port, a serial port, a disk drive, a CD-ROM drive, or one or more user interface devices, such as a display, keyboard, keypad, mouse, control panel, touch screen display, microphone, etc., may facilitate user interaction with the computing device. The one or more I/O interfaces may be utilized to receive or collect data and/or user instructions from a wide variety of input devices. Received data may be processed by one or more computer processors as desired in various embodiments of the disclosed technology and/or stored in one or more memory devices.

One or more network interfaces may facilitate connection of the computing device inputs and outputs to one or more suitable networks or connections; for example, the connections that facilitate communication with any number of sensors associated with the system. The one or more network interfaces may further facilitate connection to one or more suitable networks; for example, a local area network, a wide area network, the Internet, a cellular network, a radio-frequency network, a Bluetooth-enabled network, a Wi-Fi-enabled network, a satellite-based network, any wired network, any wireless network, etc., for communication with external devices or systems.

Embodiments of the present invention generally relate to the following system model

\[ y = Hx + w, \]

where \( y \) is an \( N_x \times 1 \) complex received signal vector, \( H \) is an \( N_x \times N_c \) complex channel matrix, \( x \) is an \( N_c \times 1 \) complex transmitted signal vector drawn from the QAM constellation set, whose real and imaginary parts are \( \{-\sqrt{3}/2, 1, \ldots, -1, 1, \ldots, \sqrt{3}/2\} \) with \( x \) being the constellation size, and \( w \) is the additive white Gaussian noise vector with zero mean and covariance matrix \( \sigma_w I_N \). We assume that \( H \) is known at the receiving side but unknown at the transmitting side.

A primary goal of the invention is to design greedy IIL algorithms with further improved convergence and decreased complexity while keeping similar error performance in LR-aided detectors compared to the existing greedy ILL algorithms.

Greedy ILL Algorithm-I

Two designs are proposed to implement the greedy ILL algorithm-I according to embodiments of the present invention.

First, a relaxed Lovász condition for searching the candidate set of IIL iterations with column swap operations is proposed as

\[
\frac{|R_{k, \ldots, k-1}|}{|R_{k, \ldots, k-1}|} \geq \frac{1}{\sqrt{2}}, \quad \forall k \in [1, N_c].
\]

Since this relaxed Lovász condition does not involve the off-diagonal elements in \( R \), its evaluation does not need size reduction operations so that it can save complexity compared to the existing greedy ILL algorithms.

Second, a relaxed criterion of the decrease in IIL potential to select the optimal one in the candidate set of IIL iterations is proposed as

\[
k = \arg \min_{2 \leq k \leq N_c} \frac{|R_{k, \ldots, k-1}|}{|R_{k, \ldots, k-1}|},
\]

which also exhibits lower complexity than that of the existing greedy ILL algorithms. Besides, its main calculation part is the same as the aforementioned relaxed Lovász condition in (2), which can be denoted as

\[
\eta_k = \frac{|R_{k, \ldots, k-1}|}{|R_{k, \ldots, k-1}|}, \quad 2 \leq k \leq N_c.
\]

Since \( \eta_k \) depends on the diagonal elements of \( R \), and the IIL iteration at index \( k \) affects the diagonal elements \( R_{k, k} \) and \( R_{k, k-1} \), we only need to update \( \eta_k \) if \( k > 1 \), \( \eta_1 \), and \( \eta_{k+1} \) if \( k < N_c \) after the first IIL iteration instead of calculating all \( \eta_k \) each time.

Based on the aforementioned two relaxations, the proposed greedy ILL algorithm-I is summarized in Table II. In the table, lines 2-5 are the initial evaluation of the proposed
selection method of LLL iterations and lines 10-13 correspond to the updates of \( \eta_l \) and the next selection of LLL iteration. Line 7 is the condition to determine whether the algorithm is terminated or not. In line 7, besides the relaxed Lovász condition, the early termination is also adopted to set a predefined maximum iteration number as \( N_{\text{max}} \) (N_{\text{max}} = \infty if there is no early termination). Note that for size reduction in Table II, we adopt the effective size reduction (line 8) as in ELLL plus the delayed full size reduction (DFSR, lines 16-18) as in PLLLL-OSSC. And in the LR-aided SIC/K-best detectors, the DF SR part can be dropped without affecting the error performance.

### Table II: Proposed Greedy LLL Algorithm-I

<table>
<thead>
<tr>
<th>Input: ( Q, R, P ) (after QR/SQRD/MMSE-SQRD)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output: ( Q, R, T )</td>
</tr>
<tr>
<td>1. Initialize: ( Q = Q, \hat{R} = R, T = P, N_{\text{max}} )</td>
</tr>
<tr>
<td>2. for ( i = 2 ): ( N_i )</td>
</tr>
<tr>
<td>3. ( \eta_i =</td>
</tr>
<tr>
<td>4. end</td>
</tr>
<tr>
<td>5. ( k = \arg \min_{k=2,\ldots,N_i} \eta_i )</td>
</tr>
<tr>
<td>6. ( \eta_{\text{new}} = 0 )</td>
</tr>
<tr>
<td>7. while ( \eta_k &lt; 1 \sqrt{2} ) &amp; &amp; ( \eta_{\text{new}} &lt; N_{\text{max}} )</td>
</tr>
<tr>
<td>8. Execute effective size reduction (lines 4-10 of Table I)</td>
</tr>
<tr>
<td>9. Execute column swap (lines 12-15 of Table I)</td>
</tr>
<tr>
<td>10. for ( i = {k, k + 1} \cap {2, N_i} )</td>
</tr>
<tr>
<td>11. ( \eta_i =</td>
</tr>
<tr>
<td>12. end</td>
</tr>
<tr>
<td>13. ( k = \arg \min_{k=2,\ldots,N_i} \eta_k )</td>
</tr>
<tr>
<td>14. ( \eta_{\text{new}} = \eta_k + 1 )</td>
</tr>
<tr>
<td>15. end</td>
</tr>
<tr>
<td>16. Use k = 2 : ( N_i )</td>
</tr>
<tr>
<td>17. Execute size reduction (lines 4-10 of Table I)</td>
</tr>
<tr>
<td>18. end</td>
</tr>
</tbody>
</table>

*Lines 16-18 can be dropped for LR-aided SIC/K-best detectors.*

### Greedy LLL Algorithm-II

Two designs are proposed to implement the greedy LLL algorithm-II according to embodiments of the present invention.

First, a relaxed Lovász condition for searching the candidate set of LLL iterations with column swap operations is proposed as

\[
\sqrt{2} |\hat{R}_k / \hat{R}_{k-1}|, \quad \forall k \in [2, N] \tag{5}
\]

Compared with the relaxed Lovász condition in (2) of the greedy LLL algorithm-I, the relaxed Lovász condition in (5) exhibits an equivalent form with less complexity since it does not need the division operation.

Second, the criterion to select the optimal one in the candidate set of LLL iterations is proposed based on the detection type as

\[
k = \begin{cases} 
\arg \min_{k=1,\ldots,N_i} \eta_k & \text{if Dual-LR-aided LD} \\
\arg \min_{k=1,\ldots,N_i} \eta_k & \text{if LR-aided SIC/K-best} 
\end{cases} \tag{6}
\]

where \( \eta_k = |\sqrt{2} R_k / \sqrt{2} R_{k-1}| \) indicate whether the relaxed Lovász condition is satisfied or not. Equation (6) means that the selection of the optimal LLL candidate each time is either the maximum value or minimum value of the column index \( k \) in the candidate set of LLL iterations.

Based on the aforementioned discussion, we summarize the proposed greedy LLL algorithm-II in Table III. In this table, the main computational parts, i.e., the effective size reduction, the column swap, and the DFSR, are the same as the greedy LLL algorithm-I in Table II. Here, the relaxed Lovász condition (lines 2-4) is expressed in an equivalent form as (2) but without division operation, so it is more suitable for high speed hardware implementation. Another difference compared to the greedy LLL algorithm-I is the selection method of LLL iterations (line 7) which is optimized corresponding to the error performance of specific LR-aided detectors.

### Table III: Proposed Greedy LLL Algorithm-II

<table>
<thead>
<tr>
<th>Input: ( Q, R, P ) (after QR/SQRD/MMSE-SQRD)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output: ( Q, R, T )</td>
</tr>
<tr>
<td>1. Initialize: ( Q = Q, \hat{R} = R, T = P, \text{flag} = \text{zeros} (1, N_i), N_{\text{max}} )</td>
</tr>
<tr>
<td>2. for ( i = 2 ): ( N_i )</td>
</tr>
<tr>
<td>3. ( \text{flag}(i) = (\sqrt{2}</td>
</tr>
<tr>
<td>4. end</td>
</tr>
<tr>
<td>5. ( \eta_{\text{new}} = 0 )</td>
</tr>
<tr>
<td>6. while (\text{sum(flag) = 0} &amp; &amp; \eta_{\text{new}} &lt; N_{\text{max}})</td>
</tr>
<tr>
<td>7. ( k = \arg \min_{k=2,\ldots,N_i} \eta_k )</td>
</tr>
<tr>
<td>8. Execute effective size reduction (lines 4-10 of Table I)</td>
</tr>
<tr>
<td>9. Execute column swap (lines 12-15 of Table I)</td>
</tr>
<tr>
<td>10. for ( i = {k, k + 1} \cap {2, N_i} )</td>
</tr>
<tr>
<td>11. ( \text{flag}(i) = (\sqrt{2}</td>
</tr>
<tr>
<td>12. end</td>
</tr>
<tr>
<td>13. ( \eta_{\text{new}} = \eta_k + 1 )</td>
</tr>
<tr>
<td>14. end</td>
</tr>
<tr>
<td>15. ( \text{Execute delayed full size reduction (lines 16-18 of Table II)} )</td>
</tr>
</tbody>
</table>

Line 15 can be dropped for LR-aided SIC/K-best detectors.

**FIG. I** depicts the uncoded BER performance of different LR algorithms in dual-LR-aided MMSE-SIC and LR-aided MMSE-SIC detectors for a 4x4 MIMO system with 64-QAM. To make fair comparison, we use the LRIs with full size reduction in the dual-LR-aided MMSE detector, i.e., LLL, PLLLL-OSSC, GDR+DFSR (adding DFSR in the end of GDR), and the proposed greedy LLL algorithm-I/II, while we adopt the LRIs with only effective size reduction in the LR-aided MMSE-SIC detector, i.e., ELLL, PLLLL-OSSC without DFSR, GDR, and the proposed greedy LLL algorithm-I/II without DFSR. It can be seen that all LR algorithms have almost the same BER performance in either the dual-LR-aided MMSE-SIC detector or the LR-aided MMSE-SIC detector, which indicates that the proposed two greedy LLL algorithms exhibit almost no performance loss compared with the LLL/PSLLL-OSSC/GDR algorithm.

**FIG. II** illustrates the convergence of different LRs by the complementary cumulative distribution function (CCDF) of the number of LLL iterations. One LLL iteration is defined as one-time execution of (effective) size reduction, (relaxed) Lovász condition evaluation, and (possible) column swap in the LLL algorithm or its variants. First, the LRs with 5-1 need more LLL iterations than those with 6-0.75 in LLL, PLLLL-OSSC, and GDR algorithms. Second, the PLLLL-OSSC/GDR converges much faster than LLL due to the greedy characteristic. Finally, the proposed greedy LLL algorithm-I/II can further improve the convergence compared to PSLLL-OSSC/GDR algorithms.

**FIG. III** depicts the complexity of different LRs from 3 x3 to 8 x 8 MIMO systems by average equivalent real floating-point operations (flops). First, for each LR scheme of LLL, PLLLL-OSSC, and GDR, the version with 5-1 exhibits higher complexity than the version with 6-0.75. Second, the PLLLL-OSSC has a little higher complexity than the GDR and LLL algorithms. Finally, the proposed greedy LLL
algorithms achieves the lowest complexity in both dual-LR-aided MMSE-SIC and LR-aided MMSE-SIC detectors.

FIG. 4 and FIG. 5 depict the results of BER and complexity of different LR algorithms with early termination, i.e., N_{max} = 6, which is usually the case in practical hardware.

First, FIG. 4 demonstrates the convergence of different LR algorithms in terms of BER versus maximum number of LLI iterations N_{max}, where the Eb/No values are selected such that the BER of the LLI with N_{max} = 6 (without early termination) can achieve around 10^{-3}. It can be seen that the LLI algorithm exhibits much slower convergence than all greedy LLI algorithms in all cases while the proposed two greedy LLI algorithms have almost the same convergence as the PS-LLL-OSCC/GDR in both dual-LR-aided MMSE detector and the LR-aided MMSE-SIC detector. All the greedy LLI's need only N_{max} = 6 LLI iterations to approach the best performance.

Second, FIG. 5 shows the complexity of different LR algorithms in terms of average number of flops versus N_{max}, where the values of Eb/No are selected the same as those in the FIG. 4. It can be seen that the complexity of each LR remains stable after some N_{max} LLI iterations. Based on the final stable complexities, the proposed two greedy LLI algorithms enable the smallest complexity. When only considering the N_{max} = 6, the proposed two greedy LLI algorithms still have the lowest complexity while maintaining the best error performance as shown in FIG. 4.

FIG. 6 provides a flowchart of exemplary operations for lattice reduction according to an example embodiment of the present invention. At block 602, a plurality of receiving antennas of a transmission system (for example, a MIMO system) each receive a plurality of transmit signal vectors with each transmit signal vector originating from one of a plurality of transmitting antennas. For example, the plurality of transmit signal vectors from a transmitting antenna may be due to multipath effects.

At block 604, a channel matrix is generated based on the plurality of transmit signal vectors received by the receiving antennas (e.g., the complex received signal vectors). At block 606, decomposition is applied to the channel matrix to generate at least one alternate matrix. For example, QR decomposition may be used to generate Q and R matrices from the complex channel matrix H.

Lattice reduction to generate a transformed channel matrix comprising a reduced basis is then performed. At block 608, a relaxed Lovász condition is used to search a candidate set of Lenstra-Lenstra-Lovász (LLL) iterations with column swap operations using the R matrix. This evaluation using the relaxed Lovász condition does not need size reduction operations, reducing complexity compared to other greedy LLI algorithms (size reduction is only used inside the next LLI iteration after the searching stage). At block 610, a relaxed criterion of decrease in LLI potential is used in selecting a first selection from the candidate set of LLI iterations with column swap operations.

At block 612, the first selection from the candidate set of LLI iterations is compared to a predetermined termination condition to determine whether the greedy LLI algorithm should be terminated or not. Embodiments may also provide for a pre-defined maximum number of LLI iterations that may be undertaken before the greedy LLI algorithm is terminated. If, at block 612, it is determined that the greedy LLI algorithm should not be terminated (the termination condition is not met, 612-NO), an iterative process of selecting the next LLI iteration from the candidate set is started. If, at block 612, it is determined that the greedy LLI algorithm should be terminated (the termination condition is met, 612-YES), operations continue to block 624.

At block 614, size reduction is performed on the alternate matrixes. At block 616, column swapping is performed on the reduced alternate matrixes (for example, k-1 and k may be swapped in the R and R matrixes. At block 618, the relaxed Lovász condition is used to search a candidate set of Lenstra-Lenstra-Lovász (LLL) iterations with column swap operations using the alternate matrix modified at blocks 614 and 616. At block 620, the relaxed criterion of decrease in LLI potential to determine (select) the next selection from the candidate set of LLI iterations. At block 622, the next selection from the candidate set of LLI iterations is compared to the predetermined termination condition to determine whether the greedy LLI algorithm should be terminated or not. If, at block 622, it is determined that the greedy LLI algorithm should not be terminated (the termination condition is not met), 622-NO), the iterative process of selecting the next LLI iteration from the candidate set is continued by returning to block 614. If, at block 622, it is determined that the greedy LLI algorithm should be terminated (the termination condition is met, 622-YES), the lattice reduction is complete and operations continue to block 624. A t block 624, the reduced basis channel matrix is generated based on the alternate matrixes.

At block 626, the reduced basis channel matrix may be provided to a detector (for example, an LR-aided detectors such as LR-aided SIC and K-best detectors). At block 628, the LR-aided detector may detect particular transmitted signal vectors from each transmitting antenna. At block 630, the detected transmitted signal vectors may be forwarded for further processes in the transmission system.

Numerous characteristics and advantages have been set forth in the foregoing description, together with details of structure and function. While the invention has been described in several forms, it will be apparent to those skilled in the art that many modifications, additions, and deletions, especially in matters of shape, size, and arrangement of parts, can be made therein without departing from the spirit and scope of the invention and its equivalents as set forth in the following claims. Therefore, other modifications or embodiments as may be suggested by the teachings herein are particularly reserved as they fall within the breadth and scope of the claims here appended.

What is claimed is:
1. A method comprising:
   - receiving, at each one of a plurality of receiving sources, a plurality of transmit signal vectors, each of the plurality of transmit signal vectors originating from one of a plurality of transmitting sources;
   - generating a channel matrix based on the received plurality of transmit signal vectors;
   - decomposing the channel matrix to generate at least one alternate matrix;
   - performing lattice reduction on the at least one alternate matrix to generate a transformed channel matrix comprising a reduced basis, the lattice reduction comprising:
     - using a relaxed condition, searching a candidate set of Lenstra-Lenstra-Lovász (LLL) iterations with column swap operations in the at least one alternate matrix, wherein the relaxed condition provides for searching the candidate set of LLI iterations without performing size reduction operations on at least one alternate matrix;
using a relaxed criterion of decrease in LLL potential, wherein the relaxed criterion of decrease in LLL potential comprises

\[ k = \arg \min_{k \leq \lfloor \sqrt{N_c} \rfloor} \frac{|\mathbf{R}_{k,k}|}{|\mathbf{R}_{k-1,k-1}|}, \]

selecting a first selection from the candidate set of LLL iterations, wherein \( |\mathbf{R}_{k,k}| \) indicates the absolute value of

\[ \mathbf{R}_{k,k}, \text{ and } \arg \min_{k \leq \lfloor \sqrt{N_c} \rfloor} \frac{|\mathbf{R}_{k,k}|}{|\mathbf{R}_{k-1,k-1}|} \]

indicates finding the \( k \) value in the range of \( 2, 3, \ldots, N_c \) that corresponds to a minimum value in

\[ \frac{|\mathbf{R}_{k,k}|}{|\mathbf{R}_{k-1,k-1}|}; \]

comparing the first selection to a predetermined termination condition;

responsive to determining that the termination condition is not met, iteratively selecting a next selection from the candidate set of LLL iterations, each selection iteration comprising:

performing a size reduction of the at least one alternate matrix to obtain at least one reduced matrix;

performing a column swap on the at least one reduced matrix;

using the relaxed condition, searching the at least one reduced matrix for a candidate set of LLL iterations with column swap operations;

using the relaxed criterion of decrease in LLL potential, determining the next selection from the candidate set of LLL iterations; and

comparing the next selection to the termination condition;

responsive to determining that the termination condition is met, generating the reduced basis transformed channel matrix from the at least one alternate matrix;

providing the reduced basis transformed channel matrix to a detector; and

based on the reduced basis transformed channel matrix, detecting particular transmit signal vectors for processing.

2. The method of claim 1, wherein the transmitting sources comprise transmitting antennas in a multiple-input, multiple-output system and the receiving sources comprise receiving antennas in a multiple-input, multiple-output system.

3. The method of claim 1, wherein the relaxed condition for searching the candidate set of iterations comprises

\[ \frac{|\mathbf{R}_{k,k}|}{|\mathbf{R}_{k-1,k-1}|} \leq \frac{1}{\sqrt{2}}, \forall k \in [2, N_c], \]

wherein \( \mathbf{R}_{k,k} \) indicates each \( k \) value in the range of \( 2, 3, \ldots, N_c \).

4. The method of claim 1, wherein the predetermined termination condition comprises \( \eta_{k,2} = 1/\sqrt{2} \), wherein \( \eta_{k} \) is defined as

\[ \eta_{k} = \frac{|\mathbf{R}_{k,k}|}{|\mathbf{R}_{k-1,k-1}|}, \]

\( \forall k \subseteq [2, N_c] \).

5. The method of claim 4, wherein the predetermined termination condition further comprises an iteration count being less than a predefined maximum count.

6. The method of claim 1, wherein the relaxed condition for searching the candidate set of iterations comprises \( \sqrt{2}|\mathbf{R}_{k,k}| \leq |\mathbf{R}_{k-1,k-1}| \), \( \forall k \subseteq [2, N_c] \), wherein the value of \( (\sqrt{2}|\mathbf{R}_{k,k}| < |\mathbf{R}_{k-1,k-1}|) \) is 1 if \( \sqrt{2}|\mathbf{R}_{k,k}| \) is less than \( |\mathbf{R}_{k-1,k-1}| \), otherwise, the value of \( (\sqrt{2}|\mathbf{R}_{k,k}| < |\mathbf{R}_{k-1,k-1}|) \) is 0.

7. A method comprising:

receiving, at each one of a plurality of receiving sources, a plurality of transmit signal vectors, each of the plurality of transmit signal vectors originating from one of a plurality of transmitting sources;

generating a channel matrix based on the received plurality of transmit signal vectors;

decomposing the channel matrix to generate at least one alternate matrix;

performing lattice reduction on the at least one alternate matrix to generate a transformed channel matrix comprising a reduced basis, the lattice reduction comprising:

using a relaxed condition, searching a candidate set of LLL (LLL) iterations with column swap operations in the at least one alternate matrix, whereby the relaxed condition provides for searching the candidate set of LLL iterations without performing size reduction operations on the at least one alternate matrix;

using a relaxed criterion of decrease in LLL potential, wherein the relaxed criterion of decrease in LLL potential comprises

\[ k = \begin{cases} \arg \min_{k \leq \lfloor \sqrt{N_c} \rfloor} \mathbf{f}(k), & \text{if Dual-LR-aided LD} \\ \arg \max_{k \leq \lfloor \sqrt{N_c} \rfloor} \mathbf{f}(k), & \text{if LR-aided SIC / K-best} \end{cases} \]

wherein \( \arg \min_{k \leq \lfloor \sqrt{N_c} \rfloor} \mathbf{f}(k) \) indicates finding a minimum \( k \) value, which is in the range of \( 2, 3, \ldots, N_c \) and meanwhile the corresponding value of \( \mathbf{f}(k) \) is 1, and \( \arg \max_{k \leq \lfloor \sqrt{N_c} \rfloor} \mathbf{f}(k) \) indicates finding a maximum \( k \) value, which of \( 2, 3, \ldots, N_c \) and meanwhile the corresponding value of \( \mathbf{f}(k) \) is 1; wherein LR is lattice reduction, LD is linear detector, and SIC is successive interference cancelation, selecting the first selection from the candidate set of LLL iterations;

comparing the first selection to a predetermined termination condition;

responsive to determining that the termination condition is not met, iteratively selecting a next selection from the candidate set of LLL iterations, each selection iteration comprising:
performing a size reduction of the at least one alternate matrix to obtain at least one reduced matrix;

performing a column swap on the at least one reduced matrix;

using the relaxed condition, searching the at least one reduced matrix for a candidate set of LLL iterations with column swap operations;

using the relaxed criterion of decrease in LLL potential, determining the next selection from the candidate set of LLL iterations; and

comparing the next selection to the termination condition;

responsive to determining that the termination condition is met, generating the reduced basis transformed channel matrix from the at least one alternate matrix; providing the reduced basis transformed channel matrix to a detector; and

based on the reduced basis transformed channel matrix, detecting particular transmit signal vectors for processing.

8. The method of claim 7, wherein the predetermined termination condition comprises \( \text{flag}(k) = \sqrt{2} \left| \mathbf{R}_{k,d}\right| < \left| \mathbf{R}_{k-1} \right| \), wherein the value of \( \sqrt{2} \left| \mathbf{R}_{k,d}\right| < \left| \mathbf{R}_{k-1} \right| \) is 1 if \( \sqrt{2} \left| \mathbf{R}_{k,d}\right| \) is less than \( \left| \mathbf{R}_{k-1} \right| \), otherwise, the value of \( \sqrt{2} \left| \mathbf{R}_{k,d}\right| < \left| \mathbf{R}_{k-1} \right| \) is 0.

9. The method of claim 8, wherein the predetermined termination condition further comprises an iteration count being less than a predefined maximum count.

10. A transmission system comprising:

a plurality of transmitting antennas \( N_t \);

a plurality of receiving antennas \( N_r \);

wherein a received signal vector \( y = [y_1, y_2, \ldots, y_N]^T \) is expressed as \( y = HS + W \), where \( H \) is an \( N_r \times N_t \) channel matrix, \( S = [s_1, s_2, \ldots, s_N]^T \), \( s \in \mathbb{S} \) is a transmit signal vector drawn from a quadrature amplitude modulation (QAM) constellation set \( \mathbb{S} \) with \( |E_{\mathbb{S}}|^2 = \sigma_S^2 \), whose real and imaginary parts are \(-\sqrt{M} + 1, \ldots, -1, \ldots, 1, \ldots, \sqrt{M} - 1 \) with \( M \) being the constellation size of \( S \), and \( W = [w_1, w_2, \ldots, w_N]^T \) is the additive white Gaussian noise vector with zero mean and covariance matrix as \( \sigma^2 I_N \); and

an apparatus comprising:

at least one processor; and

at least one memory comprising computer program instructions, the computer program instructions When executed by the at least one processor, causing the apparatus to:

receive, at each one of the plurality of receiving antennas, a plurality of transmit signal vectors, each of the plurality of transmit signal vectors originating from one of the plurality of transmitting antennas; generate a channel matrix based on the received plurality of transmit signal vectors;

decompose the channel matrix to generate at least one alternate matrix;

perform lattice reduction on the at least one alternate matrix to generate a transformed channel matrix comprising a reduced basis, the lattice reduction comprising:

using a relaxed condition, searching a candidate set of Lenstra-Lenstra-Lovász (LLL) iterations with column swap operations in the at least one alternate matrix, wherein the relaxed condition provides for searching the candidate set of LLL iterations without performing size reduction operations on the at least one alternate matrix;

using a relaxed criterion of decrease in LLL potential to select a first selection from the candidate set of LLL iterations, wherein the relaxed criterion of decrease in LLL potential comprises

\[
\begin{align*}
    k &= \min_{\mathbf{R}_{k,d} \in \mathbb{S}} \left| \frac{\mathbf{R}_{k,d}}{\mathbf{R}_{k-1}} \right| \\
\end{align*}
\]

wherein \( \left| \mathbf{R}_{k,d}\right| \) indicates the absolute value of \( \mathbf{R}_{k,d} \) and \( \min_{\mathbf{R}_{k,d} \in \mathbb{S}} \left| \frac{\mathbf{R}_{k,d}}{\mathbf{R}_{k-1}} \right| \)

indicates finding the \( k \) value in the range of 2, 3, \ldots, \( N_r \) that corresponds to a minimum value in

\[
\left| \frac{\mathbf{R}_{k,d}}{\mathbf{R}_{k-1}} \right|.
\]

comparing the first selection to a predetermined termination condition;

responsive to determining that the termination condition is not met, iteratively selecting a next selection from the candidate set of LLL iterations, each selection iteration comprising:

performing a size reduction of the at least one alternate matrix to obtain at least one reduced matrix;

performing a column swap on the at least one reduced matrix;

using the relaxed condition, searching the at least one reduced matrix for a candidate set of LLL iterations with column swap operations;

using the relaxed criterion of decrease in LLL potential, determining the next selection from the candidate set of LLL iterations; and

comparing the next selection to the termination condition;

responsive to determining that the termination condition is met, generating the reduced basis transformed channel matrix from the at least one alternate matrix; providing the reduced basis transformed channel matrix to a detector;

based on the reduced basis transformed channel matrix, detecting particular transmit signal vectors for processing.

11. The system of claim 10, wherein the transmitting antennas comprise transmitting antennas in a multiple-input, multiple-output system and the receiving antennas comprise receiving antennas in a multiple-input, multiple-output system.

12. The system of claim 10, wherein the relaxed condition for searching the candidate set of iterations comprises

\[
\left| \frac{\mathbf{R}_{k,d}}{\mathbf{R}_{k-1}} \right| \leq \frac{1}{\sqrt{2}}, \quad \forall k \in [2, N_r],
\]

wherein \( \forall k \in [2, N_r] \) indicates each \( k \) value in the range of 2, 3, \ldots, \( N_r \).
13. The system of claim 10, wherein the predetermined termination condition comprises \( \eta_d = 1/\sqrt{2n_\lambda z_1} \), wherein \( \eta_d \) is defined as
\[
\eta_d = \frac{|R_{k,d}|}{|R_{k-1,k-1}|}.
\]
\( \forall k \in [2, N_f] \).

14. The system of claim 13, wherein the predetermined termination condition further comprises an iteration count being less than a predefined maximum count.

15. The system of claim 10, wherein the relaxed condition for searching the candidate set of iterations comprises \( \forall k \in [2, N_f] \), wherein the value of \( \forall k \in [2, N_f] \) satisfying the condition if \( (\forall k \in [2, N_f] < |R_{k-1,k-1}|) \) is 1 if \( (\forall k \in [2, N_f] < |R_{k-1,k-1}|) \) is less than \( |R_{k-1,k-1}| \), otherwise, the value of \( \forall k \in [2, N_f] \) satisfying the condition if \( (\forall k \in [2, N_f] < |R_{k-1,k-1}|) \) is 0.

16. A transmission system comprising:

- a plurality of transmitting antennas \( N_t \);
- a plurality of receiving antennas \( N_r \);
- wherein a received signal vector \( y = [y_1, y_2, \ldots, y_N] \) is expressed as \( y = Hs + w \), where \( H \) is an \( N_r \times N_t \) channel matrix, \( s = [s_1, s_2, \ldots, s_N] \), \( (s \in S) \) is a transmit signal vector drawn from a quadrature amplitude modulation (QAM) constellation set \( S \) with \( \mathbb{E}[ss^H] = \sigma_s^2 I_N \), where real and imaginary parts are \( \pm \sqrt{M} \) with \( M \) being the constellation size of \( S \), and \( w = [w_1, w_2, \ldots, w_N] \) is the additive white Gaussian noise vector with zero mean and covariance matrix \( \sigma_w^2 I_N \); and
- an apparatus comprising:

  - at least one processor; and
  - at least one memory comprising computer program instructions, the computer program instructions when executed by the at least one processor, causing the apparatus to:

- receive, at each one of the plurality of receiving antennas, a plurality of transmit signal vectors, each of the plurality of transmit signal vectors originating from one of the plurality of transmitting antennas;
- generate a channel matrix based on the received plurality of transmit signal vectors;
- decompose the channel matrix to generate at least one alternate matrix;
- perform lattice reduction on the at least one alternate matrix to generate a transformed channel matrix comprising a reduced basis, the lattice reduction comprising:

  - using a relaxed condition, searching a candidate set of Lenstra-Lenstra-Lovász (LLL) iterations with column swap operations in the at least one alternate matrix, wherein the relaxed condition provides for searching the candidate set of LLL iterations without performing size reduction operations on the at least one alternate matrix;

17. The system of claim 16, wherein the predetermined termination condition comprises \( \text{flag}((k) = (\forall k \in [2, N_f] < |R_{k,k}|) \), wherein the value of \( \forall k \in [2, N_f] < |R_{k,k}| \) is 1 if \( \forall k \in [2, N_f] < |R_{k,k}| \) is less than \( |R_{k,k}| \), otherwise, the value of \( \forall k \in [2, N_f] < |R_{k,k}| \) is 0.

18. The system of claim 17, wherein the predetermined termination condition further comprises an iteration count being less than a predefined maximum count.

* * * * *