Final Report: Optimal Linearity Testing of Sigma-Delta Based Incremental ADCs Using Restricted Code Measurements

S. Kook¹, A. Gomes², L. Jin, D. Wheelright² and A. Chatterjee¹
School of ECE, Georgia Tech, Atlanta, GA¹
National Semiconductor Corporation, Santa Clara, CA²

Abstract: Linearity testing of high-precision (beyond 20-bit resolution) Analog-to-Digital converters (ADCs) is extremely expensive due to the large number of codes (>16 million for a 24-bit converter) that need to be tested and the associated low data rates making traditional histogram based testing infeasible. Industry often performs linearity test for such high-precision data converters with significantly reduced numbers of code measurements during production test. Given a specified allowed number of code measurements, the problem is to determine the requisite code points that result in the highest failure coverage. In this report, a methodology and tools for analyzing the “goodness” of a particular choice of test code points versus another is described. A least squares based polynomial fitting approach using measurements made at selected test code points is used to characterize the transfer function of the ADC for INL (Integral Nonlinearity) error. In addition, the characteristics of devices that may escape from the proposed approach (test escapes) are revealed for the specified test via an optimization based search technique. Software simulations are performed to study and validate the proposed methodology.

I. INTRODUCTION

With the new generation of highly integrated mixed-signal System-on-Packages (SoPs) and System-on-Packages (SoPs) and the advantages of digital processing, data converters are increasingly used between the analog-digital boundaries of such systems. Hence, the performance of such systems highly depends on the performance and quality of the data converters. Due to the demand for high-resolution data converters for sensing as well as high-precision audio/ high-definition video applications, ΔΣ ADCs and ΔΣ based incremental ADCs have received substantial attention in the recent past. However, the increased resolution of such converters has resulted in tighter linearity requirements driving up associated manufacturing and production test costs. As a result, there is great need for a low cost test methodology that allows such converters to be tested rapidly in production without compromising failure coverage.

The histogram test method, also called the code-density method, is the standard linearity test technique for data converters. The histogram test applies a precise ramp or sinusoidal signal to the ADC under test across a large number of cycles and uses the number of hits per code to calculate the individual code widths of the data converter. To guarantee test quality, larger than 30 hits per code and up to several hundred hits per code might be necessary. In addition, a high-precision input signal, at least 3-bit higher resolution than the ADC under test, is needed for histogram test, thereby increasing the cost of test instrumentation. Since high-resolution ADCs are relatively low-speed devices, collecting a large number of such output codes with an expensive test stimulus generator dramatically increases the test time and cost [1]-[2].

There has been significant work in the past to address the challenges of histogram testing for high precision data converters. In [3], Deterministic Dynamic Element Matching (DDEM) based test technique is proposed that allow testing of high precision data converters using “inexpensive” input stimuli. This method allows histogram testing of a higher resolution ADC by using a lower resolution DAC along with additional measurements that effectively cancel out DAC nonidealities using back-end mathematical analysis of the test data based on an assumed ADC transfer function model. In [4]-[5], the authors propose a Stimulus Error Identification and Removal (SEIR) technique to compensate for the non-linearity present in the input test stimulus. In order to guarantee the spectral purity at the output of the DAC a low-pass filter or a band-pass filter is used. While the method reduces the amount of data collection, it still requires the use of a large set of measurements for high-precision ADCs. A least square based approach with scaling and segmentation is explored to reduce the test time and test throughput for linearity specification testing of high-resolution ADCs [6]. The approach uses two lower resolution DACs to generate the test stimulus. It reduces test cost by using low precision input signals and reduces test time by sampling the overall set of ADC codes and using a least squares fitting algorithm to determine the coefficients of the input-output transfer function polynomial corresponding to the converter. Linear model based test is proposed in [7]-[8]. The approach builds a linear model in terms of code transition points and errors and measures only a defined subset of code transition levels. In addition, authors in [11]-[13] propose the nonlinearity testing of ADCs from spectral measurements, which are adequate for high-resolution ADC testing.

All the techniques presented above reduce the amount of data collection and/or ease the tight requirement for expensive test stimulus generation. Nevertheless, these methods still require excessive test time and cannot be adopted by industry as production test solutions. In contrast, the test methodology proposed in this research aims to
determine the best codes to measure that allow the nonlinearity of the ADC to be measured as accurately as possible given a maximum number of allowed code measurements. Then an algorithm to evaluate the characteristics of bad devices that could escape the applied test is developed.

II. Objectives

The goals and objectives of the proposed work in this report are outlined as follows:

- Develop a fast INL test for high-precision ADCs that can be adopted by industry as a production test solution.
- Develop a methodology that allows accurate INL estimation for a high-resolution ADC with extremely small number of code measurements with minimal loss of failure coverage.
- Develop a methodology that defines the minimum necessary test code points.
- Develop a methodology that defines test escapes and reveals the characteristics of such devices.

In the following sections, we first describe the behavioral model of a high-precision ADC, which is used to study and validate the proposed methodology. The proposed test methodology is presented in Section 4, and the optimization approach for characterizing possible test escapes described in Section 5.

III. BEHAVIORAL MODEL OF ΔΣ ADC

High-precision data converters are implemented using Sigma-Delta architectures due to their over-sampling, averaging and noise shaping properties. A 24-bit 3rd order C1FF Sigma-Delta incremental ADC has been modeled in Matlab and Simulink incorporating key module level nonlinearities as shown in Figure 1. Main nonlinearities modeled are as follows:

1) clock jitter at the input sampler
2) kT/C noise in switched-capacitor circuit
3) operational amplifier DC gain
4) operational amplifier slew rate
5) operational amplifier gain bandwidth
6) operational amplifier input referred noise
7) operational amplifier saturation voltage level
8) operational amplifier total harmonic distortion
9) operational amplifier offset
10) operational amplifier PSRR
11) operational amplifier CMRR

Details of non-idealities are well studied and explained in literatures [9].

IV. Test Code Selection Approach

In the following, first the test problem is defined. Next, the details of the proposed test methodology are discussed.

IV.1. Problem Definition

Data converters with 24-bit resolution have more than 16 million codes. Testing such converters with the histogram method mandates collection of more than 480 million or 1.6 billion output samples with an average number of 30 to 100 samples per code. Further, such high-resolution ADCs generally have a low sampling rate, which in turn implies long test times. Sigma-Delta based incremental converters have maximum output data rate of a few hundred samples per second. In addition, voltage drifts in the tester must be taken into account. Although advanced ATE may supply a stationary reference voltage over small periods of time, small drifts over long test times can substantially affect the overall test quality. As a result, the histogram based test method is not feasible for such converters, and thus a fast test approach that can reduce the volume of test data collection is highly necessary.

IV.2. Test with Reduced Number of Codes

In this section, we propose the least square based polynomial fitting method via test code selection for 24-bit resolution ADCs.

Full histogram based test is not suitable for testing extremely high-resolution ADCs in industry as stated above, but the histogram test method can be practical when the resolution of ADCs under test is forced to be less (reduced code measurements) than the full-code measurement. Figure 2 illustrates the basic concept of such an approach using a 4-bit resolution ADC test as an example. In this Figure, 4-bit resolution is reduced to 2-bit resolution by
treating code 0 to code 3 of the 4-bit ADC as code 0 and treating code 4 to code 7 of the 4-bit ADC as code 1 and so on. As a result, a 2-bit equivalent histogram can be constructed for a 4-bit ADC histogram. For the same test time, one can achieve 115 samples per code for 2-bit equivalent ADC or 30 samples per code for the original 4-bit ADC. In contrast, for the same number of 100 hits per code testing a 4-bit ADC requires a total of 1600 samples while testing the 2-bit equivalent ADC requires only 400 samples. However, relatively good approximation of \textit{INL} can be extracted with significantly reduced test data volume in the latter case. Figure 3 – 6 depict INL plots of the identical 24-bit resolution ADC using reduced resolution histogram. In all cases, an average number of 100 samples per code was collected. These results indicate that INL errors are well approximated with significantly fewer samples although DNL errors are not explored. Figure 7 compares the plot in Figure 5 with the INL estimated using polynomial fitting \textit{across only 4 precise input signal values} (-5V, -2.5V, 2.5V, 5V). In this estimation, 3rd order polynomial function was used, and 100 measurements for each point were taken and averaged in order to suppress the noise effect. In this case, the INL was not estimated from the histogram but from the polynomial fitting of 4 points corresponding to 4 DC input values. The results indicate that surprisingly small amount of test data can be used to accurately predict INL of a 24bit ADC. The polynomial-fitting based test is a popular method to characterize such transfer function of the system or ADCs [6], [11], [13]. However, a key question is whether these 4 code measurements are sufficient to predict \textit{all} ADC anomalies induced by small and large process variations and parasitics. To study the effects of process variations, a population of 500 devices was implemented with process variations generated from Monte Carlo simulation, each instance with a unique combination of parameter (nonlinearity) values.
IV. Test Code Selection

In order to find the optimal set of test measurement points for the maximum fault coverage, the use of Principal Component Analysis (PCA) is developed in this report. PCA, a well-known statistical technique, is widely used in data analysis and compression, and reduces the dimensionality of data while retaining as much information as possible of the variations present in the original data set through an orthogonal transformation. All the possible digital codes of a 24-bit ADC are considered as variables, and the PCA analysis converts these into a subset of new variables (principal components or test code points), in such a way that the transfer function of the ADC can be reconstructed from the principal components (which are significantly fewer in number than the full set of digital codes of the 24-bit ADC). The principal components can be easily calculated using the PCA toolset available in the MATLAB statistics toolbox.

The approach begins with the use of the first three principal components, which are subsequently used to fit a 2nd order polynomial function for the ADC transfer function. The larger the number of principal components that are considered, the higher the total measurements samples that are needed and the better the INL estimate for the ADC under test. The goal is to keep the number of principal components to a minimum, to reduce the total test time. Further, use of many principal components does not always result in the best INL estimate since 1) the first few principal components are generally dominant and give a good approximation to the overall INL statistics and 2) use of high order polynomial functions can result in over-fitting. Note that maximum possible degree of the polynomial function (the number of principal components – 1) is used all the time, but the highest degree is limited to a 5th order polynomial in order to avoid over-fitting.

We consider a case in which some or all of the selected principal components (as known as test code points) are located in certain regions of the code space only. This undesirable code selection ends up with unavoidable test-fail because the full-scale transfer function must be reconstructed from the test data. In order for the test code points to be distributed across full-scale, it is necessary to include “anchor points” into the polynomial calculation. These anchor points consist of predetermined input-output values corresponding to non-significant principal components that are used during polynomial fitting but are not measured for each device that is tested.

Table 1 presents the first 10 principal components (test code points) produce. The digital codes for the 24-bit ADC model range from -8388608 to 8388608, and the input signal range is from -5V to +5V. The full-scale range was divided into 10 sub-regions with at least one code selected from each sub-region. Note that the analog DC values that correspond to such code points found from PCA are candidates for test stimuli.

Table 1. Principal Components

<table>
<thead>
<tr>
<th>Test Code Points</th>
<th>Input Signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>1st Principal Comp.</td>
<td>-8297945</td>
</tr>
<tr>
<td>2nd Principal Comp.</td>
<td>-7205814</td>
</tr>
<tr>
<td>3rd Principal Comp.</td>
<td>7071597</td>
</tr>
<tr>
<td>4th Principal Comp.</td>
<td>-2910847</td>
</tr>
<tr>
<td>5th Principal Comp.</td>
<td>2634023</td>
</tr>
<tr>
<td>6th Principal Comp.</td>
<td>5701737</td>
</tr>
<tr>
<td>7th Principal Comp.</td>
<td>2088763</td>
</tr>
<tr>
<td>8th Principal Comp.</td>
<td>-5695865</td>
</tr>
<tr>
<td>9th Principal Comp.</td>
<td>-1066167</td>
</tr>
<tr>
<td>10th Principal Comp.</td>
<td>1778385</td>
</tr>
</tbody>
</table>

Table 2 summarizes the results using different number of principal components. First column indicates the number of principal components, and the degree of polynomial function is given in the second column. The third column shows the number of devices, in which polynomial function with corresponding principal components fails to estimate the actual INLS. From the table 2, 5th order polynomial function with the first 5 principal components give the best INL predictions. Higher degree polynomial functions with 7 or more principal components results in over-fitting. With six test code points and 5th order polynomial fitting, the INL estimate of Figure 8 were improved as seen in Figure 9.

Table 2. Performances of Principal Components

<table>
<thead>
<tr>
<th>Number of Principal Comp.</th>
<th>Polynomial Degree</th>
<th>Fault Estimation (out of 500)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>2</td>
<td>76</td>
</tr>
<tr>
<td>4</td>
<td>3</td>
<td>21</td>
</tr>
<tr>
<td>5</td>
<td>4</td>
<td>8</td>
</tr>
<tr>
<td>6</td>
<td>5</td>
<td>1</td>
</tr>
<tr>
<td>7</td>
<td>5</td>
<td>1</td>
</tr>
</tbody>
</table>

V. Search Algorithm for Characterization of Test Escapes

The proposed technique defines the test code selection and achieves test time reduction with significantly small number of measurements. However, the approach cannot guarantee 100% fault coverage as long as there exist undetectable faulty devices that escape from the proposed test approach but whose actual INLS are bad due to inaccurate estimation. In this section, an optimization based search algorithm is introduced for finding such devices.
(ADCs), and a set of ADC nonlinearity characteristics (device vulnerability) that make the faulty DUTs pass the proposed test will be identified.

An Augmented Lagrange based optimization technique is used to find undetectable bad devices as a search algorithm in this report. This Augmented Lagrange approach is useful in our study since the method converts a constrained problem into an unconstrained function. Similar to other constrained optimization problems, the technique minimizes our objective function subject to constraints. The optimization problem is formed as follows:

**Objective function:** \( \min \{ f(x) \} \)

**Subject function (constraints):** \( G(x) \leq 0 \)

The Augmented Lagrange based optimization technique minimizes objective function while satisfying the subjective function of \( G(x)=[g_1(x), g_2(x), \ldots, g_n(x)] \). Our goal is to search undetectable faulty devices that escape our INL test (test pass/spec. fail). INL errors obtained from full-code measurements and obtained from our proposed method are defined as \( \text{Full\_Test}_k \) and \( \text{Reduced\_Test}_k \) for a specific device \( \text{k} \). When the maximum allowable INL error is defined as \( \text{INL\_Limit} \), then above objective and constrained functions are constructed as

\[
\begin{align*}
f(x) &= \max\{\text{Reduced\_Test}_k\} - \text{INL\_Limit} \leq 0 \\
G(x) &= \text{INL\_Limit} - \max\{\text{Full\_Test}_k\} \leq 0
\end{align*}
\]

If the problem is concerned with various specifications, \( G(x) \) can be a set of \( G(x)=[g_1(x), g_2(x), \ldots, g_n(x)] \) where \( n \) is the number of specifications in consideration. However, since our study is associated with only INL in this report, we solve the problem with only one constraint. The Augmented Lagrange function can be formulated in various ways, and we adapt the function presented in [10], which is

\[
L(x, \lambda, \gamma) = f(x) + \sum_{i=1}^{N} \left[ \max \left( \frac{1}{2} \lambda_i + \gamma \cdot g_i(x), 0 \right) \right]^2
\]

where \( \lambda_i \) is Lagrangian multipliers, \( \gamma \) is penalty parameter, and \( x \) is a combination of parameters (nonlinearity). A flow of the algorithm is presented in Figure 10.

For simplicity, an example of the algorithm is experimented using 2500 devices with variations of only two nonlinearities (OP AMP Slew Rate and Gain Bandwidth). Devices with two nonlinearities allow us to generate 3-D surface plot and track the search path of the algorithm. Devices with maximum INL error of 10 ppm or higher are defined as faulty devices and as good devices with maximum INL error of less than 10 ppm. The surface plot is presented in Figure 11. The device at the destination in Figure 11 is the escaped device from our proposed approach. Its maximum INL error was estimated as 9.185ppm, but its actual maximum INL error was 12.82ppm. One iteration of the algorithm finds one undetectable faulty device, and the algorithm iterates until there is no more undetectable faulty device.

**Figure 10. Augmented Lagrange Search Algorithm Flow.**

**Figure 11. Example of Augmented Lagrange Search.**

Described search algorithm was applied to the identical set of 500 devices used in the previous section. One faulty device previously passes the proposed test when using six test code points, and this device was found using the search algorithm. Figure 12 shows the undetectable faulty device found among 500 instances. The 24-bit ADCs are consist of 11 nonlinearities as described in Section 3, but the resulted plots are presented with only 4 nonlinearities in Figure 12 to avoid redundant plots. The result reveals the set of nonlinearities for the undetectable faulty device that allow the device to escape from our proposed test approach.

**VI. Conclusion**

In this report, a fast linearity test for high-resolution (i.e. 24-bit) was proposed as industry solution. The proposed technique is based on a least squares based polynomial fitting using measurements made at the selected test code points, and the requisite test code points for the highest failure coverage are determined by principal component analysis. Furthermore, an optimization based search algorithm is developed to detect the devices that escape from the applied proposed test method and to reveal the
characteristics of such devices. Our approach achieves extremely fast yet accurate INL estimations with significantly small number of measurements for high-precision ADCs whose static specifications performances are hard to be characterized by the traditional histogram test.

VII. References


