Final Report for NSF Award #1042187

Project Title: EAGER, New Concept for Low Cost, High Throughput Inspection for Cracks in PV Manufacturing
Award Number: 1042187

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Activities and Findings:

The research objectives of this project were to validate a new concept in surface inspection of thin crystalline silicon wafers of the type used in photovoltaic manufacturing with electrostatic imaging technique (Kelvin probes) to reveal surface cracks. A wafer scanning system consisting of multiple probes, Kelvin probe sensors (vibrating and non-vibrating) and a fiber optic sensor, with a scanning dimension up to 8 inch square, was successfully designed and built from this award, as shown in Fig.1. The wafer scanning system allows for measuring and inspecting silicon wafers and cells under different illumination conditions. A variety of silicon wafers and cells were tested, which indicated the detectability of crack from surface potential maps.

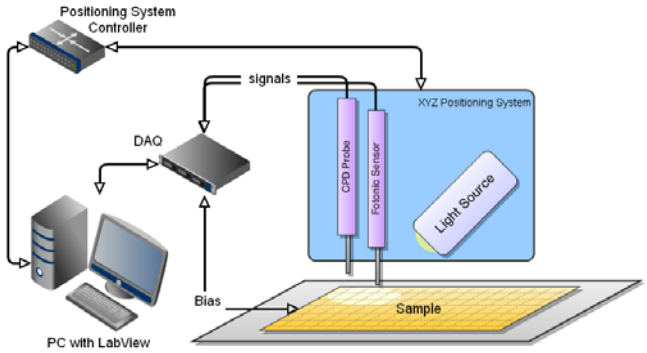


Fig.1. Schematic diagram of the scanning system.

Fig. 2 shows examples of the surface potential maps for four different single crystalline silicon cells in the dark condition. A good uniformity can be found on those cells, except for the cell D.

A large surface potential difference is also found on the lower left corner on the cell C, where a crack exists.

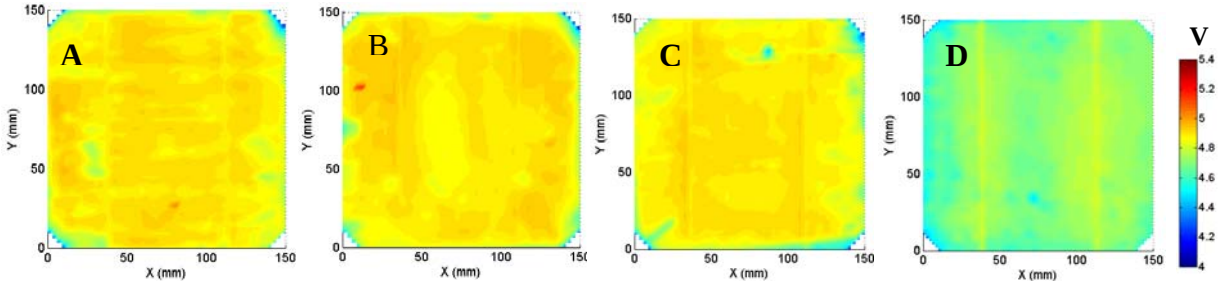


Fig. 2. Surface potential of four single crystalline silicon cells (A, B, C, D) in dark condition.

Surface potential was further analyzed under light illumination. Fig. 3 shows the delta surface potential images derived from the light and dark scans. It can be seen that the cell without micro-cracks (cell A) shows a much higher delta surface potential than the cells with the micro-cracks. Micro-cracks on the cells lead to a reduced delta surface potential. In fact, micro-cracks on the cell D behave like a shunting spot, which drains the current completely. A potential gradient towards the micro-cracks is also visible in the surrounding area.

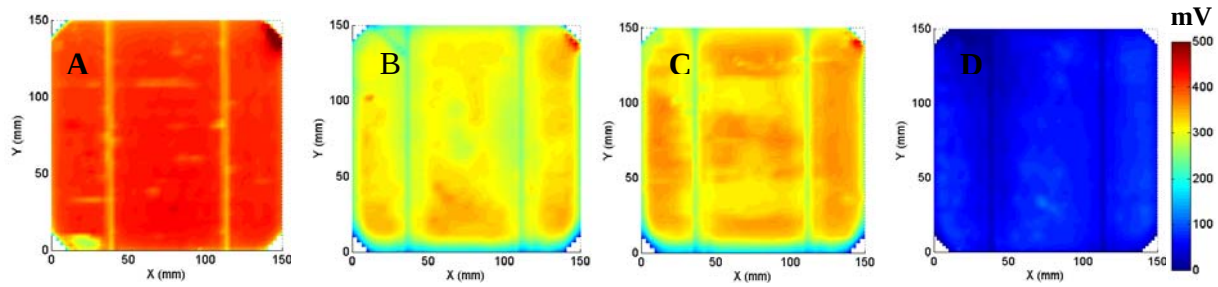
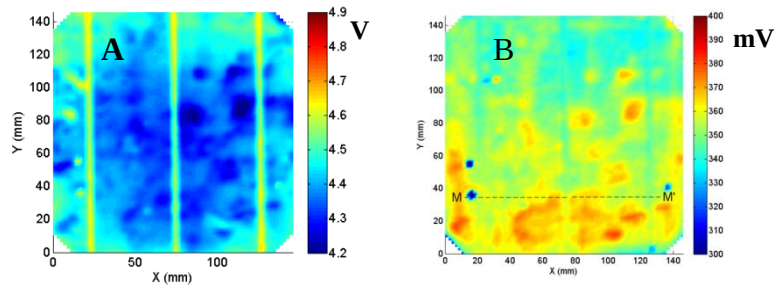


Fig. 3. Delta surface potential of four single crystalline silicon cells (A, B, C, D).

Fig. 4 shows the surface potential difference between single crystalline and multi-crystalline silicon wafers. The process defects will affect both delta surface potential (ΔV_{SP}) and surface band bending (ϕ) of the cells. Higher surface potential and higher delta surface potential ΔV_{SP} was found on the sc-Si cells than mc-Si cells. We conclude that high ΔV_{SP} and low ϕ_s are expected to contribute to the high conversion efficiency on a cell.



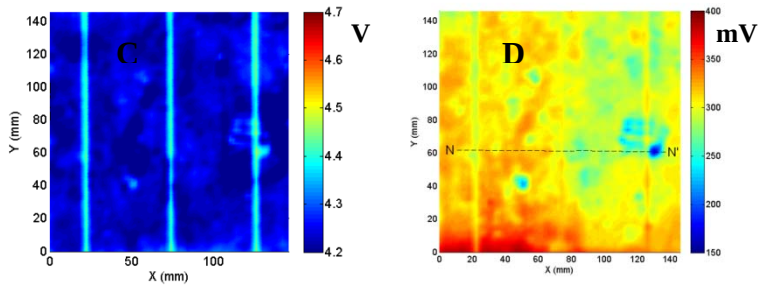


Fig.4.Dark surface potential (SP) and delta surface potential (ΔV_{SP}) maps of sc-Si (A,B) and mc-Si (C,D) cells.

In conclusion, we explored the concept of detecting surface micro-cracks on silicon wafers with capacitive Kelvin probes. We demonstrated the capability of measuring micro-cracks and also a variety of process defects on silicon PV solar cells.

Publications:

There are a total of four papers published and two patent disclosures under the sponsorship of this award.

1. Yang, C. Pyekh, Y. and Danyluk, S., Surface Potential Imaging of PV Cells with a Kelvin Probe, Solar Energy Materials & Solar Cells, Vol. 102, 2012, pp. 167-172.
2. Yang, C. and Danyluk, S., A Multi-Purpose Wafer Scanning System for PV Inspection, The 38th IEEE Photovoltaic Specialists Conference, Austin, TX, USA. June 3-8, 2012,
3. Yang, C. Pyekh, Y. and Danyluk, S., Crack Induced Surface Potential Variation on Si PV Cells, 37th IEEE Photovoltaic Specialists Conference, Seattle, WA, June 19-24, 2011
4. Yang, C. Pyekh, Y. and Danluk, S., A new metrology system for high speed, high throughput inspection of PV wafer/cell cracks, the 2011 NSF Engineering Research and Innovation Conference, Atlanta, GA, January 4-7, 2011.

Patent disclosures

1. Danyluk, S. and Yang, Y., A Method and Apparatus for Characterizing and Mapping PV Cell Performances Utilizing Kelvin Probes and Controlled Illumination, US patent 61/468,350 (2011).
2. Yang, Y. and Danyluk, S., Measurement of Wafer Curvature and TTV for Thin PV Wafers, US patent 61/511,676 (2011).