Project Participants

Senior Personnel

Name: Sitaraman, Suresh
Worked for more than 160 Hours: Yes
Contribution to Project:
Prof. Sitaraman is the principal investigator of the project and is responsible for the overall direction of the project. In particular, he directs the fabrication and mechanical aspects of the project.

Name: Swaminathan, Madhavan
Worked for more than 160 Hours: Yes
Contribution to Project:
Prof. Swaminathan is the co-PI on the project and is responsible for the overall direction of the project. In particular, he directs the electrical modeling and characterization of the compliant interconnects.

Post-doc

Graduate Student

Name: Okereke, Raphael
Worked for more than 160 Hours: Yes
Contribution to Project:
Raphael Okereke, a Mechanical Engineering PhD student, is responsible for fabricating the compliant interconnects and assessing the interconnect reliability.

Name: Huh, Suzanne
Worked for more than 160 Hours: Yes
Contribution to Project:
PhD student Suzanne Huh works on the electrical modeling of compliant interconnects and their comparison using multiple tools. Using S-parameters, RLC models and eye diagrams, she determines the electrical characteristics of the multi-path compliant interconnects to be able to identify the likely candidates for further fabrication and experimental characterization.

Name: Bhat, Anirudh
Worked for more than 160 Hours: Yes
Contribution to Project:
Anirudh Bhatt is a master’s student in Mechanical Engineering and is responsible for understanding the compliance and response of the interconnects under impact loading.

Name: Woodrum, David
Worked for more than 160 Hours: Yes
Contribution to Project:
David Casey Woodrum explored how compliant interconnects could be used in practical applications.

Name: Chen, Wei
Worked for more than 160 Hours: No
Contribution to Project:
Wei Chen was involved in developing analytical models for compliance calculations.

Undergraduate Student

Name: Lee, Robert

Worked for more than 160 Hours: Yes

Contribution to Project:
Robert Lee, an undergraduate Mechanical Engineering student, is responsible for developing interconnect geometries and assessing their compliance.

Name: Ramesh, Pranav

Worked for more than 160 Hours: No

Contribution to Project:
Pranav Ramesh, an undergraduate student in Electrical and Computer Engineering, helps with electrical modeling and test vehicle layout.

Name: Green, Trevor

Worked for more than 160 Hours: Yes

Contribution to Project:
Trevor Green, an undergraduate student in Electrical and Computer Engineering, helps with electrical aspects of the project.

Technician, Programmer

Other Participant

Research Experience for Undergraduates

Organizational Partners

Qualcomm Incorporated
Based on the results obtained in this project, Qualcomm has provided additional funding to explore compliant interconnects for other applications.

Other Collaborators or Contacts
- We have presented the work to Qualcomm. They are very interested in this work and have provided additional funding to continue the work.
- We have presented the compliant interconnect concept to Freescale Semiconductor. They are interested in this idea for their MEMS applications.
- We have also presented the work to Intel Corp. Intel is continued to be interested in compliant interconnects.

Activities and Findings

Research and Education Activities: (See PDF version submitted by PI at the end of the report)
The attached file provides a summary of all research and education activities.

Findings: (See PDF version submitted by PI at the end of the report)
The attached file provides a summary of major findings for this project.

Training and Development:
1) Mechanical Engineering (ME) PhD student Raphael Okereke has gained valuable experience in cleanroom fabrication and characterization of compliant interconnects.
2) Electrical and Computer Engineering (ECE) PhD student Suzanne Huh has gained valuable experience in electrical modeling and simulation of compliant interconnects.

3) Mechanical Engineering (ME) PhD student Wei Chen gained experience in theoretical modeling of compliant interconnects.

4) Mechanical Engineering MS student Anirudh Bhat has worked on dynamic reliability of compliant interconnects and has graduated with his MS degree to work in a high-performance semiconductor company. MS student David Casey Woodrum intends to pursue PhD at Georgia Tech starting Spring 2013.

5) Undergraduate ME student Rob Lee has designed several variations of compliant interconnects and determined the compliance of such structures through computer models.

6) PhD Raphael Okereke has gained experience in mentoring undergraduate student Rob Lee.

7) Undergraduate ECE students Pranav Ramesh and Trevor Green have gained experience in mask design and electrical modeling and simulation of compliant interconnects. Ramesh will be pursuing his graduate degree in ECE.

8) PhD student Suzanne Huh has gained experience in mentoring undergraduate student Pranav Ramesh.

9) PhD student Raphael Okereke won the First Place in the 2010 Student Poster Competition, The Electronic and Photonic Packaging Division, ASME 2010 International Mechanical Engineering Congress and Exposition (IMECE2010), November 2010, Vancouver, British Columbia, Canada. Also, he won the 1st Place Best Student Paper (Poster) award at the Global Interposer Technology Workshop, Nov. 2012 for the poster entitled, 'Mechanically Compliant Single-Path and Multi-Path Electrical Interconnects.'

Outreach Activities:
1) We have presented the compliant interconnect technology to the industry attendees of the 3D IC Packaging Technical Symposium organized by the Packaging Research Center at Georgia Tech in April 2010 and also at the Global Interposer Technology Workshop, Nov. 2011 and Nov. 2012.

2) The material has been presented in ASME International Mechanical Engineering Congress and Exposition (IMECE) 2010 as well as Electronic Components and Technology Conference 2011.

3) The material from this project is routinely presented in industry meetings and other avenues to be able to reach a wider audience.

Journal Publications


Books or Other One-time Publications


Bibliography: IMECE2010-38376
We have submitted an invention disclosure describing various proposed designs of the compliant interconnects. The proposed interconnects will have multiple paths with multiple posts to obtain high compliance as well as acceptable electrical parasitics.

Sharing Information:
The proposed invention will be important to address thermo-mechanical reliability challenges with interconnects for 3D packaging structures. Also, it will enhance the reliability of low-K/Cu dies by decoupling the dies from the substrates and thus reducing the stresses induced in the die. Thus, the proposed invention will have significant contribution to microelectronics and microelectronic packaging industries.

Contributions within Discipline:
1) The proposed multi-path compliant interconnects provide a paradigm shift in microelectronics and microelectronic packaging industries by addressing one of the important reliability concerns. The interconnects can decouple the die from the substrate and therefore, can reduce the stresses in the die. The reduced stresses will ensure that the low-K dielectric material in the current and future generations of ICs will not crack or delaminate.
2) By using multiple electrical paths, the proposed interconnect will add redundancy to the interconnect and at the same time, enhance the interconnect's electrical metrics.
3) The proposed interconnects do not require an underfill for thermo-mechanical reliability and therefore, the packaging assembly will be reworkable.
4) By employing wafer-level processing, low-cost fabrication is feasible, and by using traditional fabrication steps, the proposed interconnects can be easily fabricated in existing wafer fab without the need for additional infrastructure.
5) The proposed interconnects are scalable, and therefore, the interconnects can meet the fine pitch requirements of current and future microelectronic systems.

Contributions to Other Disciplines:
1) Beyond microelectronic packaging industry, the proposed structures can be used in interfaces in energy systems where dissimilar materials need to be decoupled.
2) Beyond electrical interconnects, the proposed structures can be used as thermal interface layer to be able to mechanically decouple the heat-generating dies from heatspreaders and to provide a thermal path for the thermal management of dies.
3) The proposed structures can also function as vibration isolators for MEMS and other microelectronic systems.
4) By attaching suitable magnetic material, the proposed structures can be used for characterizing interfacial strength of dissimilar materials.
5) By bio-conjugating the interconnect geometries with monoclonal antibodies, the geometries can be used to detect cancer- or other disease-specific antigens or other biomolecules in serum. Such an ability to measure low concentration of biomolecules will help with early diagnosis and treatment of cancer and other diseases.

Contributions to Human Resource Development:
1) Three PhD students ? two in Mechanical Engineering (ME) and the third in Electrical and Computer Engineering (ECE) ? have worked on this project. One ME PhD student has gained valuable experience in cleanroom fabrication and characterization of compliant interconnects. The other ME PhD student has gained experience in theoretical modeling of compliant interconnects. The ECE PhD student has gained valuable experience in electrical modeling and simulation of the compliant interconnects.
2) Of the three PhD students, one ME PhD student is an African American, while the ECE PhD student is a woman. Thus, the project is
training students from under-represented groups toward their doctoral research.

3) One MS student in Mechanical Engineering has worked on the dynamic simulations and drop testing of the compliant interconnects. The student has contributed toward understanding the reliability of the interconnects under drop testing. Another MS student intends to pursue PhD at Georgia Tech starting Spring 2013.

4) Three undergraduate students, one in Mechanical Engineering, recently graduated, and the other two in Electrical and Computer Engineering, have worked on mechanical design and compliance of the structures as well as the mask design and electrical simulation of the structures.

5) By mentoring the undergraduate students, the graduate students gain valuable mentoring experience.

6) The compliant interconnects have been integrated in classroom teaching as well.

Contributions to Resources for Research and Education:

1) Thermo-mechanical and electrical models have been developed as part of this project. These models can be used in other projects as well as in classroom exercises, as needed.

2) Fabrication recipes are being developed and/or modified. These recipes can be used in other projects as well as in cleanroom exercises, as needed.

3) Invention disclosure on multi-path compliant interconnects has been filed. This could lead to wider adaptation or commercialization of the developed technology.

Contributions Beyond Science and Engineering:

1) The proposed interconnect technology can be used in a number of microelectronic systems used in computer, telecommunication, medical, and other applications, and thus, the proposed technology will have far-reaching implications.

2) By using reworkable and environmentally friendly lead-free assembly processes, the proposed interconnect technology will be important from environmental considerations.

3) The proposed technology is a good candidate for commercialization, and therefore, may contribute toward setting up a start-up company and employing people in a high technology industry.

4) With appropriate modifications, the proposed technology can be used as a bio-sensor, and thus can be used for detecting low levels of concentration of serum biomolecules associated with various diseases. Therefore, the proposed technology could play a critical role in early diagnosis and effective treatment of cancer and other diseases.

Conference Proceedings

Categories for which nothing is reported:

Any Web/Internet Site
Any Conference
FINDINGS

- Several multi-path compliant interconnect designs were developed as part of this project. It was found that some of the multi-path interconnects provide better mechanical compliance compared to single-path interconnect.

- When the number of legs for a fan structure was increased, it was found that the electrical performance of the interconnect would improve. However, the mechanical compliance will decrease. Thus, one needs to balance the mechanical and electrical metrics to obtain the optimum number of paths for the interconnects.

- It was found that arc-like structures provide better mechanical compliance than spline-like structures when used in multi-path compliant interconnects.

- Through simulations, it was seen that the stresses induced in the die will be minimum, and therefore, the proposed interconnects will help prevent the cracking or the delamination of low-K dielectric in the current and future generations of microelectronic systems.

- It was found that under thermal cycling, most of the differential displacements will be borne by the compliant arcuate structures, and thus, the interconnects will help reduce stresses elsewhere in the assembly, as designed and intended.

- It was found that as the interconnect has more parallel paths from the substrate pad to the die pad, the least parasitic resistance and inductance are achieved. The resistance and inductance scales with the number of legs of the structure.

- To determine the optimized number of legs, the actual performance metrics are calculated to compare the expected performance degradation of the selected interconnects. The metrics included the DC drop, inductive drop, and total voltage drop. Since the parasitic scaled with the number of legs, both DC drop and inductive drop scaled with the number of legs as well.

- Current density per leg was calculated to ensure that the interconnects would be safe from electromigration-related problems. It was found that all fan interconnects had a large enough cross section per leg.

- A heterogeneous array of interconnects offer an excellent compromise between mechanical compliance and electrical parasitics.

- Under drop impact loading, the compliant interconnects will be able to isolate the die from the substrate and thus can function as vibration isolators for microelectronic and MEMS devices in addition to being electrical interconnects.
1.0 INTRODUCTION

With the introduction of on-chip low-K dielectric materials, it is increasingly important to reduce on-chip stresses so that the low-K dielectric material will not crack or delaminate. One way to reduce the thermo-mechanical stresses is to introduce compliant structures between the die and the substrate and thus to decouple the die from the substrate. Decoupling the die from the substrate or the substrate from the board by means of mechanically compliant interconnects will reduce stresses created by the coefficient of thermal expansion mismatch. A decoupled die-substrate or substrate-board interface will allow the different components to expand or contract differently without inducing high stresses in the components. In this work, we report the design, fabrication, modeling, and characterization of innovative multi-path fan-shaped off-chip compliant interconnects. The proposed interconnects can be fabricated at the wafer-level and are cost-effective, can be of fine pitch and scalable, and will have redundant electrical paths.

Fan-shaped interconnects with two, three, or four arcs have been designed. In these interconnects, the outer ends of the arcs will be connected to the die pad, while the center or hub of the arcs will be connected to the substrate pad through solder. Through mechanical simulations and experiments, it is seen that the interconnects will have a compliance that is several orders of magnitude greater than the compliance of typical solder bump interconnects. Through parallel electrical paths, the developed interconnects have high mechanical compliance without compromising their electrical performance. Based on this study, it appears that multi-path fan-shaped interconnects could potentially offer a new suite of compliant interconnects for microelectronic systems.

Although the proposed interconnects can be used as die-to-substrate first-level interconnects or substrate-to-board second-level interconnects, most of the ensuing discussion is primarily focused on die-to-substrate interconnects. However, the discussion can be generalized and applied to substrate-to-board interconnects as well. In this report, we present results from two fabrication approaches for the multi-path interconnects: Domed interconnects and legged interconnects.

2.0 FABRICATION OF DOMED MULTI-PATH INTERCONNECTS

Fig. 2.1 shows the SEM images of fabricated domed interconnects at 100-um pitch. As seen, the interconnects can have four, three, or two arcs to create parallel electrical paths. The center pad is used for solder assembly of the interconnect to the substrate pad. The die pads are not fabricated in this version of the interconnects. The die pads can be either circular encompassing the entire interconnect footprint or annular touching the legs of the interconnect.
Fig. 2.2 presents the fabrication steps where the interconnects are fabricated on a silicon wafer and the legs of the interconnects make contact to an annular pad on the die.

Figure 2.2 Sequential Fabrication Steps for 3-Arc Interconnect with an Annular Pad
Figure 2.3: Fabrication Steps for Domed Interconnect
Figure 2.3 illustrates a cut-section highlighting the various fabrication steps. Starting with a wafer with annular pads and patterned resist, as illustrated in Figure 2.3a, the resist is reflowed in an oven (or on a hotplate) to generate the dome profile shown in Figure 2.3b. A metallization seed layer of titanium and copper (Figure 2.3c) is then sputtered over the wafer for electroplating the compliant structure. The titanium layer ensures adhesion of the sputtered copper layer to the annular copper pad to improve its structural integrity. Following the metallization step, two paths of approach are illustrated in Figure 2.3d for patterning the interconnect geometry. Path 1 employs photoresist spinning which generally tends to create a fairly even surface, while Path 2 employs spray coating whereby the resist is aerosolized and sprayed on the wafer to create a conformal coating. The reasons for the two process paths are discussed in the following paragraph. The photoresist is then patterned as in Figure 2.3e, and the interconnect is then plated up as in Figure 2.3f. Upon electroplating, a third layer resist is spun to define the mold cavity for electroplating the solder as shown in Figure 2.3g. Solder is then electroplated as shown in Figure 2.3i. This completes the buildup process for the interconnects. The next step is to release the structures to make them free-standing. First, the top two resist layers are stripped away using an appropriate stripper and then the copper/titanium seed layer is etched using an etchant with good selectivity between copper and solder. This exposes the underlying polymer dome which is then etched away to reveal the free standing structure shown in Figure 2.3j. The last step which is the reflow of the plated solder shown in Figure 2.3k is an optional step. Unlike stencil printed solders, plated solder has enough mechanical rigidity and will adhere to the pad without the need for reflowing.

With spin coating of photoresist under Path 1 in Figure 2.3d, the height of photoresist for exposure is non-uniform. This is because the height of the resist above the dome is lower than the height of the resist at the base of the dome. This difference in height causes a non-uniform intensity dosage of the resist during UV exposure, resulting in uneven width of the arcuate legs from the center to the annular pad. This uneven exposure can be addressed through several approaches such as intentionally designing a varying width for the arcuate structures, making the photoresist layer much thicker compared to the dome height and thus making the effect of uneven exposure minimal, or by stitch masks to provide different exposure intensity in different parts of the interconnect. Alternatively, the spray coating approach provides conformal uniform resist thickness over the dome, and thus can address the intensity variation issue. Figure 2.4 shows the SEM images of the interconnect fabricated through the two approaches.

![Figure 2.4 a) Sample fabricated by spin coating (arcs are wider near the center pad). b) Spray coated sample shows more consistent width](image-url)
3.0 FABRICATION OF LEGGED INTERCONNECT

Fabrication of the legged compliant free standing structure, without the dome, is achieved through the use of photolithography, electroplating and molding (LIGA) processes [Becker, 1986]. This LIGA-like fabrication technique utilizes photosensitive polymers to create molds in which the free standing compliant interconnects will be electrodeposited. Figure 3.1 shows the processing steps required for the fabrication of a dual-path, single-anchor interconnect. A) The process begins with a wafer with etched passivation layer to expose the copper pad. B) A metal seed layer of Ti/Cu/Ti is then blanket sputtered over the wafer for electroplating. C) A layer of photoresist is then spun and patterned over the seed layer to create a mold for the vertical post of the interconnect. Then using a high acid electroplating solution, a vertical copper post is plated. The high acid content increases the throwing power of the plating solution thereby improving plating uniformity [Newton, 1998]. D) Following this, a second seed layer of Ti/Cu is sputtered. E) A second photoresist is then spun and patterned over the seed layer to create a mold for the parallel-path arcuate beams. F) Using the same copper plating bath, the arcuate beams are plated. G) Interface materials such as nickel and gold can then be optionally plated over the copper arcuate beams. E) Finally, the free standing compliant structure is released from the mold by stripping the photoresist and etching the seed layers.

Figure 3.1: Fabrication steps for dual-path interconnect
The purchased 4 inch wafers did not have pre-existing copper pads for compliant interconnect fabrication. Therefore, the fabrication steps outlined in Figure 3.1 were augmented to include the fabrication of copper pads and the passivation layer. Accordingly, the actual fabrication process started with a blank 4 in. diameter silicon wafer with a thickness of 550 μm. A titanium/copper/titanium seed layer 30/100/30 nm thick was first blanket sputtered on top of this silicon wafer. A 2 μm thick SiO₂ passivation layer was then deposited using plasma enhanced chemical vapor deposition (PECVD) on the wafer. A 4 μm thick photoresist layer was then spun and patterned over the passivation layer. The photoresist doubled as an etch mask to open up the passivation layer and also to create a mold for electroplating the vertical post. An isotropic wet etch process using buffered oxide etch (BOE) was used to open the passivation layer. The cross-section of the opening is 10 μm by 10 μm. Electroplating was then carried out in a copper sulfate plating bath until the columns were about level with the photoresist surface. To make the plating process predictable, a strip of copper with an area much greater than the features on the wafer was attached to the back of the wafer. The current density used for the plating process was 2 mA/cm². Higher current densities up-to 4 mA/cm² were tested. However, the resulting joule heating at the contacts made them unsuitable for plating. A second seed layer of titanium/copper 30/100 nm thick was then blanket sputtered over the wafer in preparation for plating the arcuate beams. Following this, a second photoresist layer, 8 μm thick was then spun and patterned over the seed layer. Using the same plating conditions, the arcuate beams were plated with copper. No interface metal was plated on top of copper. To release the structure, the second layer (topmost) photoresist was first stripped using acetone. This was followed by a flash etch of the top seed layer using aluminum etchant/BOE to strip the copper/titanium layers respectively. The bottom photoresist layer which now lies beneath the arcuate beams was stripped in a bath of acetone using an ultrasonic bath. Agitation was needed to release portions of the photoresist trapped under the arcuate beams.

**Figure 1.2: SEM Images of Intermediate Fabrication Steps:**
(A) 1st layer photoresist with 2nd seed layer
(B) Partially plated post
(C) Released free-standing interconnects

On a 4 in. wafer, there were twelve 20 mm x 20 mm dies. For each die, there were three rows of peripheral interconnects at a pitch of 100 μm. A close-up image of one of such interconnect is shown in Fig. 3.3a. Fig. 3.3b shows an array of fabricated interconnects.
4.0 THERMO-MECHANICAL MODELING

To understand the thermo-mechanical behavior of the interconnects in a packaging configuration, finite-element simulations were carried out. The simulations were done using ANSYS® 12.1. A 20 x 20 mm flip chip on a 22 x 22 mm organic substrate with 40,000 area-array interconnects at 100 μm pitch was used in this study. As a full 3D model would be computationally expensive and as a 2D model would not be able to capture the arcuate structures appropriately, a 2.5D generalized plane deformation (GPD) model was used. A GPD model combines the features of 2D and 3D models such that the arcuate beams are geometrically modeled in their entirety, while one row of interconnects is modeled as in 2D models. Figure 4.1 shows the finite-element mesh of the GPD model. The width of the GPD model is the pitch of the interconnects and is equal to 100 μm. Due to symmetry, one half of the packaging assembly was modeled, and thus the length of model was 10 mm for the die and 11 mm for the substrate. The cut section used in this model was parallel to one of the edges of the package. The thickness of the die was 550 μm and the thickness of the substrate was 800 μm. Table 4.1 summarizes the dimensions of the package used in the simulations.

4.1 MATERIAL MODELS

The copper interconnect was modeled as an isotropic, linear elastic and kinematically hardening material. The silicon die was modeled as an isotropic, linear elastic material with a modulus of 121 GPa and coefficient of thermal expansion (CTE) of 3 ppm/K. The substrate intended for use in the assembly is a single layer, low CTE type substrate with a CTE value of 11 ppm/K. The substrate was modeled as an orthotropic, temperature-dependent and linear elastic material. The lead-free tin-silver Ag3.5Sn solder was modeled as a multi-linear kinematically hardening viscoplastic material.
4.2 THERMO-MECHANICAL LOADING

The applied load is in the form of temperature cycling consistent with JEDEC (JESD22-A104D-J) standards [JEDEC, 2009]. The melting temperature of Ag3.5Sn solder, 220 °C, was assumed to be the stress-free temperature of the assembly. Starting from this temperature, the entire assembly was simulated to be cooled down to room temperature. After dwelling for 60 minutes at room temperature, the assembly was simulated to be thermally cycled between 100 and 0 °C with a 5 °C/min ramp rate and 5 min dwells at high and low temperatures. Thus, each simulated thermal cycle lasted 50 minutes.

4.3 THERMO-MECHANICAL RELIABILITY

Using a Coffin-Manson type equation (4.1) for the life prediction of electroplated copper, the fatigue life of the interconnect was calculated [Ianuzelli, 1991]. This model utilizes plastic strain range, $\Delta \varepsilon_p$, as the damage metric. Other parameters are $N_f$, which represents the mean life to fatigue failure and, $\varepsilon_f$, which is the fatigue ductility coefficient having values ranging between 0.15 and 0.3 [Prahbu et al., 1995]

$$N_f^{-0.6} \varepsilon_f^{0.75} = \Delta \varepsilon_p \quad (4.1)$$
It took three cycles to attain a stabilized hysteresis loop. The accumulated plastic strain range from the last cycle was used to compute the fatigue life of the interconnects. It was seen that the maximum strain occurred in the arcuate section of the compliant interconnect, as designed and intended. This is shown in Figure 4.2. The highlighted elements in the insert represent the most stressed region and hence the failure point of the interconnect. Based on the maximum plastic strain range (0.00420), the mean fatigue life of the interconnects was computed to be more than 1400 thermal cycles using equation (4.1). For these computations, the ductility coefficient was taken to be 0.225 which is the average of 0.15 and 0.3.

In addition to compliant interconnect strains, die and substrate stresses were also obtained from the simulation. It was seen that the maximum principal stress at the back of the die was about 5.61 MPa, which is at least one order of magnitude less than the stress in an underfilled solder bump flip-chip assembly [Michaelides and Sitaraman, 1999]. The substrate stress was found to be 1.42 MPa. Figure 4.3 shows the principal stresses in the assembly.

As seen, the die stresses as a result of the thermal excursion is very low. This implies that the low-K materials in current and future dies will not crack or delaminate, when compliant interconnects are used.
5.0 ELECTRICAL MODELING OF LEGGED INTERCONNECTS

As discussed earlier, the 2-Arc Fan, has two electrical paths, similar to the dual-path interconnect discussed thus far. However, unlike that single-anchor, dual-path compliant interconnect where the die pad and the substrate pad are offset laterally and where the arc-like structures are supported by a single leg, the 2-Arc Fan has the die pad and the substrate pad laterally aligned. Also, the 2-Arc Fan has two posts connecting to the die pad, and thus will provide two parallel paths and the associated redundancy for electrical connection (Figure 5.1).

Figure 5.1: 2-Arc Fan with second-order splines: 3-D rendering (left) and top view (right)

The 3-Arc Fan and 4-Arc Fan interconnects, as illustrated in Figure 5.2 and Figure 5.3, respectively, add more electrical paths and thus additional redundancy.

Figure 5.2: 3-Arc Fan with second-order splines: 3-D rendering (left) and top view (right)

Figure 5.3: 4-Arc Fan with second-order splines: 3-D rendering (left) and top view (right)

It should be pointed out that the arcs in 2-Arc, 3-Arc, and 4-Arc Fan interconnects are second-order splines. The width, thickness, length, and number of arcuate structures influence the mechanical compliance of the interconnects. In general, narrower, thinner, and longer arcuate
structures result in higher compliance. When comparing the compliance of one structure against a different one, it is also important to ensure the electrical parasitic are kept constant against different structures, and thus, when the number of arcuate structures increase, it will be necessary to scale down the cross-section area of each arcuate structure so that the total cross-section area remains the same for different interconnects. On the other hand, the length of each arcuate structure for a 4-Arc structure will be less than the length of each arcuate structure for a 2-Arc structure to accommodate the geometry within a given footprint and to ensure that the arcuate structures do not touch one another during deformation. Thus, care should be exercised when comparing the electrical and mechanical performance characteristic of the different designs.

FastHenry™ was used to calculate the equivalent R and L of each interconnect. The R and L between the top of the solder and the far end of vertical posts were calculated. Figure 5.4 shows how multiple legs were modeled by extracted R and L with top and side views. The far end of multiple vertical posts were assumed to have an equal potential in FastHenry™, and then the R and L between the top of the solder and the far end of one vertical post were calculated. As a result, all legs were taken into account when calculating the R and L. Yellow dotted rectangle in Figure 15(b) is an example of the cross-sectional area of one leg. As the number of legs is 2, the total cross-sectional area will be two times the cross-sectional area of individual leg. In the 4-Arc Fan interconnect, the width and height of the legs were scaled down so as to keep the total cross-sectional area of legs the same with the 2-Arc Fan interconnect. In the case of the 3-Arc Fan interconnect, for fabrication and other considerations, the total area was made to be approximately the same as the other two designs; however, the total cross-sectional area was slightly greater than those of the 2- and 4-Arc Fan interconnect.

![Figure 5.4. 2-Arc Fan interconnect (a) top view, (b) side views](image)

In Table 5.1, a list of the frequency-dependent R and L values of the 2-Arc Fan interconnect is shown along with the top view of the interconnect. In the same manner, the simulated values of the 3- and 4-Arc Fan interconnects are shown in Tables 5.2 and 5.3, respectively.
### Table 5.1. R and L values of 2-Arc Fan interconnect

<table>
<thead>
<tr>
<th>Frequency</th>
<th>R Ω</th>
<th>L (H)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10Hz</td>
<td>0.018956</td>
<td>6.97898e-011</td>
</tr>
<tr>
<td>100Hz</td>
<td>0.018956</td>
<td>6.97898e-011</td>
</tr>
<tr>
<td>1KHz</td>
<td>0.018956</td>
<td>6.97898e-011</td>
</tr>
<tr>
<td>10KHz</td>
<td>0.018956</td>
<td>6.97898e-011</td>
</tr>
<tr>
<td>100KHz</td>
<td>0.018956</td>
<td>6.97898e-011</td>
</tr>
<tr>
<td>1MHz</td>
<td>0.0189561</td>
<td>6.97897e-011</td>
</tr>
<tr>
<td>10MHz</td>
<td>0.0189626</td>
<td>6.97839e-011</td>
</tr>
<tr>
<td>100MHz</td>
<td>0.0194449</td>
<td>6.9484e-011</td>
</tr>
<tr>
<td>1GHz</td>
<td>0.0331785</td>
<td>6.68557e-011</td>
</tr>
<tr>
<td>10GHz</td>
<td>0.0859992</td>
<td>6.39715e-011</td>
</tr>
<tr>
<td>100GHz</td>
<td>0.156211</td>
<td>6.33373e-011</td>
</tr>
</tbody>
</table>

### Table 5.2. R and L values of 3-Arc Fan interconnect

<table>
<thead>
<tr>
<th>Frequency</th>
<th>R Ω</th>
<th>L (H)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10Hz</td>
<td>0.0144764</td>
<td>4.34317e-011</td>
</tr>
<tr>
<td>100Hz</td>
<td>0.0144764</td>
<td>4.34317e-011</td>
</tr>
<tr>
<td>1KHz</td>
<td>0.0144764</td>
<td>4.34317e-011</td>
</tr>
<tr>
<td>10KHz</td>
<td>0.0144764</td>
<td>4.34317e-011</td>
</tr>
<tr>
<td>100KHz</td>
<td>0.0144764</td>
<td>4.34317e-011</td>
</tr>
<tr>
<td>1MHz</td>
<td>0.0144765</td>
<td>4.34316e-011</td>
</tr>
<tr>
<td>10MHz</td>
<td>0.0144811</td>
<td>4.34257e-011</td>
</tr>
<tr>
<td>100MHz</td>
<td>0.0147744</td>
<td>4.31565e-011</td>
</tr>
<tr>
<td>1GHz</td>
<td>0.022242</td>
<td>4.18707e-011</td>
</tr>
<tr>
<td>10GHz</td>
<td>0.0584109</td>
<td>4.00766e-011</td>
</tr>
<tr>
<td>100GHz</td>
<td>0.111834</td>
<td>3.9625e-011</td>
</tr>
</tbody>
</table>

### Table 5.3. R and L values of 4-Arc Fan interconnect

<table>
<thead>
<tr>
<th>Frequency</th>
<th>R Ω</th>
<th>L (H)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10Hz</td>
<td>0.0106443</td>
<td>2.48997e-011</td>
</tr>
<tr>
<td>100Hz</td>
<td>0.0106443</td>
<td>2.48997e-011</td>
</tr>
<tr>
<td>1KHz</td>
<td>0.0106443</td>
<td>2.48997e-011</td>
</tr>
<tr>
<td>10KHz</td>
<td>0.0106443</td>
<td>2.48997e-011</td>
</tr>
<tr>
<td>100KHz</td>
<td>0.0106443</td>
<td>2.48997e-011</td>
</tr>
<tr>
<td>1MHz</td>
<td>0.0106444</td>
<td>2.48997e-011</td>
</tr>
<tr>
<td>10MHz</td>
<td>0.0106481</td>
<td>2.48941e-011</td>
</tr>
<tr>
<td>100MHz</td>
<td>0.0108524</td>
<td>2.46506e-011</td>
</tr>
<tr>
<td>1GHz</td>
<td>0.0147444</td>
<td>2.39755e-011</td>
</tr>
<tr>
<td>10GHz</td>
<td>0.0406033</td>
<td>2.29088e-011</td>
</tr>
<tr>
<td>100GHz</td>
<td>0.104923</td>
<td>2.26312e-011</td>
</tr>
</tbody>
</table>
For example, at 10GHz, the R decreases from 86mΩ to 58.4mΩ and 40.6mΩ as the number of leg increases from 2 to 3 and 4, respectively. Also, the L decreases from 64pH to 40.1pH and 22.9pH. Both R and L of the interconnect scale with the number of legs, as shown in Figure 5.5. The 4-Arc Fan interconnect has the least parasitic resistance and inductance, as expected.

![Figure 5.5. Decrease in electrical parasitic with the number of legs](image)

The electrical performance of the interconnects was compared at 10, 20, and 40GHz, as shown in Table 5.4. The values in the first 5 rows are from FastHenry™ and CST Microwave Studio™, which is a full-wave commercially available simulator from Computer Simulation Technology. Using the following example values, the other parameters in Table 5.4 were computed:

- Length of the die side = 20mm
- Pitch between interconnects = 200um
- Number of interconnect per side = 98
- Total number of interconnect = 388
- Zo = 50Ω
- Supply voltage for the die = 2.5V

### Table 5.4. Electrical performance

<table>
<thead>
<tr>
<th># of legs</th>
<th>2</th>
<th>3</th>
<th>4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Freq.</td>
<td>10GHz</td>
<td>20GHz</td>
<td>40GHz</td>
</tr>
<tr>
<td>R</td>
<td>8.600E-02</td>
<td>1.098E-01</td>
<td>1.324E-01</td>
</tr>
<tr>
<td>S_{II}</td>
<td>-1.447E-02</td>
<td>-3.715E-02</td>
<td>-1.202E-01</td>
</tr>
<tr>
<td>I/pin</td>
<td>5.000E-02</td>
<td>5.000E-02</td>
<td>5.000E-02</td>
</tr>
<tr>
<td>ΔV_{dc}</td>
<td>4.300E-03</td>
<td>5.489E-03</td>
<td>6.618E-03</td>
</tr>
<tr>
<td>cross-area/leg</td>
<td>1.280E-04</td>
<td>1.280E-04</td>
<td>1.280E-04</td>
</tr>
<tr>
<td>J_{smax}</td>
<td>1.953E+02</td>
<td>1.953E+02</td>
<td>1.953E+02</td>
</tr>
<tr>
<td>t</td>
<td>1.000E-11</td>
<td>5.000E-12</td>
<td>2.500E-12</td>
</tr>
<tr>
<td>di/dt</td>
<td>5.000E+09</td>
<td>1.000E+10</td>
<td>2.000E+10</td>
</tr>
<tr>
<td>L·di/dt</td>
<td>3.199E-01</td>
<td>6.364E-01</td>
<td>1.269E-01</td>
</tr>
<tr>
<td>ΔV</td>
<td>3.242E-01</td>
<td>6.419E-01</td>
<td>1.275E+00</td>
</tr>
</tbody>
</table>

Table 5.4. Electrical performance
In these simulations, all the interconnects were assumed to be used as I/O connections. Current per pin was calculated by dividing the supply voltage by the line impedance: \(2.5/50=50\text{mA}\). Using the equivalent R (3rd row), the DC drop, \(\Delta V_{\text{DC}}\) could be calculated. The 2-Arc Fan interconnect induces twice as much DC drop as compared to the 4-Arc Fan interconnect. In the 8th row, the cross-sectional area per leg was calculated by multiplying the width and height of each leg. Then, the current density per leg could be calculated. This row was used to make sure that the interconnect would not suffer from electromigration-related problems due to excess current density. Since the threshold value of electromigration is \(1.5 \times 10^{11} \text{A/m}^2\) from the published literature, all three interconnect designs were found to be safe. In the 10th row, the rise time was assumed to be one-tenth of the signal period. At 10GHz, the period is 0.1ns, and thus, the rise time equals 0.01nsec. Then, \(\text{di/dt}\) can be calculated along with \(L\cdot\text{di/dt}\), which is the inductive potential drop. As the equivalent \(L\) of the 2-Arc Fan interconnect is twice the equivalent \(L\) of the 4-Arc Fan interconnect, the inductive potential drop for the 2-Arc Fan interconnect is also about twice the inductive potential drop for the 4-Arc Fan interconnects. Consequently, the 4-Arc Fan interconnect has the least total voltage drop among all interconnect designs, as shown in the last row.

6.0 MECHANICAL COMPLIANCE TESTING

Mathematically, the compliance of a structure is the inverse of its stiffness otherwise known as the spring constant. A benefit of the low stiffness is that the compliant interconnects can accommodate the differential displacement incurred between the die and the substrate under thermal excursions of the packaged die assembly. Thus, a mechanically compliant interconnect will be able to decouple the die from the substrate and will result in lower stresses in the die.

The mechanical compliance characterization of the interconnects was performed using a Hysitron tribo-indenter equipped with a Berkovich tip and a load head capable of applying up to 9 mN. An illustration of the test setup is shown in Figure 6.1. The load head through the tool tip applies a downward force by gradually increasing the displacement of load tip while recording the reactionary force on the load cell as a function of displacement.

![Image](image_url)

Figure 6.1: a) Tribo-indenter for mechanical compliance testing b) Schematic showing the force direction on the compliant interconnect
Interconnects with “High,” “Medium,” and “Low” compliance values were fabricated. The purpose of such varying compliance is that on a given chip, the outermost interconnects need the maximum compliance, while the interconnects near the center of the chip need the minimum compliance and the in-between interconnects will have “medium” compliance. Such a heterogeneous arrangement of interconnects will have an increasing compliance from the center of the die to the edge of the die, and will facilitate to tailor the electrical parasitics accordingly from the center to the edge of the die, as discussed in Section 8.0. Figure 6.2a shows load vs. displacement plot of a “High” compliance interconnect. Using the region of plot marked by the blue arrow, the compliance (inverse of the slope of the curve) of the High compliance interconnect was determined to be about 7 mm/N. Similarly Figures 6.2b and 6.2c show the experimentally-measured compliance of Medium and Low compliance interconnects to be about 5 mm/N and 2 mm/N.
Similar to the 3-arc compliant interconnects, the out-of-plane mechanical compliance of the dual-path compliant interconnects was measured using a nano-indenter. As illustrated in Fig. 6.3, the wafer with compliant interconnects was fixed on the nanoindenter table and the nano-indenter tip was used to apply a downward force to the center pad of the interconnect. The resulting displacement and the corresponding load on the indenter tip were then recorded.

Captured in Fig. 6.4 is one of such load-displacement curves from a number of compliance tests conducted.
The slope of the force-displacement curve in Fig. 6.4 gives the stiffness of the interconnect. The inverse of the slope gives an out-of-plane compliance of about 2.80 mm/N.

6.1 NUMERICAL DETERMINATION OF MECHANICAL COMPLIANCE

In addition to experimental measurements, a finite-element model was built to determine the mechanical compliance of the dual-path interconnect. As a first step, the dimensions of the fabricated interconnect were measured for modeling purposes. This is because the designed dimensions are invariably different from the fabricated dimensions due to various process steps including exposure and development as well as electroplating and etching. By design, the dimensions of the interconnect beams are 4 µm wide x 8 µm deep. However, the pattern transfer during the lithography steps resulted in a slightly wider beam than designed. The depth or thickness of the beam and the supporting post are also greater than the designed thickness due to overplating. The image in Fig. 6.5 shows dimensions of the widest and narrowest portions of the fabricated beam. These measurements of 5.67 µm and 7.67 µm were averaged over their respective lengths to give a mean width of 6.0 µm. The post height (stand-off height) and the beam thicknesses were also measured to be 9 µm and 8.3 µm respectively.

Using the measured dimensions, a finite-element model was created. In this model, the compliant interconnect was constrained at the bottom of the post to mimic the experiments, and a downward force was applied to the node in the central portion of the center pad. The downward displacement of the center pad where the force was applied was tracked. As the force increased from 1 µN to 450 µN, it was seen that the displacement increased linearly, as in experiments, and the out-of-plane compliance was computed from the force versus displacement diagram. The calculated compliance from the finite-element model (Fig. 6.6) was 2.16 mm/N.
7.0 DROP TESTING

In addition to studying the thermo-mechanical and electrical behavior of the compliant interconnects, the performance of the interconnects under drop impact loading was also studied. An InstronDynatup® 8250 drop weight impact tester was used to conduct the drop tests. The Instron machine was suitably modified to accommodate drop testing. A custom drop test fixture which mimics a drop table was designed and fabricated using impact-resistant steel. This fixture was designed to house the drop test sample inside it and would serve as the drop table needed for mounting the test sample. The fixture was bolted onto the crosshead of the Instron machine, as shown in Fig. 7.1, and could be freely raised or lowered using the crosshead movement controls of the Instron drop weight tester.

Stand-off screws were used to raise the board above the drop test surface inside the fixture. Hex screws were used to bolt the board onto the stand-off screws. The stand-off screws allowed the board to flex during the drop test, which is known to be the primary reason for interconnect failure during drop [Seah, 2002]. Strain was used as a metric for determining the effect of the drop test on the mounted sample. A linear 1-axis strain gauge (Gauge Factor 2.09) was attached directly on top of the free surface of the board. A bi-axial tee-roseette strain gauge (Gauge Factor 2.1) was attached on the polymer die, directly opposite the linear 1-axis strain gauge at the center of the die. In addition, a unidirectional piezoelectric accelerometer was mounted next to the linear 1-axis strain gauge, to measure the input acceleration as well as the
impact pulse generated during the actual drop event. The information from the accelerometer was used to generate input boundary conditions necessary to conduct finite element simulations using the Input-G method. The gauge and accelerometer positions and orientations are shown in Fig. 7.2.

![Diagram](image)

**Figure 7.2: Accelerometer and strain gauge positions and orientations- (a) Accelerometer and Linear single-axis strain gauge mounted on board (top view), (b) Side view of mounted accelerometer and strain gauges, and (c) Bi-axial Tee-rosette strain gauge mounted on die (bottom view)**

In Fig. 7.2, SG1 refers to the linear 1-axis strain gauge attached on the board parallel to the planar $X$ direction, along the length of the board. SG2 and SG3 together refer to the bi-axial tee-rosette strain gauge attached at the center of the die. SG2 is parallel to the planar $X$ direction, while SG3 is parallel to the planar $Z$ direction. The accelerometer is mounted next to SG1. This layout of strain gauges and accelerometers was used for all the samples during the experimental drop tests. As the objective was to determine how well the interconnects are able to isolate the die from the substrate, 75 times scaled-up polymer prototypes, fabricated using stereolithography, were used in this study. The prototypes consisted of a 3x3 compliant interconnect array sandwiched between a die and a substrate. Fig. 7.3 shows the strain data plots calculated from the strain output data recorded by the strain gauges for different drop heights (100mm, 300mm and 500mm). In the strain data plots, SG1 represents the linear 1-axis strain gauge along the $X$ direction mounted on the free surface of the board; SG2 refers to the tee-rosette strain gauge along the longitudinal axis ($X$ direction) mounted at the center of the die and SG3 refers to the tee-rosette strain gauge along the width ($Z$ direction) mounted at the center of the die. The data shown was normalized and filtered using a 1000Hz low-pass filter, which was deemed sufficient to filter the high frequency scatter and noise. Table 7.1 shows the microstrain values for different drop heights for all the strain gauges mounted on the drop test samples.
Figure 7.3: Strain data plots for three-arc compliant interconnect drop test experiments
Table 7.1: Microstrain values for 3-arc interconnect for different drop heights

<table>
<thead>
<tr>
<th>Drop Height (mm)</th>
<th>SG1</th>
<th>SG2</th>
<th>SG3</th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td>2226</td>
<td>312</td>
<td>250</td>
</tr>
<tr>
<td>200</td>
<td>3964</td>
<td>495</td>
<td>305</td>
</tr>
<tr>
<td>300</td>
<td>4291</td>
<td>879</td>
<td>692</td>
</tr>
<tr>
<td>400</td>
<td>5673</td>
<td>1006</td>
<td>646</td>
</tr>
<tr>
<td>500</td>
<td>5774</td>
<td>1008</td>
<td>562</td>
</tr>
<tr>
<td>600</td>
<td>6258</td>
<td>1069</td>
<td>441</td>
</tr>
</tbody>
</table>

Based on the values given in Table 7.1, the strain in the board, SG1, can be seen to monotonically increase as the drop height increases from 100mm to 600mm. The strain in the die along the longitudinal direction, given by SG2, was found to increase for drop heights 100mm to 400mm, after which the microstrain values were fairly constant around 1000. The strain in the die along the transverse direction, recorded by SG3 was reported as nearly half that of SG2. It was gathered that the board strains are heavily dependent on the drop height. The die strains (SG2 and SG3) seem to be much smaller in magnitude compared to SG1. This was attributed to the effect of the three-arc compliant interconnects, which were able to absorb and thus damp most of the strain that was being transferred from the board to the die. If the ratio of the board to die strain was calculated, the ratio was averaged at 5.85: 1. The three-arc compliant interconnects were able to isolate the impact and reduce the strain in the die by a factor of approximately 6 compared to the strain in the board.

7.1 DROP TESTING SIMULATION

For the purpose of conducting drop test simulations, the Input-G method was selected, which makes use of an implicit method to simulate a drop test. In this technique, the impact acceleration recorded from experimental drop tests is converted to displacement boundary conditions. The calculated displacement is then applied at the supports, taking into account the impulse time of the drop [Luan, 2004].

Figure 7.4: Three-arc Compliant Interconnect Model for Drop Test Simulation

The finite element simulations were carried out using the ANSYS® Implicit solver. A 3x3 array of scaled up compliant interconnects was created with die and assembly as shown in Fig. 7.4, which shows a close up of the exposed three-arc compliant interconnect array. The model geometry was designed to closely mimic the drop test samples used for experimental
testing. The model used for simulation was created using SOLID185 elements. A total of 66859 elements were used to create the model. The polymer material used to fabricate the experimental drop test samples was modeled in the simulation as a linear elastic material with a modulus of elasticity of 2.282GPa, a Poisson’s ratio of 0.3 and a density 1180 Kg/m3. Fig. 7.4 shows the simulated strain plots for the compliant interconnects for various drop heights. Table 7.2 compares the microstrain values recorded from both experiment and simulation. Both experiments and simulation showed significantly lower strains in the die than that observed in the board. The simulation results were found to report monotonically increasing strains in the board (SG1), ranging from 2754 microstrain for a drop height of 100mm to 5026 microstrain for a drop height of 500mm. These values were found to be in close relation with the experimentally reported microstrain values of 2256 microstrain for 100mm drop height to 5774 microstrain for 500mm drop height.

![Strain data plots for three-arc compliant interconnect drop test simulations](image)

(a) 100 mm drop height strain data

(b) 300 mm drop height strain data

(c) 100 mm drop height strain data

**Figure 7.5: Strain data plots for three-arc compliant interconnect drop test simulations**
Table 7.2: Comparison of microstrain values – experiments and simulation

<table>
<thead>
<tr>
<th></th>
<th>Drop Height (mm)</th>
<th>100</th>
<th>300</th>
<th>500</th>
</tr>
</thead>
<tbody>
<tr>
<td>SG1</td>
<td>Experimental</td>
<td>2256</td>
<td>4291</td>
<td>5774</td>
</tr>
<tr>
<td></td>
<td>Simulation</td>
<td>2754</td>
<td>4675</td>
<td>5026</td>
</tr>
<tr>
<td>SG2</td>
<td>Experimental</td>
<td>312</td>
<td>879</td>
<td>1008</td>
</tr>
<tr>
<td></td>
<td>Simulation</td>
<td>257</td>
<td>504</td>
<td>689</td>
</tr>
<tr>
<td>SG3</td>
<td>Experimental</td>
<td>250</td>
<td>692</td>
<td>562</td>
</tr>
<tr>
<td></td>
<td>Simulation</td>
<td>201</td>
<td>302</td>
<td>442</td>
</tr>
</tbody>
</table>

On comparing the die strains, it was observed that the die strains (SG2 and SG3) were reported to be lower than board strain (SG1) in both experiments and simulations. A close relation was observed between experimental and simulation microstrain values. These results gave evidence of the strong decoupling effect of the compliant interconnects, while proving that the compliant nature of the interconnects reduced strain transfer from the board to the die.

8.0 HETEROGENEOUS INTERCONNECTS

Although the compliant interconnects are able to mechanically decouple the die from the substrate and thus reduce the stresses induced in the die, the interconnects have higher electrical parasitics compared to solder bumps. As discussed earlier, the various designs studied in this project such as 2-arc, 3-arc, and 4-arc interconnects as well as dual-path single-anchor interconnect have different electrical parasitics and mechanical compliance. Based on this study, it is seen that the 3-arc interconnects offer a good compromise between mechanical performance and electrical parasitics. However, it is not necessary to have the same level compliance throughout an entire die, as the interconnects near the die corner undergo maximum differential displacement due to CTE mismatch, while the interconnects near the die center undergo minimum differential displacement, and thus, the interconnects near the corner/edge can be designed to have maximum mechanical compliance, while the interconnects near the die center can be designed to have minimum mechanical compliance. The interconnects that are situated between the center region and edge region can be designed to have a compliance that is “medium.” Such a heterogeneous array of interconnects will be beneficial from an electrical perspective as well. Typically, when mechanical compliance is reduced by making the arc widths greater, the electrical parasitics are also reduced, and vice versa. Thus, it is possible to have the center interconnects with low mechanical compliance and lower electrical resistance can be used as power and ground interconnects, while the interconnects near the edge/corner can serve as signal interconnects. Such a heterogeneous arrangement can be achieved through a single mask step, as the only parameter that is changed is the width and length of the arcs of the interconnects. Figure 8.1 shows one such heterogeneous array of fabricated 3-arc interconnects.
9.0 EDUCATION ACTIVITIES

- Three PhD students – two in Mechanical Engineering (ME) and one in Electrical and Computer Engineering (ECE) – have worked on this project. One ME PhD student has gained valuable experience in cleanroom fabrication and characterization of compliant interconnects. The other ME PhD student has gained experience in theoretical modeling of compliant interconnects. The ECE PhD student has gained valuable experience in electrical modeling and simulation of the compliant interconnects.
- Of the three PhD students, one ME PhD student is an African American, while the ECE PhD student is a woman. Thus, the project is training students from under-represented groups toward their doctoral research.
- One MS student – in Mechanical Engineering – has worked on the dynamic simulations and drop testing of the compliant interconnects. The student has contributed toward understanding the reliability of the interconnects under drop testing.
- Three undergraduate students – one in Mechanical Engineering, recently graduated, and the other two in Electrical and Computer Engineering – have worked on mechanical design and compliance of the structures as well as the mask design and electrical simulation of the structures.
By mentoring the undergraduate students, the graduate students gain valuable mentoring experience.

Compliant interconnects were discussed and presented in the Undergraduate ECE/ME/MSE cross-listed course 4754 Electronic Packaging and Assembly in Spring 2010, Spring 2011, and Spring 2012, and students got exposed to compliant interconnect technology as part of this course. Also, student groups from the graduate-level ME 6124 – Finite-Element Method: Theory and Practice did a project on compliant interconnects in Spring 2010, Spring 2011, and Spring 2012. In addition, material from the research was also discussed in the graduate-level ME/ECE/MSE 6776 - Microelectronics Systems Packaging. Thus, the compliant interconnects were introduced in three courses – one undergraduate and two graduate.

The material from this project is routinely presented in industry meetings and other avenues to be able to reach a wider audience.

PhD student – Raphael Okereke – won the First Place, 2010 Student Poster Competition, The Electronic and Photonic Packaging Division, ASME 2010 International Mechanical Engineering Congress and Exposition (IMECE2010), November 2010, Vancouver, British Columbia, Canada; for the poster titled, “Parallel-Path Compliant Structures as Electrical Interconnects.” Also, he won the 1st Place Best Student Paper (Poster) award at the Global Interposer Technology Workshop, Nov. 2012 for the poster entitled, “Mechanically Compliant Single-Path and Multi-Path Electrical Interconnects.”

10.0 SUMMARY

A comprehensive inter-disciplinary program is underway in the area of compliant interconnects. A wide range of interconnect geometries have been designed, and their electrical and thermo-mechanical characteristics are being assessed. It is seen that the fan-like interconnects with arc structures have advantages such as ease of assembly and substrate/die pad layout due to lack of lateral offset. It is also seen that the proposed interconnects have mechanical compliance that is several orders of magnitude greater than that of solder bumps, and the stresses induced in the die will not crack or delaminate low-K dielectric on the die. It is seen that the current density per leg is less than the electromigration threshold. Also, the overall electrical parameters for the interconnects are acceptable. An array of interconnects has been fabricated, and the mechanical compliance of the interconnects is several orders of magnitude greater than solder bump interconnects. Also, a heterogeneous configuration of compliant interconnects is explored. The material from the project has been integrated in classroom lectures. Also, results from the projects are disseminated through scholarly publications. Based on the results obtained thus far, additional funding has been obtained from industry to explore compliant structures for other applications.
REFERENCES