Final Report

"Radiation Analysis of SiGe HBT Devices and Circuits”

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**Abstract**

SiGe HBT technology has generated significant interest in the space community because it effectively marries high-speeds, high levels of integration, and low cost capability, and initial results suggest that SiGe has a built-in total ionizing dose (TID) immunity. Single event effect (SEE) mitigation remains a key concern for the deployment of SiGe in space. SEE analysis and understanding in SiGe HBTs (and importantly circuits) require a focused and dedicated effort, and is the subject of this proposal.

The overall goal of this program is to continue to enhance our understanding of SiGe HBTs (and particularly the circuits built from them) operating in a radiation environment such as space. We focused on a multiple of topics of importance to the space community, with continued emphasis towards more comprehensive understanding and implementation at the circuit and system level. As in the past, Cressler’s close synergy with the major suppliers of SiGe hardware (eg., IBM, Jazz, TI) will be utilized (at no cost to this effort) in the experimental studies supporting this work.

**Description of Tasks**

Georgia Tech’s research emphasis for this project is on experimentally and theoretically deepening our understanding of SEE phenomena in SiGe HBTs and the circuit built from them, and establishing best-practice techniques for mitigating various SEE phenomena in digital, analog, and RF SiGe circuits. We highly leverage our industry connections to provide early assessment of different SiGe technologies, for both devices and circuits fabricated at no cost to this project: IBM, IHP, ST Microelectronics, TI, National, Jazz, etc. Our focus is heavily circuit-relevant, and is conducted in collaboration with both the Auburn and Vanderbilt SiGe teams, and highly leverages several external radiation programs: AFOSR MURI, MDA (radar), NASA ETDP (cryo-SiGe) and NASA (radar).

Specific tasks included:

1) **Development of Mitigation Approaches for Single-Event Upset of SiGe HBT Circuits.** We continued to refine and develop best-practice approaches to SEE hardening of SiGe HBTs for high-speed digital circuits. Building on our current NASA funding, we continued to explore and develop various layout-based SEE mitigation approaches, to be verified using ion microbeam / backside laser / broadbeam heavy ions studies to monitor the resultant SEE response. We also continued to explore circuit-level RHBD approaches (e.g., improved latch designs). This effort first targeted transistor-level measurements to show merit, and then was followed by circuit-level implementations (e.g., shift registers) for ultimate broad-beam verification of our approaches.

2) **Evaluating Single-Event Transient Phenomena in SiGe HBTs and High-Speed Analog Circuits.** Ion microbeam studies have proven very useful in understanding charge collection related to heavy ion strikes in SiGe HBTs. To date, however, those measurements have been static (dc), and not dynamic in nature, and the role of single event transients in SiGe analog/mixed-signal circuits remains virtually unexplored. We built upon the last 6 months of our funded effort to demonstrate and use SiGe circuits (e.g., voltage references, operational amplifiers) of various topologies as a test-bench for assessing single-event
transients in SiGe analog/mixed-signal circuits, and mapped out key circuit-level sensitivities. SiGe references were designed which utilized varying levels of RHBD (from task 1), in order to quantify and refine best-practice approaches to RHBD in SiGe analog circuits and systems.

3) Evaluation of New SiGe Technology Platforms: We performed total-dose, ion microbeam, and laser testing of newly emergent SiGe technology platforms, at both the device and circuit level, including: IBM (8WL vs 8HP; 5PAe vs 5AM), IHP (complementary SiGe, with nnp + pnp SiGe HBTs – C-SiGe), ST Microelectronics (SiGe on SOI), Texas Instruments (C-SiGe), Jazz (new 130 nm vs 8HP) and National Semiconductor (C-SiGe).

Management Approach

Professor Cressler’s SiGe research team at Georgia Tech has a long track record of outstanding collaboration with the NASA Goddard radiation effects team (including: K. LaBel, P. Marshall, C. Marshall, R. Ladbury, et al.), as well as Auburn University (G. Niu), and Vanderbilt University (R. Reed). We will continue that collaborative mode and management path in the present effort, and will be attending all radiation experiments to assist Goddard personnel in device and circuit characterization. Beam time will be leveraged from on-going Goddard experiments, as we have done in the past.

Personnel

Professor John D. Cressler were serve as PI to this grant as before (resume below), and will be assisted by two graduate students.

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Education
B.S., Physics, summa cum laude, cooperative plan, Georgia Institute of Technology, March 1984.

University Experience
7/04-present Byers Professor, School of Electrical and Computer Engineering, Georgia Tech.
9/02-7/04 Professor, School of Electrical and Computer Engineering, Georgia Tech.
9/00-9/02 Philpott-Westpoint Stevens Professor, Electrical and Computer Engineering Department, Auburn University.
4/97-9/00 Professor, Electrical and Computer Engineering Department, Auburn University.
1/01-9/02 Director, Alabama Microelectronics Science and Technology Center, Auburn University.
11/94-1/01 Assistant Director, Alabama Microelectronics Science and Technology Center, Auburn
University.
9/92-4/97     Associate Professor, Electrical and Computer Engineering Department, Auburn University.
1/90-5/92     Adjunct Assistant Professor, Electrical Engineering Department, Columbia University.
1/87-5/90     Adjunct Professor, Mathematics Department, Western Connecticut State University.

Industrial Experience
4/84-9/92     Research Staff, IBM Research Division, T.J. Watson Research Center, Yorktown Heights, NY.

Research Interests
SiGe devices and technology, radiation effects, cryogenic electronics, Si-based RF/microwave/mm-wave circuits, device-circuit interactions, reliability physics, noise, linearity, SiC devices and technology, extreme environments, device simulation, and compact circuit modeling.

Biographical Sketch
John D. Cressler received the B.S. degree in physics from the Georgia Institute of Technology, Atlanta, GA in 1984, and the M.S. and Ph.D. degrees in applied physics from Columbia University, New York, in 1987 and 1990, respectively. From 1984 to 1992 he was on the research staff at the IBM Thomas J. Watson Research Center in Yorktown Heights, NY, and from 1992 to 2002 on the faculty at Auburn University, Auburn, AL.

In 2002, he joined the faculty at the Georgia Institute of Technology (Georgia Tech), where he is currently Byers Professor of electrical and computer engineering. His research interests include: SiGe devices and technology, mixed-signal circuits built from SiGe devices, radiation effects, cryogenic electronics, device-to-circuit interactions, noise and linearity, reliability physics, device-level simulation, and compact circuit modeling. Dr. Cressler has published over 350 papers related to his research. He is the co-author of the book (with Guofu Niu) Silicon-Germanium Heterojunction Bipolar Transistors, Artech House, Boston, MA, 2003, author of the book Reinventing Teenagers: the Gentle Art of Instilling Character in Our Young People, Xlibris, Philadelphia, PA, 2004, and editor of the book Silicon Heterostructure Handbook: Materials, Fabrication, Devices, Circuits, and Applications of SiGe and Si Strained-Layer Epitaxy, CRC Press, New York, NY, 2005.

Dr. Cressler was associate editor for the IEEE Journal of Solid-State Circuits (1998-2001), and is guest editor of the IEEE Transactions on Nuclear Science (2002-2005). He has served on the Technical Program Committees of the IEEE International Solid-State Circuits Conference (1992-1998, 1999-2001), the IEEE Bipolar/BiCMOS Circuits and Technology Meeting (1995-1999), the IEEE International Electron Devices Meeting (1996-1997), the IEEE Nuclear and Space Radiation Effects Conference (2000, 2002-2006), and the IEEE International Reliability Physics Symposium (2005). He was the Technical Program Chair of the 1998 IEEE International Solid-State Circuits Conference (ISSCC), and the Conference Co-chair of the 2004 IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems. He currently serves on the Executive Steering Committee for the IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, as International Advisor for the IEEE European Workshop on Low-Temperature Electronics, on the Technical Program Committee for the IEEE International SiGe Technology and Device Meeting, and on the Executive Committee of the ECS Symposium on SiGe: Materials, Processing, and Devices. He has served as an IEEE Electron Device Society Distinguished Lecturer since 1994, and was awarded the 1994 Office of Naval Research Young Investigator Award for his SiGe research program, the 1996 C. Holmes MacDonald National Outstanding Teacher Award by Eta Kappa Nu, the 1996 Auburn University Alumni Engineering Council Research Award, the 1998 Auburn University Birdsong Merit Teaching Award, the 1999 Auburn University Alumni Undergraduate Teaching Excellence Award, and an IEEE Third Millennium Medal in 2000. He was elected an IEEE Fellow in 2001 “for contributions to the understanding and optimization of silicon and silicon-germanium bipolar transistors.”

Honors and Awards
Eta Kappa Nu, C. Holmes MacDonald National Outstanding Teacher Award, 1996.
Auburn University Birdsong Merit Teaching Award, 1998.
Auburn University Alumni Undergraduate Teaching Excellence Award, 1999.
Auburn University Alumni Engineering Council Outstanding Research Award, 1996.
Office of Naval Research Young Investigator Award, 1994.
IEEE Electron Device Society Distinguished Lecturer, 1994-present.

Professional Society Service
Conference Co-Chair, 2004 IEEE Topical Meeting on Silicon Monolithic circuits in RF Systems (Si RF).
Program Chair, 1998 IEEE International Solid-State Circuits Conference (ISSCC).
Chair, Device Physics Subcommittee, IEEE Bipolar Circuits and Technology Meeting (BCTM), 1996-99.

Honor Societies
Sigma Xi Scientific Research Honor Society, 1990.
Phi Kappa Phi National Honor Society, 1983.
Sigma Pi Sigma Physics Honor Society, 1983.
Phi Eta Sigma Honor Society, 1980.

Best Paper Awards
‡ First Prize, 1995 Institute of Electrical and Electronics Engineers (IEEE) Prize Paper Competition, for invited paper by J.D. Cressler, "Re-Engineering Silicon: Si-Ge Heterojunction Bipolar Technology," IEEE Spectrum, pp. 49-55, March 1995. (IEEE Spectrum has a circulation of over 300,000 worldwide.)

Selected Publications (6 out of a total of >400)
Facilities

We will collaborate with the Goddard team for on-site radiation experiments, sharing equipment as needed, piggybacking on pre-existing NASA experiments. Data collapse and analysis, pre/post experiment measurements will occur at Georgia Tech.

John D. Cressler’s research team, located within the new High-Frequency Systems Laboratory of the Georgia Electronic Design Center (GEDC), is located in the Technology Square Research Building (TSRB) at Georgia Tech, and has exhaustive measurement capabilities for devices and circuits, ranging from \textit{dc} to mm-wave, fA to multi-A, \(\mu\)V to kV, and 4K to 500C. These main measurement facilities of the High-Frequency Systems Lab include specific test systems for:

- high-sensitivity \textit{dc} measurements
- reliability stressing of devices/circuits
- custom low-frequency noise system
- S-parameters (to 110 GHz) – both 2 port and 4 port systems
- broadband noise (to 40 GHz)
- phase noise (to 40 GHz)
- single tone and two tone load-pull for linearity analysis (to 24 GHz)
- BERT testing for high speed digital to 10Gb/sec
- cryogenic measurements (4 dedicated systems for both \textit{dc} and \textit{ac} down to 4K)
- high power / high-temperature \textit{dc} + \textit{ac} + CV (to 500C)
- infrared imaging

Cressler’s research team has substantial experience in analog, digital, and RF through mm-wave circuit design using the Cadence and HP-ADS design environments, and has worked extensively with multiple industrial IC design kits for the design, layout, checking, and tapeout of devices and circuits. A cluster of 40 dedicated high-end Sun workstations in the IC Design Lab adjacent to this measurement lab is dedicated to IC design, as well as device simulation using TCAD tools from Synopsys for 1D, 2D and full 3D simulation of devices. Comprehensive IC fabrication and packaging facilities are available as needed in the Microelectronics Research Center and Packaging Research Center.
Summary of Results
John D. Cressler’s SiGe Devices and Circuits Research Team

Major Accomplishments this Quarter (FY09 Q1)

Publications and Presentations

1 Journal Papers accepted by TNS


1 Conference Paper accepted to IRPS 2008


Radiation Experiments

• 36 MeV O Micro-beam – (10/08 NASA-GSFC, Sandia National Lab)
  - Inverse Cascode, 8HP no DT

• 63 MeV Protons – (11/08 NASA-GSFC, UC Davis)
  - NSC CBC8, 5AM Passives, SiGe MODFET

• Heavy Ion Broad Beam – (12/08 NASA-GSFC, Texas A&M)
  - 8HP SR with External N-ring RHBD Devices

• 2-Photon Pulsed Laser – (01/09 NASA-GSFC, DOD, NRL)
  - 8HP Standard and External N-ring Devices
**TECHNICAL HIGHLIGHTS**

*Ionizing Radiation Damage in 65nm RF CMOS*

- Gate biased vs. all-terminals-grounded during exposure
  - Higher degradation with gate bias indicates stronger role of STI isolation oxide can dominate radiation response of multi-finger RF CMOS

![Graphs showing the difference in degradation between gate biased and all-terminals-grounded conditions.](image)
TECHNICAL HIGHLIGHTS

IBM 8HP Novel Device Structure - Microbeam Charge Collection Data

- Inverse Cascode structures were tested for charge collection statistics
- IBICC measurements with 36MeV Oxygen Ions
- Results were compared to standard 8HP HBTs with identical active area
- Bias scheme employed → All terminals grounded except for Substrate at -4V
- A second variant of the inverse cascode, with a subcollector terminal connection (subcollector-tap) was also tested

Reduction in Peak Collector Charge Collection

Almost Complete Mitigation of Collector Charge Collection!
TECHNICAL HIGHLIGHTS

2-Photon Pulsed Laser Testing

- Standard and External N-Ring 8HP HBTs
- Comparison among charge cloud depth, XY location, laser energy and N-ring voltage

![Image of 2-Photon Pulsed Laser equipment and graph]

2-Photon Pulsed Laser

E-Center

LPE = 24 nJ, Z = 0

8HP $A_E = 0.12 \times 3 \mu m^2$

$V_{NR} = V_C = V_B = V_E = 0$ V

$V_S = -4$ V

Terminal Transient Current (mA)

Time (ns)
TECHNICAL HIGHLIGHTS

Heavy Ion Broad Beam Testing

- 8HP 16-bit Std. M/S Shift Register with external N-ring HBTs
- Variation in substrate ring contacting
TECHNICAL HIGHLIGHTS

**Heavy Ion Broad Beam Testing**

- 3X reduction in saturated cross section at 1 Gbit/s ↑
- No change in threshold LET ↓
- Negligible power penalty compared to other circuit RHBD ↑

![Graph showing error event cross section vs. effective LET for different architectures and technologies.](image-url)
PLANS FOR NEXT QUARTER

Upcoming Radiation Experiments

• March 09 Heavy Ion at TAMU
  - 5AM Shift Registers

• March 09 NRL 2-Photon Pulsed Laser
  - IHP n-ring, 5AM BGR, 8HP n-ring, ECL gates

NSREC Submissions

• 7 papers being presently pursued

PROBLEMS AND CONCERNS

• Slow turn-on new 6 month contract
John D. Cressler’s SiGe Devices and Circuits Research Team
Major Accomplishments this Quarter (FY09 Q2)

Publications and Presentations

6 Conference Paper accepted


1 Conference Paper submitted


Radiation Experiments

• 10 keV X-ray – (04/09 MURI, Vanderbilt University)
  - SiGe MODFET, National FETs, 5AM Inverse Cascode

• March 09 Heavy Ion at TAMU
  - 5AM Shift Registers

• 36 MeV O Micro-beam – (10/08 NASA-GSFC, Sandia National Lab)
  - Inverse Cascode, 8HP no DT
TECHNICAL HIGHLIGHTS

IHP Junction Isolation RHBD

• Junction Isolation applied to 200 GHz IHP npn devices to shunt charge away from the subcollector in the event of an ion strike
• Typical location of DT in comparable technologies is shown by dotted line

Diagram: Structure of IHP Junction Isolation RHBD with labeled parts: Base, Emitter, Collector, n+ S/D, p+ S/D, SIC, Subcollector, p-Well, n-Isolation, 2.20 μm - 2.90 μm
TECHNICAL HIGHLIGHTS

**IHP Junction Isolation RHBD**

- Left figure shows charge collection across a slice through the center of the device, with unhardened and two junction variants.
- Peak charge collection reduced by 20%.
- Right figure shows integrated charge across the same slice.
- Total integrated charge collection reduced by 69%, compared to a 34% reduction for 8HP n-ring structures.
**TECHNICAL HIGHLIGHTS**

**Proton Radiation Damage in SiGe pMODFET on SOS**

- higher Ge concentration → greater mobility enhancement
- slight improvement in transconductance post 63 MeV proton
TECHNICAL HIGHLIGHTS
Proton Radiation Damage in SiGe pMODFET on SOS

- 63 MeV Proton Passive Exposure for 1/f Noise Measurements
- 1/f Noise Decreases After Irradiation (trap assisted phenomenon)
PLANS FOR NEXT QUARTER

Upcoming Radiation Experiments

- NRL 2-Photon Pulsed Laser
  - IHP n-ring, 5AM BGR, 8HP n-ring, ECL gates

PROBLEMS AND CONCERNS

- Lack of substantial funding to support the SiGe effort is a real shame, and in my view should changed. In addition, the new 6 month grant process has introduced time slots without coverage, and substantial inconvenience.
John D. Cressler’s SiGe Devices and Circuits Research Team
Major Accomplishments this Quarter (FY09 Q3)

Publications and Presentations

2 Conference Papers Accepted


Eight NSREC 09 papers to be presented in July in Quebec City, Canada

Radiation Experiments

• Low Dose Rate Gamma – (6/09 Goddard Space Flight Center)
  - 5AM SiGe HBTs, investigation of bias current deviations under total dose irradiation.

• 36 MeV O₂ Microbeam – (5/09 Sandia National Lab)
  - 8HP with and without DT
  - 5AM BGR transients
• Four transistors in parallel were bombarded by 36 MeV oxygen ions
• Transients over the emitter area show the largest amplitudes
TECHNICAL HIGHLIGHTS

Transients in SiGe Regulator

- A bandgap voltage reference was used inside a regulator circuit
- Transient response depends on the location of the strike
TECHNICAL HIGHLIGHTS

**Mixed-mode TCAD**

- 3D TCAD Model of 0.5 x 2.5 μm² SiGe HBT Calibrated to Data

- **Goal:** Leverage 3D Model to Understand Circuit-level SET Effects

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**Device-only SET, gnd + negative V_{sub}**

- $V_S = -4$ V
- $V_B = V_E = V_C = 0$ V

SiGe 5AM HBT, $A_E = 0.5 \times 2.5$

Emitter center strike at 2ps

LET=7 MeV-cm²/mg

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**Device-only SET at BGR node voltages**

- $V_R = 0.747$ V, $V_F = 55$ mV
- $V_C = 0.745$ V, $V_S = 9$ mV

SiGe 5AM HBT, $A_E = 0.5 \times 2.5$

Emitter center strike at 2ps

LET=7 MeV-cm²/mg
TECHNICAL HIGHLIGHTS

True Mixed-mode SET

- CFDRC MixCad (Spectre + 3D NanoTCAD) used to simulate SET
- SiGe HBT Response in BGR Not Equal to Standalone SiGe HBT
- Mixed-mode SET Simulation Shows Long Output Transient
TECHNICAL HIGHLIGHTS
Physics of Ion Strikes

- Promotion of ambipolar carrier diffusion
  - reduce charges reaching sensitive junctions
- Deep Trench Isolation
  - confines carriers in vicinity of subcollector-substrate junction

Q: Will shallower or no DTI mitigate charge collection?
**TECHNICAL HIGHLIGHTS**

**Simulated Removal of Deep Trench**

Completely Removing the Deep Trench from the HP Device Deck
- reduction in peak current & diffusion tail (*less total charge collected*)
- smooth peak carrier broadening over time (*no confinement*)

![Graphs showing Collector Current and Electron Concentration](image)
TECHNICAL HIGHLIGHTS

Time Evolution of Carrier Densities

CP Platform (shallow DT)
- Even peak broadening over time

HP Platform (extensive DT)
- Confinement of electrons within DT

Graphs showing the evolution of electron concentration over time for both CP (left) and HP (right) platforms.
TECHNICAL HIGHLIGHTS

Outside Deep Trench Ion Strikes

Reduced trench depth/ no trench → drastic difference for “outside-DT”
- Larger current transients (more carrier diffusion to sensitive junction)
- Large increase in collected charge
- Distorted waveform for no-DTI case related to junction collapse

Conclusion:
Some form of isolation needed!

Previously reported charge collection mitigation by addition of “NRings”

Junction Isolation
**TECHNICAL HIGHLIGHTS**

**Experimental Deep Trench Analysis**

Two devices irradiated with 36 MeV $^{16}$O ions using a Microbeam

- IBICC performed
- Measured results support Sims
  - less collection at peak
  - more collection outside active area
• Junction Isolation Without Deep Trench
  - n-type well surrounds substrate contact ring and STI
  - tested in a 200 GHz no-DT npn process w/ shallow subcollector
TECHNICAL HIGHLIGHTS
Microbeam Testing

• 5-probe IBICC Measurement (Sandia National Lab)
  - 36 MeV O$_2$ ions, LET= 7 MeV-cm$^2$/mg, 25 µm Si range
  - 50x50 µm$^2$ scan, $V_C=V_{J1}=3$ V, $V_B=V_E=V_{SC}=0$ V
TECHNICAL HIGHLIGHTS
Microbeam Testing

• 69% Decrease in $Q_{C,INT}$ (Largest to Date for Layout RHBD)

36-MeV Oxygen

$A_e = 0.21 \times 0.84 \, \mu m^2$
$V_c = 3.0 \, V$, $V_{iso} = 3.0 \, V$
$T = 300 \, K$

Junction Isolation RHBD

Normalized Integrated Collector Charge

X Position (µm)
TECHNICAL HIGHLIGHTS

Inverse Cascode: Novel Device Structure

- Single device comprised of two devices on a shared subcollector
  - “Upper” device operated in Inverse Mode
  - “Lower” device operated in Forward Mode

- Isolation of the output “Collector” terminal from SEE induced transient
  - analogous to SOI platform, while retaining low cost of bulk platform
  - reduction of sensitive volume to directly under electrical collector
TECHNICAL HIGHLIGHTS

Inverse Cascode: Device Performance

• Characteristic “gummel plot” shows standard operation
  - TID response also shown, standard base leakage component

• AC performance can be optimized to exceed standard inverse mode
• “Standard” Inverse Cascode similar response to standard device
  - Charge collection statistics dependent on inverse cascode bias

• Adding an electrical connection to the subcollector node “CTap”
  - Drastic improvement in charge collection statistics
Simulations of collector-center ion strike explain improvements
- Only current transient due to charge deposited in the CB junction
- Charges in bulk removed through CTap node

Q: How can we add an electrical path for charge on the CTap node?
TECHNICAL HIGHLIGHTS

Inverse Cascode: CTap with Capacitor

- Cadence simulations of capacitive loading on CTap node
  - Larger mitigation with larger capacitance
  - Acceptable losses for amount of mitigation invoked
Accomplishments to Date

- Verification of device functionality (measured hardware)
- Collection of microbeam data
- Verification of experimental data with full 3D Simulations

The Next Steps

- Design of a digital circuit using the inverse cascode with capacitors
  - In progress (designs to be taped-in)
- Heavy Ion Broadbeam testing
PLANS FOR NEXT QUARTER

Upcoming Radiation Experiments

- **NRL 2-Photon Pulsed Laser**
  - IHP bulk HBTs, National & TI complementary devices, 5AM Emitter Followers, SiGe MODFETS, BGRs, VCO, Inverse Cascode devices
- **SNL Microbeam Experiment**
  - National complementary HBTs
- **Texas A&M Heavy-Ion Broad Beam**

PROBLEMS AND CONCERNS

The funding path / timing over the past year has left a lot to be desired. We need to get next round of funding in place as soon as we can. Major stretches between funding increments make Professor’s lives (and their students) very uncomfortable.